Design Note:

HFDN-41.0

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Interfacing to the MAX3815 DVI/HDMI Cable Equalizer

maxim integrated™

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1 Introduction

This design note discusses how to properly interface high-frequency signals to the inputs and outputs of the MAX3815 DVI/HDMI cable equalizer. Designs using correct interfacing techniques will ensure that the MAX3815 performs to its specifications.

2 Problem Description

The maximum data rate for the transition minimized differential signaling (TMDS) channels is 1.65Gbps. Electrical signals with such fast edge speeds, as low as 75ps, require significant attention in the design of the interface and transmission lines so that bits do not become distorted and potentially unrecoverable.

3 Stubs

Do not create any stubs that hang off of the input or output transmission lines. These will create channels for the electrical signal to flow down, reflect back, and interfere with the transmitted signal. Generally, stubs will create stair-step transitions that will partially close the data eye (Figure 1).

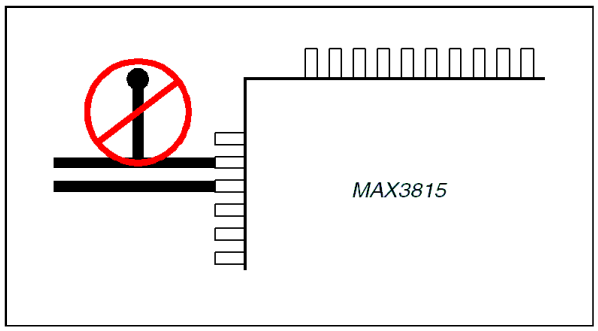

Figure 1. PCB layout with unwanted stub

4 De-skewing Lines within a Data Pair

Do not attempt to de-skew within a single data pair. Use differential coupled transmission lines because the phase of the high frequency signals will be maintained even if the pair goes around corners. The interaction of the electrical fields helps to keep them in phase with each other (Figure 2).

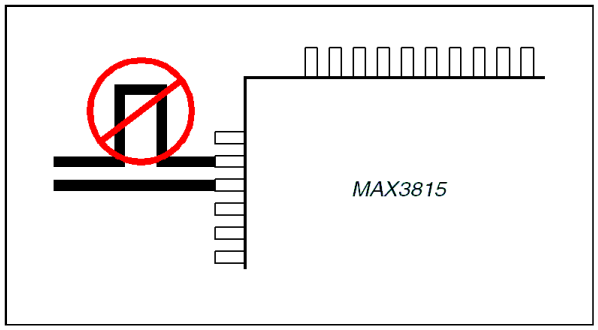

Figure 2. Intrapair de-skewing

5 Differential Impedance

Design the TMDS lines so that they have a differential impedance of 100Ω. By coupling the differential transmission lines, the signals on the "+" and "-" lines will stay in phase with each other and match the load termination. Careful consideration of the trace width, trace spacing, and dielectric thickness all contribute to the characteristic impedance of the differential pair.

6 Crosstalk

The transmission lines for the differential pairs should be kept separated (s) greater than four times the dielectric height (h), see Figure 3.

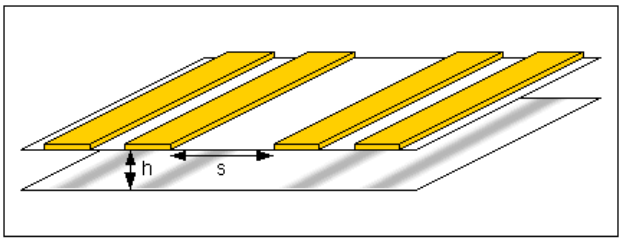

Figure 3. Channel separation

Grounded metal strips can also be used to reduce crosstalk between the pairs. The strips should be tied or "stitched" to the ground plane using vias. Do not leave a long peninsula-like section of the ground strip unconnected to ground because it can act like an antenna and resonate at specific frequencies (Figure 4).

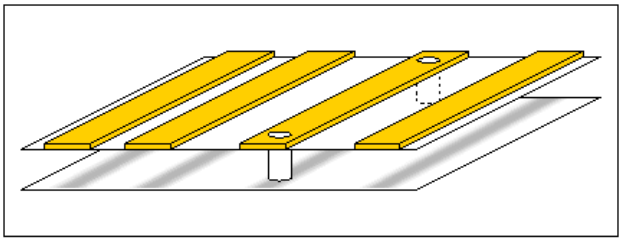

Figure 4. Channel isolation strips

7 Signal Routing Flexibility

Note that the data channels on the MAX3815 do not have to match the order or polarity of the TMDS transmitter or receiver. They just need to match as though the MAX3815 is transparent. Of course the TMDS transmitter's CLOCK signal cannot go to the MAX3815's data inputs, it must go to the RXC_IN. Likewise, the MAX3815's RXC_OUT must go to the TMDS receiver's CLOCK input (Figure 5).

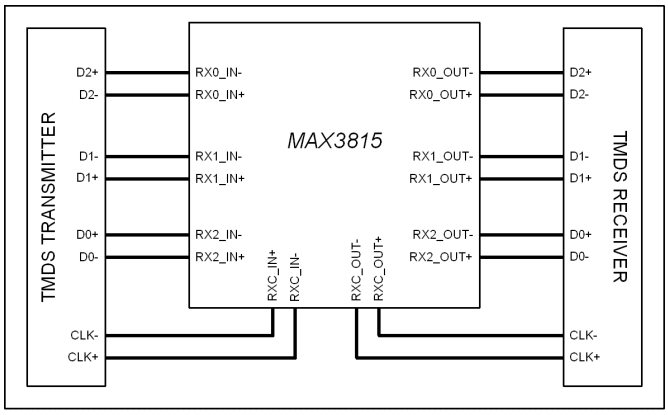

Figure 5. Possible routing option

8 Back Termination

Back terminations should only be used in circumstances where the MAX3815 is driving a known receiver and testing has been done to ensure that the TMDS receiver can tolerate a reduced amplitude signal.

An example of an application where back terminations might be used is a DVI input on an LCD monitor. In this case the MAX3815 is driving a specific TMDS receiver, possibly through a flex cable and multiple connectors that could degrade the signal due to reflections. Using 200Ω back terminations will attenuate the MAX3815's output voltage swing by 33% but can actually improve the system's jitter budget (Figure 6).

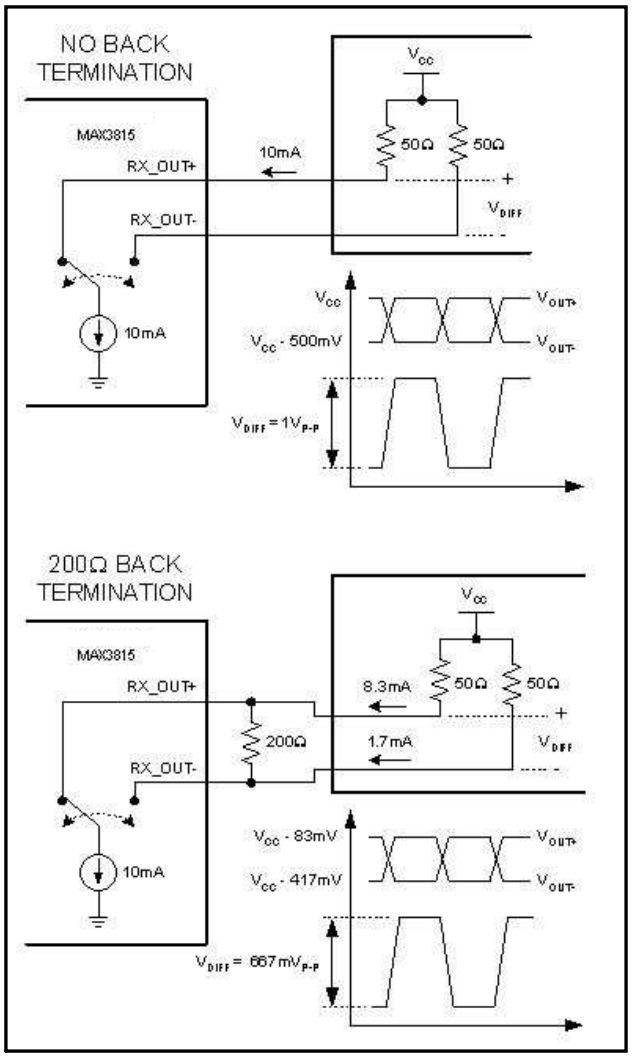

Figure 6. Back termination amplitude reduction

9 ESD Protection

The use of common-mode chokes on the output of the MAX3815 can significantly reduce the eye opening. Many common-mode chokes are designed to work with USB or IEEE1394 signals that generally have a maximum data rate of 480Mbps. Since TMDS signals operate up to 1.65Gbps, the frequencies transmitted are approximately four times higher. Very low capacitance ESD protection is required in order to maintain rise/fall times of the TMDS signals. The MAX3208E is a low capacitance, ±15kV Human Body Model, ESD protection IC designed to protect high data-rate signal lines while only adding 2.6pF (typical value) of parasitic capacitance. The effect of this capacitance can be further reduced by reducing board capacitance where MAX3208E contacts the board.

10 Supply Filtering

Proper power supply filtering is required to achieve good performance from the MAX3815. If components are allowed on the back side of the PCB, a nice low-inductance technique of supply decoupling is to place the capacitors on the bottom side of the board. One end of the capacitor is connected to the bottom side exposed-pad thermal landing, and the other end of the capacitor connects up through a via to the V_{CC} connection on the input side of the MAX3815 (Figure 7).

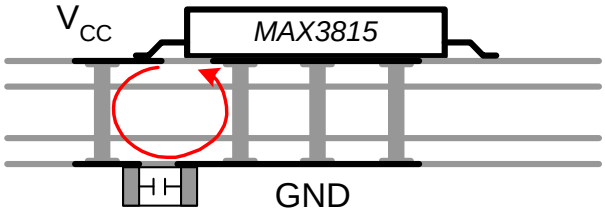

Figure 7. Supply decoupling capacitor location on bottom side of PCB

If the back side of the PCB is not populated with components, then place the decoupling capacitors as close as possible to the IC. Use a 0.01µF capacitor between each of the data input pairs, see Figure 8.

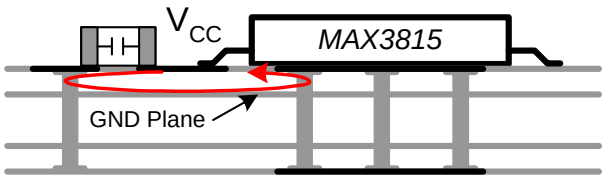

Figure 8. Supply decoupling capacitor location on top side of PCB

11 References

Digital Display Working Group 1999. Digital Visual Interface DVI, Revision 1.0.

HDMI Licensing, LLC 2004. High-Definition Multimedia Interface, Specification Version 1.1.