

**MOSFET – N-Channel,
DUAL COOL[®] DFN8,
POWERTRENCH[®]
40 V, 192 A, 1.1 mΩ**

FDMS8320LDC

Features

- Max $R_{DS(on)}$ = 1.1 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 44\text{ A}$
- Max $R_{DS(on)}$ = 1.5 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 37\text{ A}$
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free, Halogen Free and RoHS Compliant

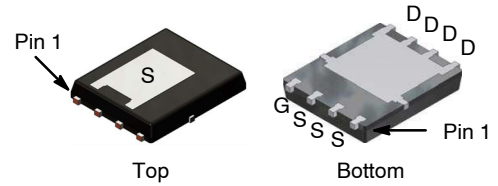
Applications

- OringFET/Load Switching
- Synchronous Rectification
- DC-DC Conversion

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

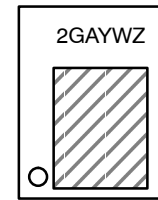
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed (Note 4)	192	A
		44	
		300	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	661	mJ
P_D	Power Dissipation, $T_C = 25^\circ\text{C}$	125	W
	Power Dissipation, $T_A = 25^\circ\text{C}$ (Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

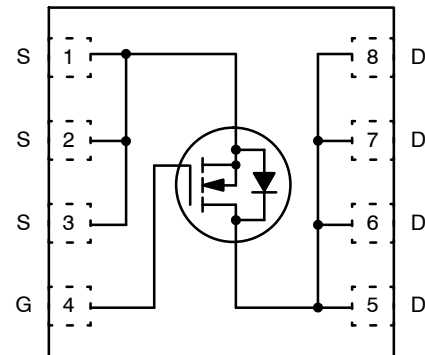


DFN8
DUAL COOL
CASE 506EG

MARKING DIAGRAM



- 2G = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- Z = Assembly Lot Code



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMS8320LDC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40	-	-	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	-	22	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	-	-	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.6	3.0	V
ΔV _{GS(th)} /ΔT _J	Gate-to-Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	-	-6	-	mV/°C
R _{DS(on)}	Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 44 A	-	0.8	1.1	mΩ
		V _{GS} = 4.5 V, I _D = 37 A	-	1.1	1.5	
		V _{GS} = 10 V, I _D = 44 A, T _J = 125°C	-	1.2	1.7	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 44 A	-	244	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	8310	11635	pF
C _{oss}	Output Capacitance		-	2255	3160	pF
C _{rss}	Reverse Transfer Capacitance		-	132	185	pF
R _g	Gate Resistance	f = 1 MHz	0.1	1.4	2.6	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 20 V, I _D = 44 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	-	19	34	ns
t _r	Rise Time		-	15	27	ns
t _{d(off)}	Turn-Off Delay Time		-	69	110	ns
t _f	Fall Time		-	14	25	ns
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 10 V, V _{DD} = 20 V, I _D = 44 A	-	121	170	nC
Q _{g(ToT)}	Total Gate Charge	V _{GS} = 0 to 4.5 V, V _{DD} = 20 V, I _D = 44 A	-	57	80	nC
Q _{GS}	Gate-to-Source Charge	V _{DD} = 20 V, I _D = 44 A	-	21	-	nC
Q _{gd}	Gate-to-Drain "Miller" Charge	V _{DD} = 20 V, I _D = 44 A	-	16	-	nC

DRAIN-SOURCE DIODE CHARACTERISTIC

V _{SD}	Source-to-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.6 A (Note 2)	-	0.7	1.1	V
		V _{GS} = 0 V, I _S = 44 A (Note 2)	-	0.8	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 44 A, di/dt = 100 A/μs	-	65	104	ns
Q _{rr}	Reverse Recovery Charge		-	57	91	nC
t _{rr}	Reverse Recovery Time	I _F = 44 A, di/dt = 300 A/μs	-	49	79	ns
Q _{rr}	Reverse Recovery Charge		-	89	143	nC

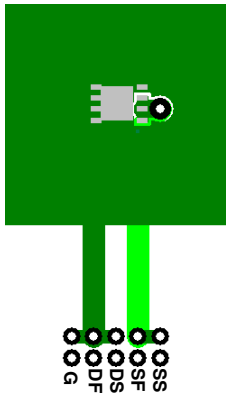
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.9	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 38°C/W when mounted on a 1 in² pad of 2 oz copper



b. 81°C/W when mounted on a minimum pad of 2 oz copper

- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- 200FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
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- 200FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

- E_{AS} of 661 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 21$ A, $V_{DD} = 40$ V, $V_{GS} = 10$ V. 100% test at $L = 0.1$ mH, $I_{AS} = 66$ A.

- Pulse Id measured at 250 μs, refer to Figure 11 SOA graph for more details.

FDMS8320LDC

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

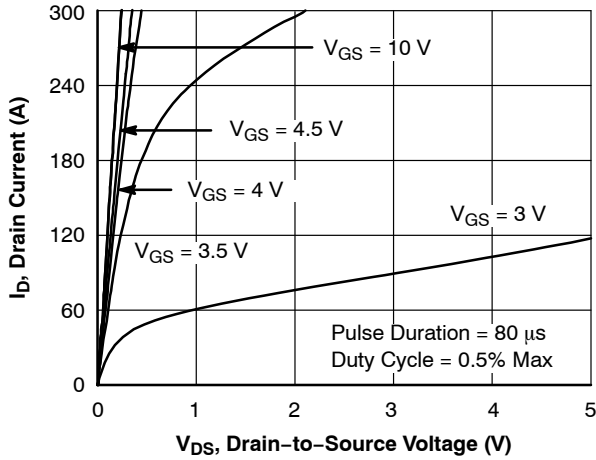


Figure 1. On-Region Characteristics

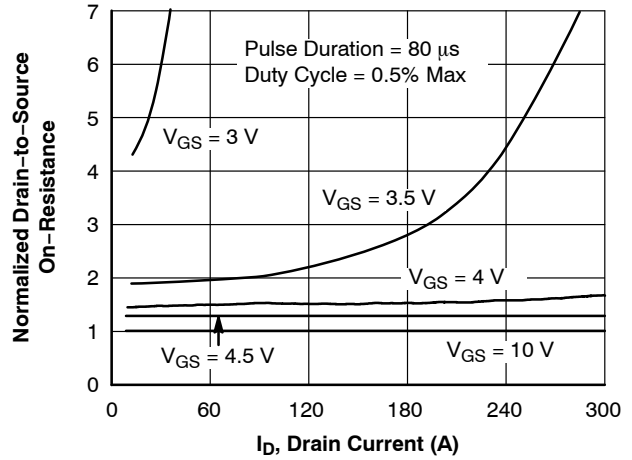


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

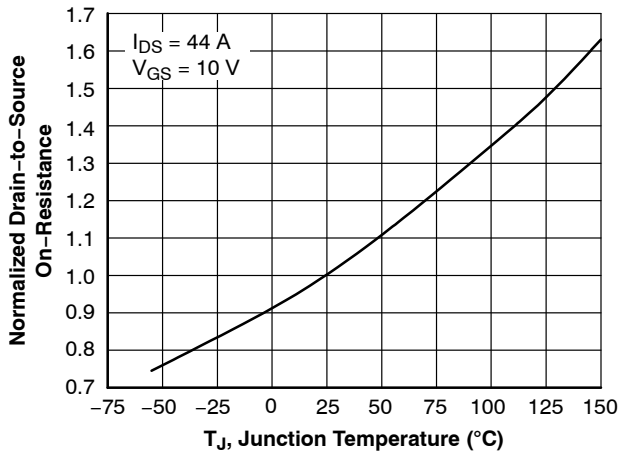


Figure 3. Normalized On-Resistance vs. Junction Temperature

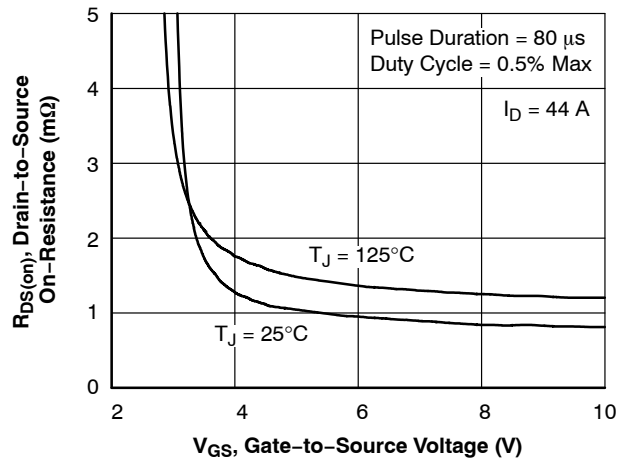


Figure 4. On-Resistance vs. Gate-to-Source Voltage

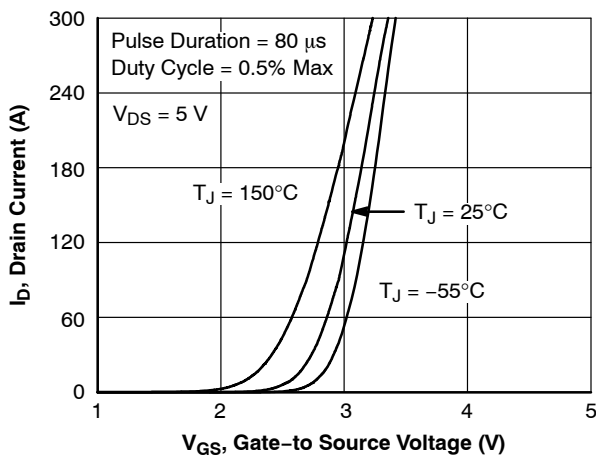


Figure 5. Transfer Characteristics

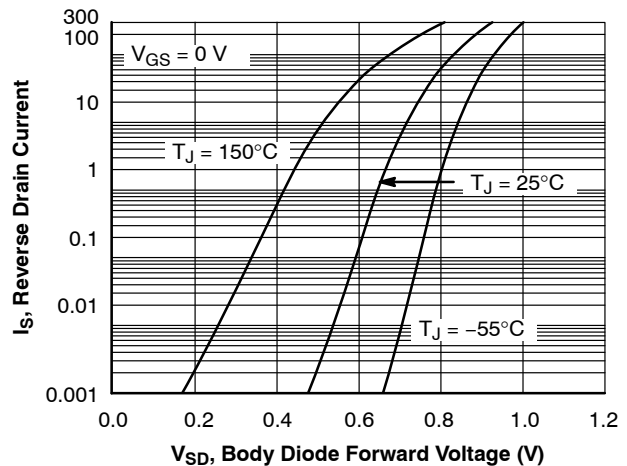


Figure 6. Source-to-Drain Diode Forward Voltage vs. Source Current

FDMS8320LDC

TYPICAL CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

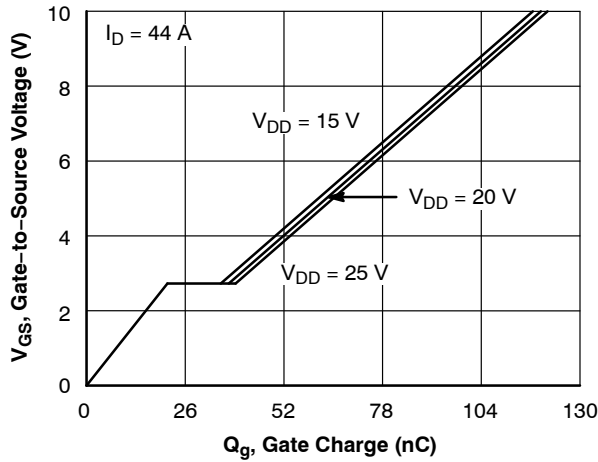


Figure 7. Gate Charge Characteristics

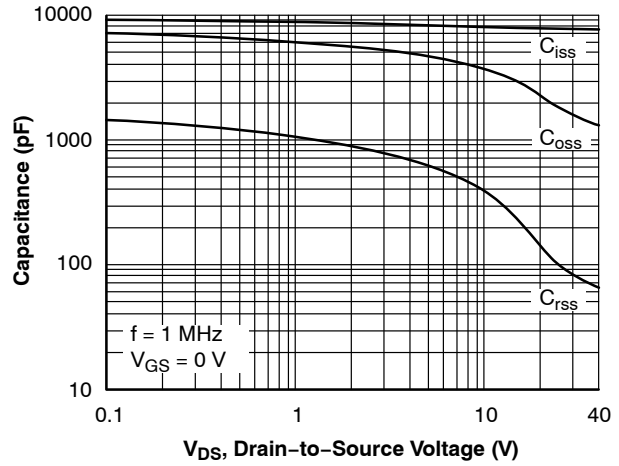


Figure 8. Capacitance vs. Drain-to-Source Voltage

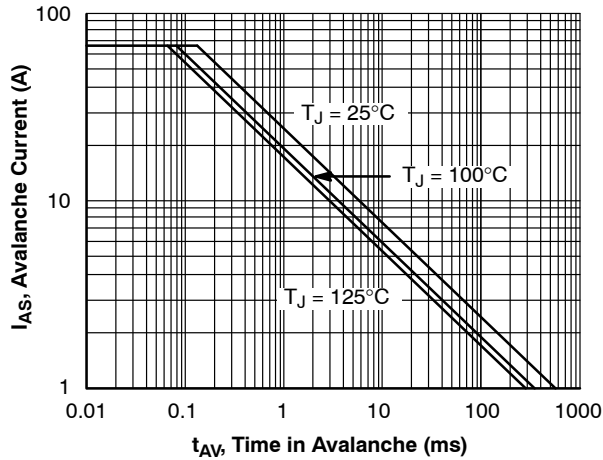


Figure 9. Unclamped Inductive Switching Capability

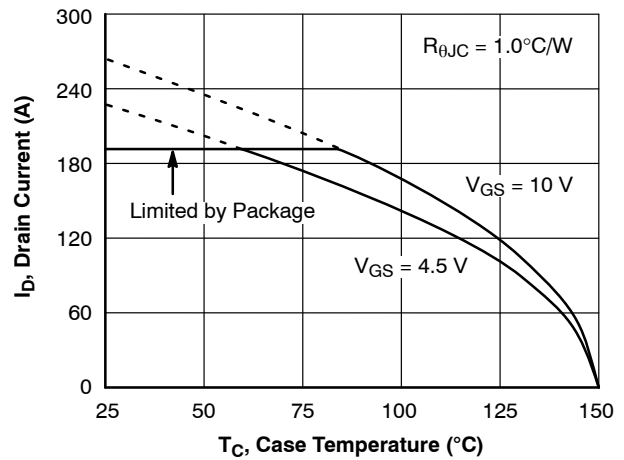


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

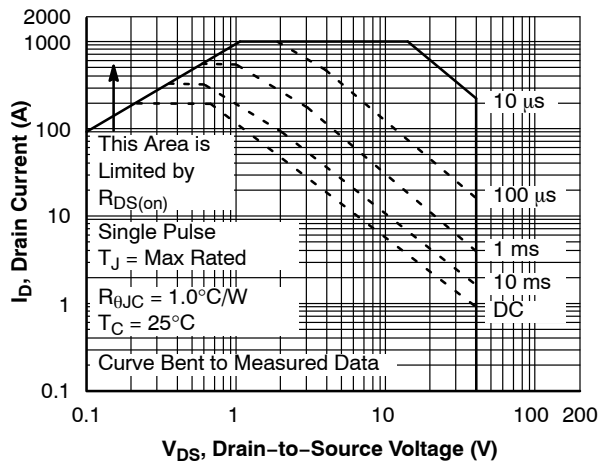


Figure 11. Forward Bias Safe Operating Area

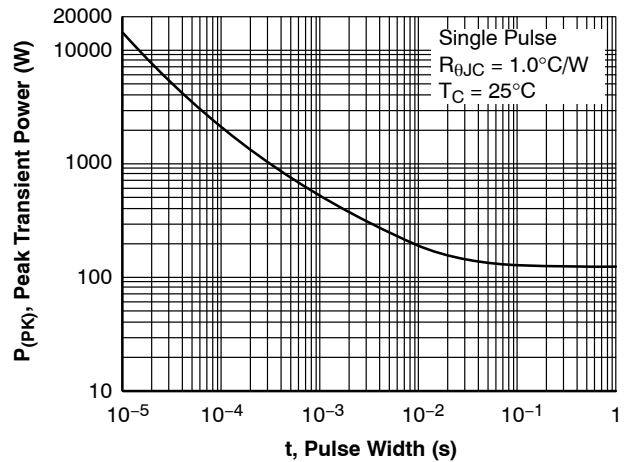


Figure 12. Single Pulse Maximum Power Dissipation

FDMS8320LDC

TYPICAL CHARACTERISTICS (CONTINUED)

($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

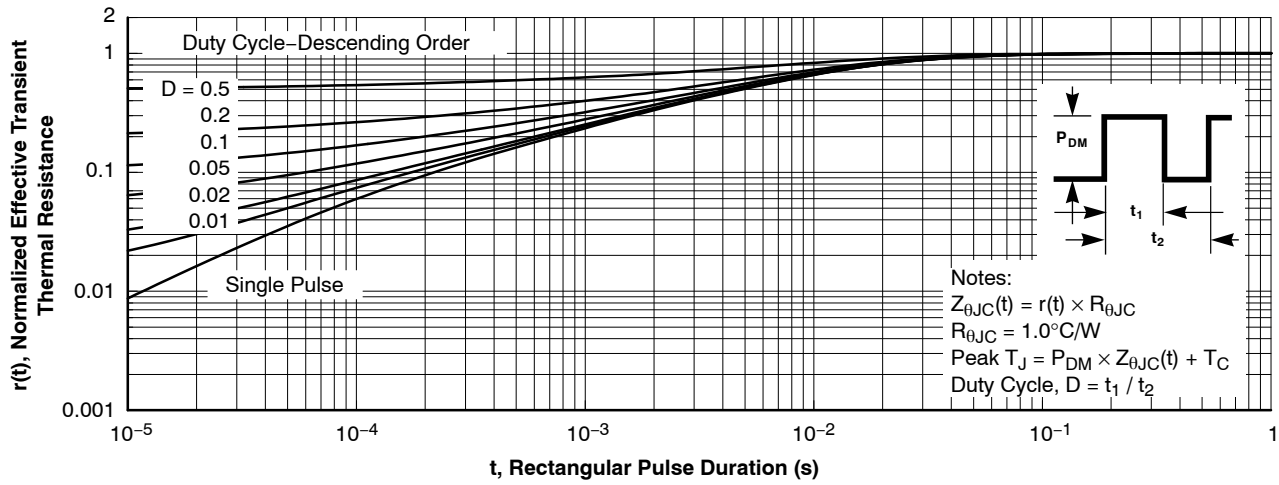


Figure 13. Junction-to-Case Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size [†]	Tape Width	Quantity
FDMS8320LDC	2G	DUAL COOL 56	13"	12 mm	3000 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

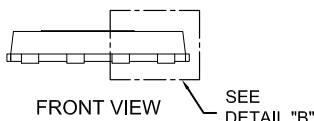
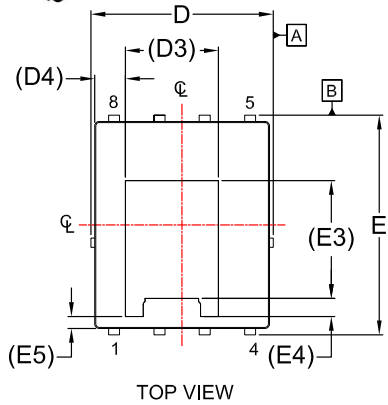
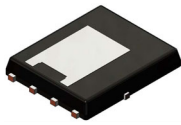
PACKAGE DIMENSIONS

ON Semiconductor®



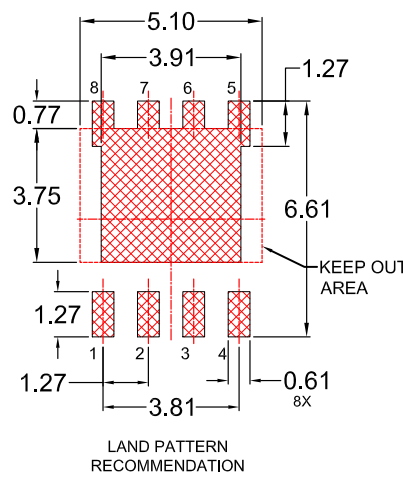
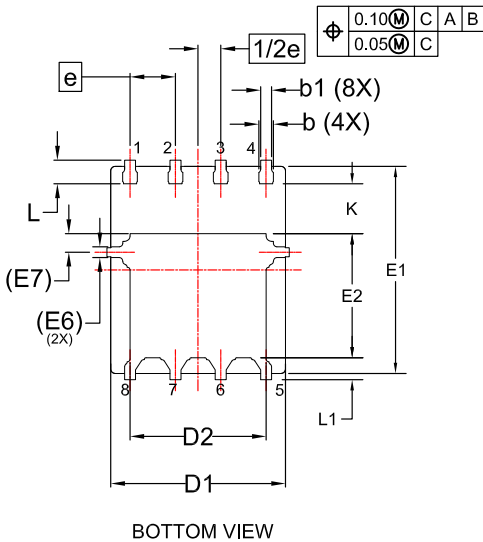
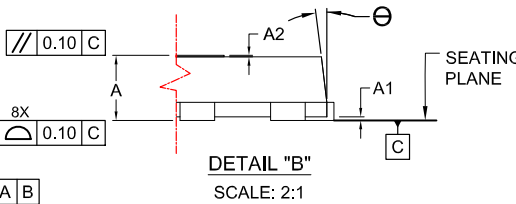
DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

DATE 25 AUG 2020



NOTES:

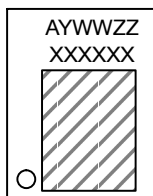
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFN8 5x6.15, 1.27P, DUAL COOL	PAGE 1 OF 1

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