

Features

- Ideal Rewritable Attribute Memory
- Simple Write Operation
 - Self-Timed Byte Writes
 - On-chip Address and Data Latch for SRAM-like Write Operation
 - Fast Write Cycle Time - 1 ms
 - 5-Volt-Only Nonvolatile Writes
- End of Write Detection
 - RDY/BUSY Output
 - DATA Polling
- High Reliability
 - Endurance: 100,000 Write Cycles
 - Data Retention: 10 Years Minimum
- Single 5-Volt Supply for Read and Write
- Very Low Power
 - 30 mA Active Current
 - 100 μ A Standby Current

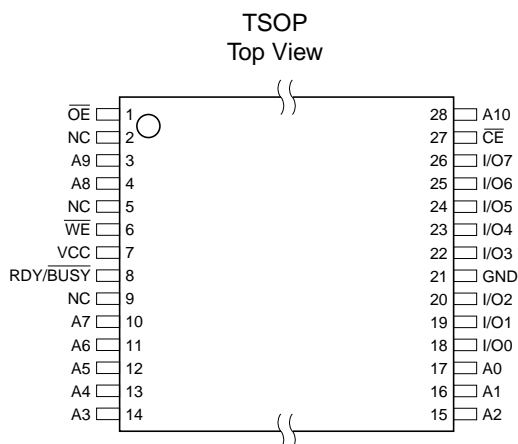
Description

The AT28C16-T is the ideal nonvolatile attribute memory: it is a low power, 5-volt-only byte writable nonvolatile memory (EEPROM). Standby current is typically less than 100 μ A. The AT28C16-T is written like a Static RAM, eliminating complex programming algorithms. The fast write cycle times of 1 ms, allow quick card reconfiguration in-system. Data retention is specified as 10 years minimum, precluding the necessity for batteries. Three access times have been specified to allow for varying layers of buffering between the memory and the PCMCIA interface.

The AT28C16-T is accessed like a Static RAM for read and write operations. During a byte write, the address and data are latched internally. Following the initiation of a write cycle, the device will go to a busy state and automatically write the latched data using an internal control timer. The device provides two methods for detecting the end of a write cycle; the RDY/BUSY output and DATA POLLING of I/O₇.

Pin Configurations

Pin Name	Function
A0 - A10	Addresses
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/BUSY	Ready/Busy Output
NC	No Connect



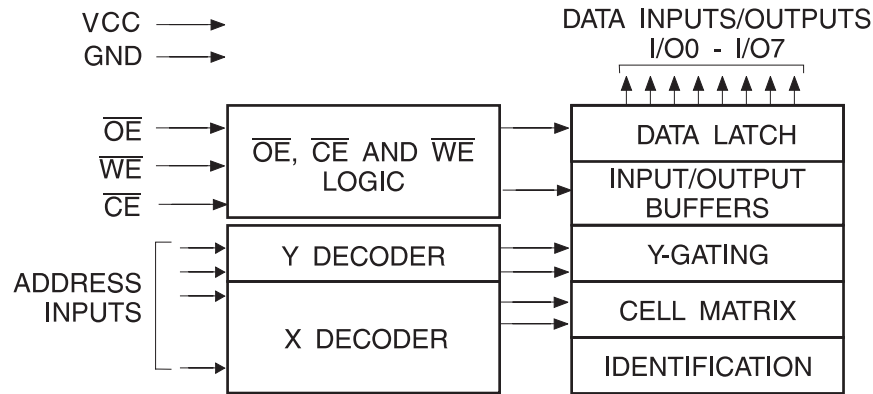
**16K (2K x 8)
PCMCIA
Nonvolatile
Attribute
Memory**

AT28C16-T

Rev. 0258C-10/98



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +125°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{CC} + 0.6V$
Voltage on \overline{OE} and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The AT28C16-T is accessed like a Static RAM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16-T is similar to writing into a Static RAM. A low pulse on \overline{WE} or \overline{CE} input with \overline{OE} high and \overline{CE} or \overline{WE} low (respectively) initiates a byte write. The address is latched on the falling edge of \overline{WE} or \overline{CE} (whichever occurs last) and the data is latched on the rising edge of \overline{WE} or \overline{CE} (whichever occurs first). Once a byte write is started it will automatically time itself to completion. For the AT28C16-T the write cycle time is 1 ms maximum. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

READY/BUSY: Pin 1 is an open drain $\overline{READY/BUSY}$ output that indicates the current status of the self-timed internal write cycle. $\overline{READY/BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain output allows OR-tying of several devices to a common interrupt input.

DATA POLLING: The AT28C16-T also provides \overline{DATA} polling to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16-T may be set to the high state by the Chip Clear operation. By setting \overline{CE} low and \overline{OE} to 12V, the chip is cleared when a 10 ms low pulse is applied to \overline{WE} .

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ($\pm 0.5V$) and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.



DC and AC Operating Range

		AT28C16-15T
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
V _{CC} Power Supply		5V ± 10%

Operating Modes

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z
Chip Erase	V _{IL}	V _H ⁽³⁾	V _{IL}	High Z

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC Programming Waveforms.
 3. V_H = 12.0V ± 0.5V.

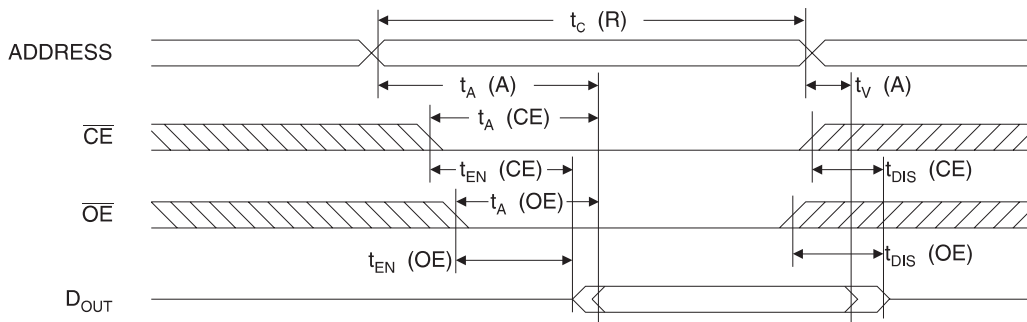
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC} + 1.0V		100	μA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC} + 1.0V	Com.	2	mA
			Ind.	3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA	Com.	30	mA
			Ind.	45	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

AC Read Characteristics

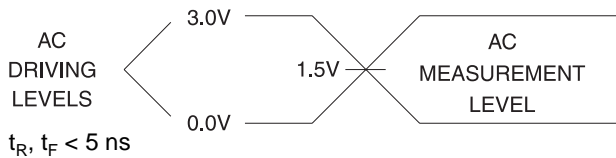
PCMCIA Symbol	Atmel Symbol	Parameter	AT28C16-15T		Units
			Min	Max	
t_C (R)	t_{RC}	Read Cycle Time	150		ns
t_A (A)	t_{ACC}	Address Access Time		150	ns
t_A (CE)	$t_{CE}^{(1)}$	\overline{CE} Access Time		150	ns
t_A (OE)	$t_{OE}^{(2)}$	\overline{OE} Access Time	0	75	ns
t_{EN} (CE)	$t_{LZ}^{(4)}$	Output Enable Time From \overline{CE}	0		ns
t_{EN} (OE)	$t_{OLZ}^{(4)}$	Output Enable Time From \overline{OE}	0		ns
t_V (A)	t_{OH}	Output Hold Time	0		ns
t_{DIS} (CE)	$t_{DF}^{(3)(4)}$	Output Disable Time From \overline{CE}	0	50	ns
t_{DIS} (OE)	$t_{DF}^{(3)(4)}$	Output Disable Time From \overline{OE}	0	50	ns

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

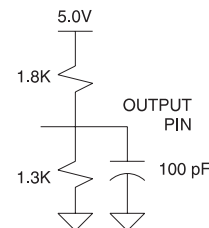


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



Output Test Load



Pin Capacitance

$f = 1$ MHz, $T = 25^\circ\text{C}^{(1)}$

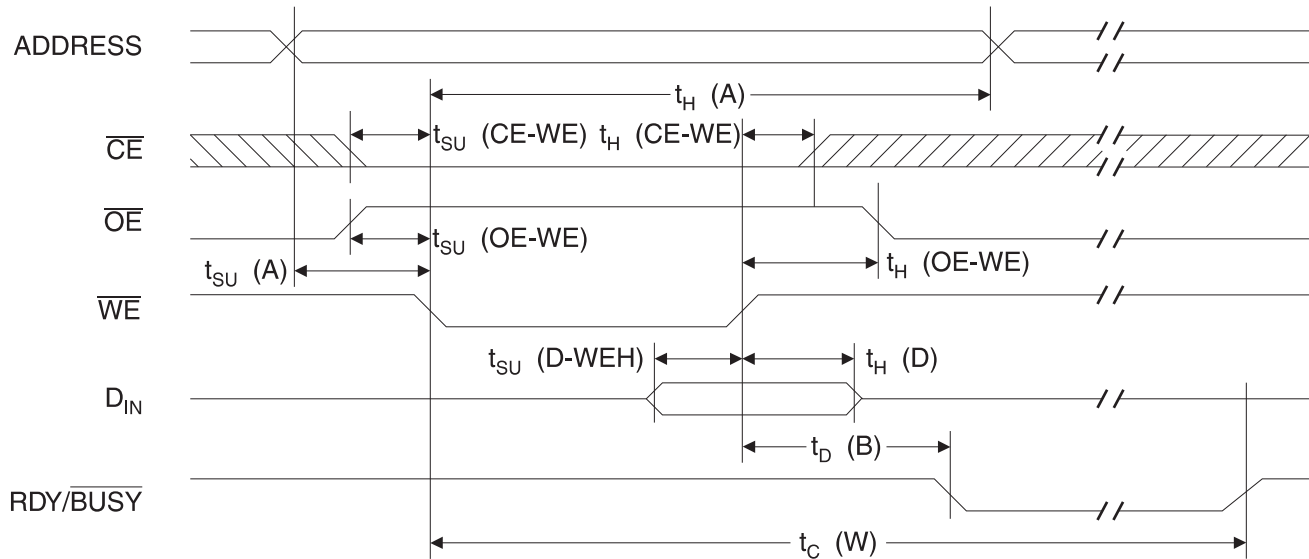
Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

- Note: 1. This parameter is characterized and is not 100% tested.

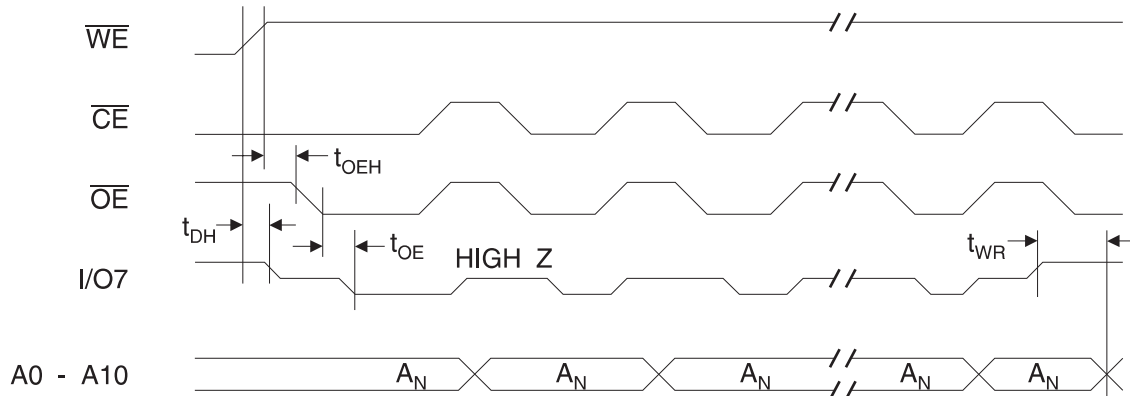
AC Write Characteristics

PCMCIA Symbol	Atmel Symbol	Parameter	Min	Max	Units
$t_{SU} (A)$	t_{AS}	Address Setup Time	10		ns
$t_{SU} (OE-WE)$	t_{OES}	Output Disable Time To \overline{WE}	10		ns
$t_{SU} (CE-WE)$	t_{CS}	Chip Enable Time To \overline{WE}	0		ns
$t_W (WE)$	t_{WP}	Write Enable Pulse Width	100	1000	ns
$t_{SU} (D-WEH)$	t_{DS}	Data Setup To \overline{WE} High	50		ns
$t_H (A)$	t_{AH}	Address Hold Time From \overline{WE}	50		ns
$t_H (D)$	t_{DH}	Data Hold Time From \overline{WE} High	10		ns
$t_H (OE-WE)$	t_{OEH}	Output Enable Hold Time From \overline{WE} High	10		ns
$t_H (CE-WE)$	t_{CH}	Chip Enable Hold Time From \overline{WE} High	0		ns
$t_D (B)$	t_{DB}	Delay From \overline{WE} High To \overline{BUSY} Asserted		50	ns
$t_C (W)$	t_{WC}	Write Cycle Time		1	ms

AC Write Waveforms

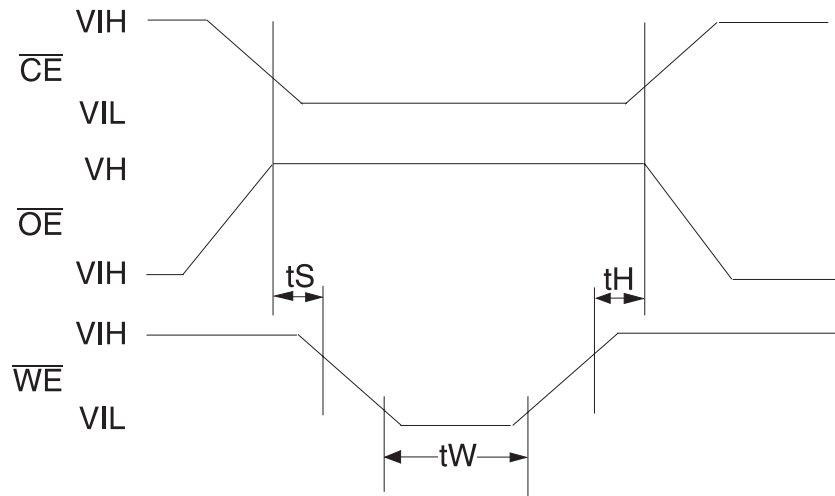


Data Polling Waveforms



Note: 1. Data Polling AC Timing Characteristics are the same as the AC Read Characteristics.

Chip Erase Waveforms



$t_S = t_H = 1 \mu\text{sec (min.)}$

$t_W = 10 \text{ msec (min.)}$

$V_H = 12.0 \pm 0.5V$



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16-15TC	28T	Commercial (0°C to 70°C)
	45	0.1	AT28C16-15TI	28T	Industrial (-40°C to 85°C)

- Notes:
1. See Valid Part Numbers table below.
 2. The 28C16 200 ns and 250 ns speed selections have been removed from valid selections table and are replaced by the faster 150 ns T_{AA} offering.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	15	TC, TI

Die Products

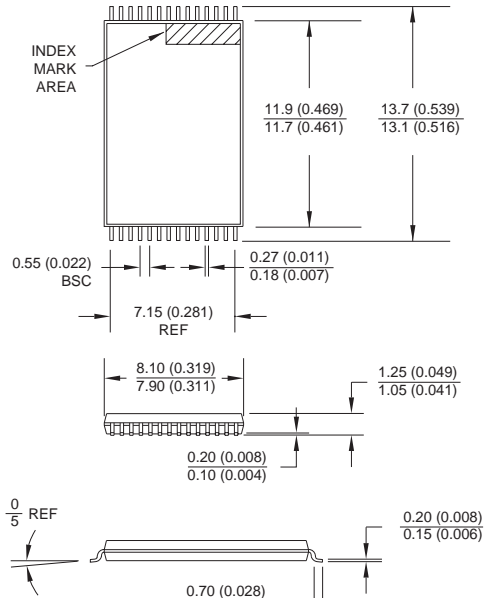
Reference Section: Parallel EEPROM Die Products

Package Type	
28T	28-Lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

28T, 28-Lead, Plastic Thin Small Outline Package (TSOP)

Dimensions in Millimeters and (Inches)*



*Controlling dimension: millimeters





Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Japan

Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

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