To: Valued Customer

Issue Date ：22 May 2020

Toshiba Electronic Devices & Storage Corporation
System Devices Marketing Center
System Devices Sales & Marketing Dept.
Logic LSI & Microcomputer Group

Product Announcement: Product defect announcement for xxxxxxxxxxxxxxxxx

Thank you for your constant support to Toshiba Products.

As per captioned, Toshiba announces product defect disclosure for xxxxxxxxxxxxxxxxx
Please see attached for full list of product affected.

Part Number affected:

TMPM066, M3H (Group1), M3H (Group 2), M4K (Group 1), M4K (Group 2)

The reason of announcement:

Discovery of technical limitation for certain function related to MCU IP operation.

Technical disclosure on product function limitation condition and workaround described in attached.
Final errata for affected product will be made available on-line in coming month.

For questions or concerns regarding this notification, please feel free to contact your local sales office or Customer service representative.

Sincerely yours,

To: Distributor

Product defect related to Serial Peripheral Interface (TSPI) utilize DMA Controller (DMAC)

TOSHIBA

2020/May/27

Toshiba Electronic Devices & Storage Corporation

Toshiba Electronic Device Solutions Corporation

Product defect discovery for certain Toshiba MCU operation:

Thank you for using Toshiba microcontrollers.

In the data transfer of DMAC + TSPI, a problem was found that some data was discarded.

This document will address the phenomenon and workaround.

We apologize for any inconvenience, but we ask that you review the content.
If you have any questions about this matter, please contact our sales representative.

Technical terms explanation

The function	Technical Terms	The explanation
Related Function		DMAC, APB Interface, TSPI
TSPI	TSPI	Toshiba Serial Peripheral Interface
	FIFO	Transmit/Receive FIFO　8 stage (7 to 16-bit), 4 stage(17 to 32-bit)
	BREQ, SREQ	DMA Request BREQ (Burst-transfer request) cab transfer multiple data with one request. (Number of transfers depends on DMA settings register.) SREQ (Single-transfer request) can transfer one data with one request.
	Fill level (n)	DMA Transmit : BREQ and SREQ are generated when FIFO level N and under. SREQ will occur if there is FIFO space.
DMAC	DMAC	DMA controller
	Arbitration	Arbitration interval = Number of transfer when BREQ occurs.
	Single-transfer is disabled	DMAC can ignore SERQ when burst transfer is possible by single-transfer is disable. However, if the remaining transfer count is a fraction less than the burst transfer count, single transfer is automatically enabled.
APB Interface	Write-buffer	The bus arbitration circuit between AHB and APB bus has a single-stage write buffer. The DMAC releases the AHB bus first when write to the write buffer is completed. After that, DMAC writes to the APB bus. * There is a time lag between DMAC and peripheral write timing.

Conditions/phenomena observed in use of product

【Applicable products】

M3H Group(1), M3HGroup(2), M4K Group(1), M4K Group(2)

*Detailed product names are shown in the bottom of this document.

【Configuration that occur】

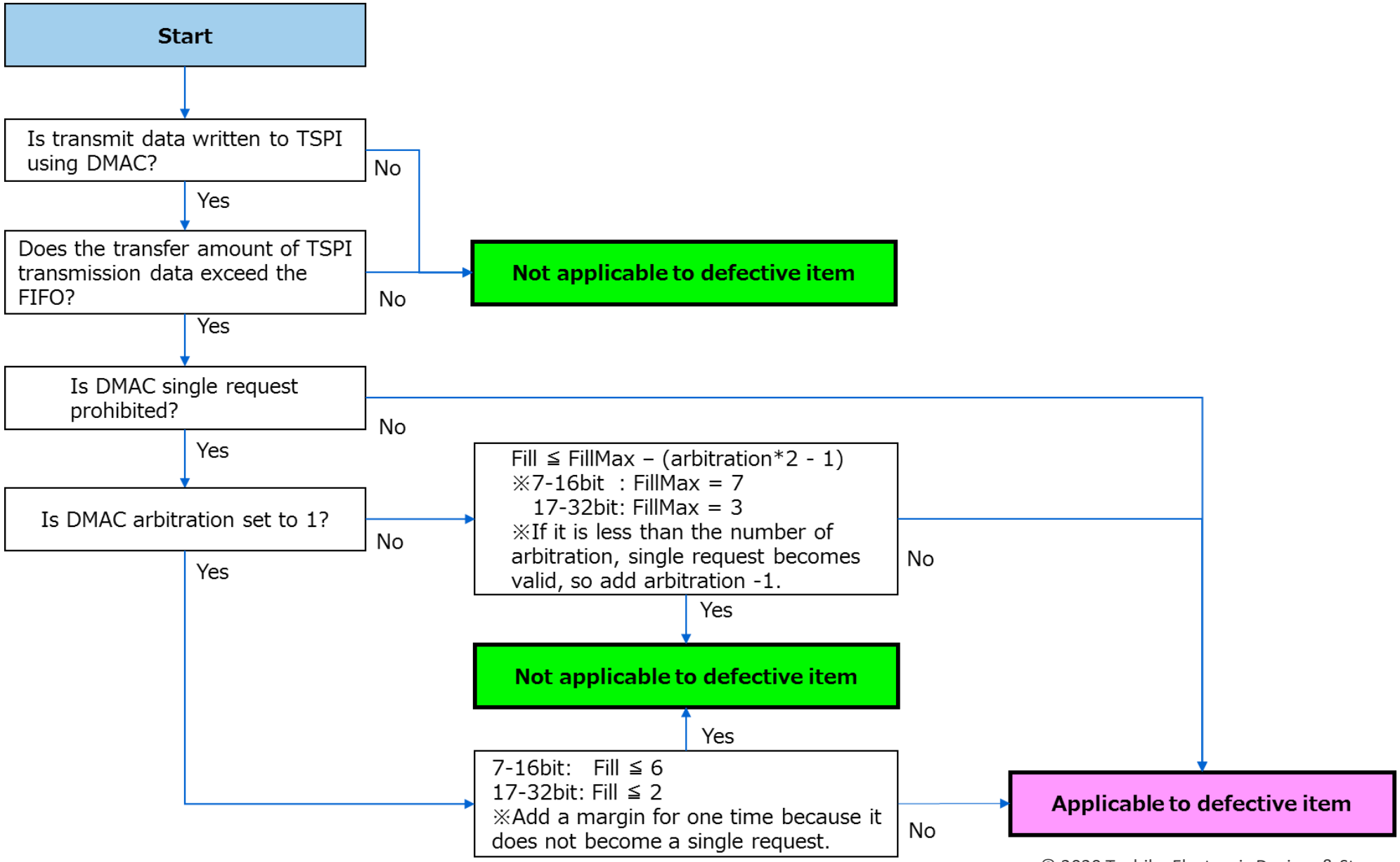
Combination of DMAC + APBIF + TSPI

【Phenomenon】

When transmitting data to TSPI using the DMAC, FIFO control may not be performed correctly depending on the DMAC and TSPI setting conditions, and the data transferred by the DMAC to the TSPI may be discarded.

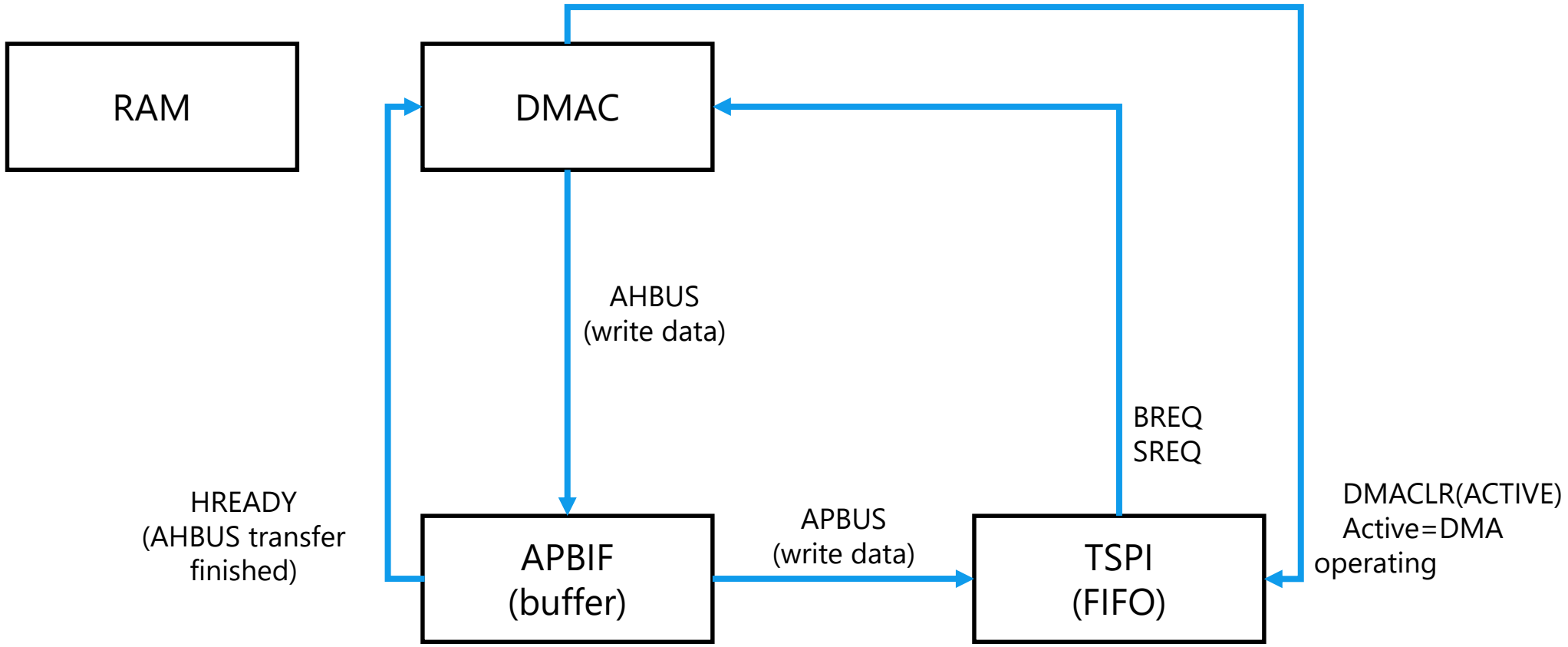
The following page shows the check flow of the occurrence conditions.

DMAC+TSPI Check flow



Block diagram DMAC+APBIF+TSPI

Related block diagram

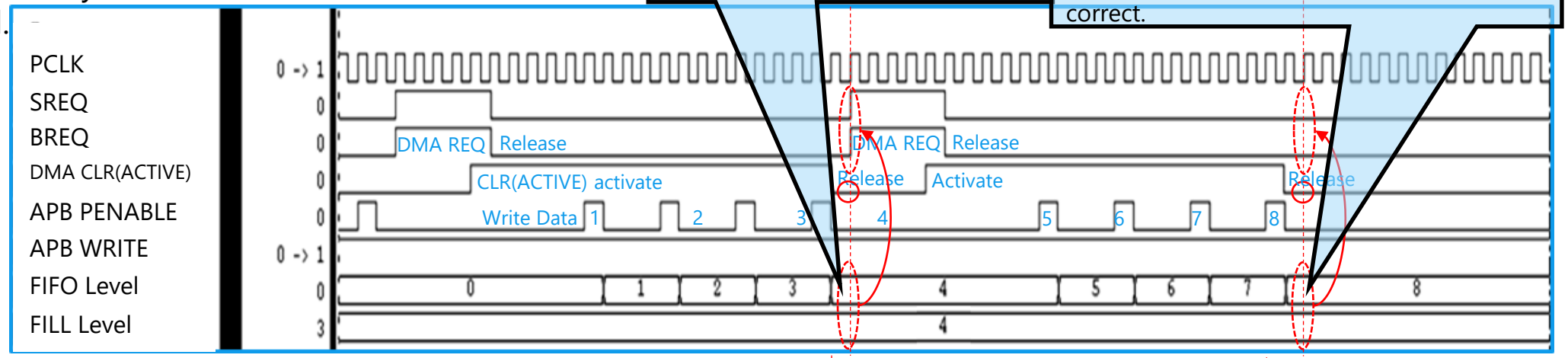


The problem will be described to next slide.

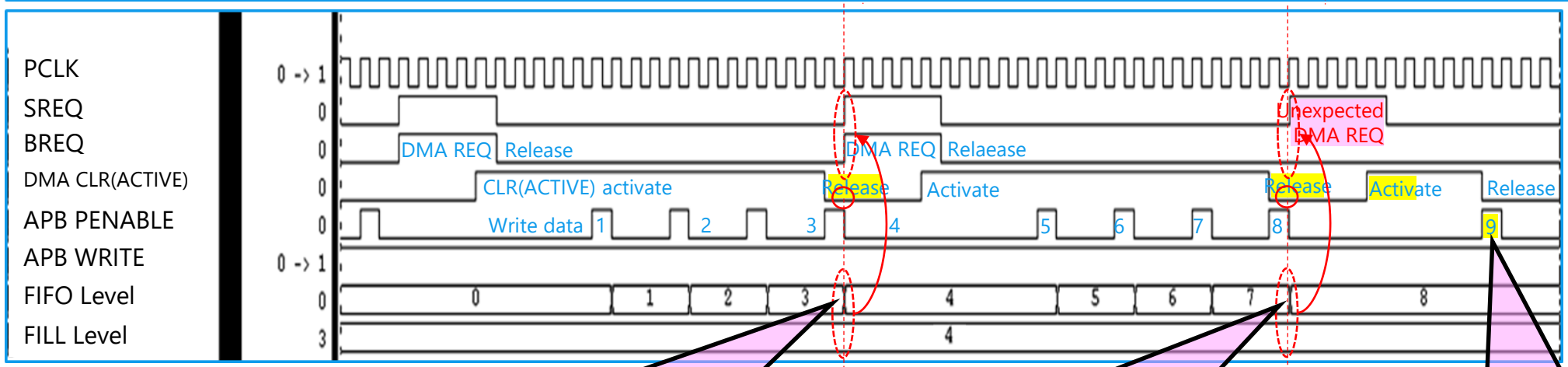
Problem (waveform)

[Problem] Unexpected DMA REQ is generated with a certain setting. The data sent by this REQ are discarded when the FIFO of TSPI is full.

Expected Operation



Unexpected Operation



BREQ is sent as FIFO level 4 when release cycle of DMACLR is correct.

DMA REQ is NOT sent because of FIFO level8(Full) when release cycle of DMACLR is correct.

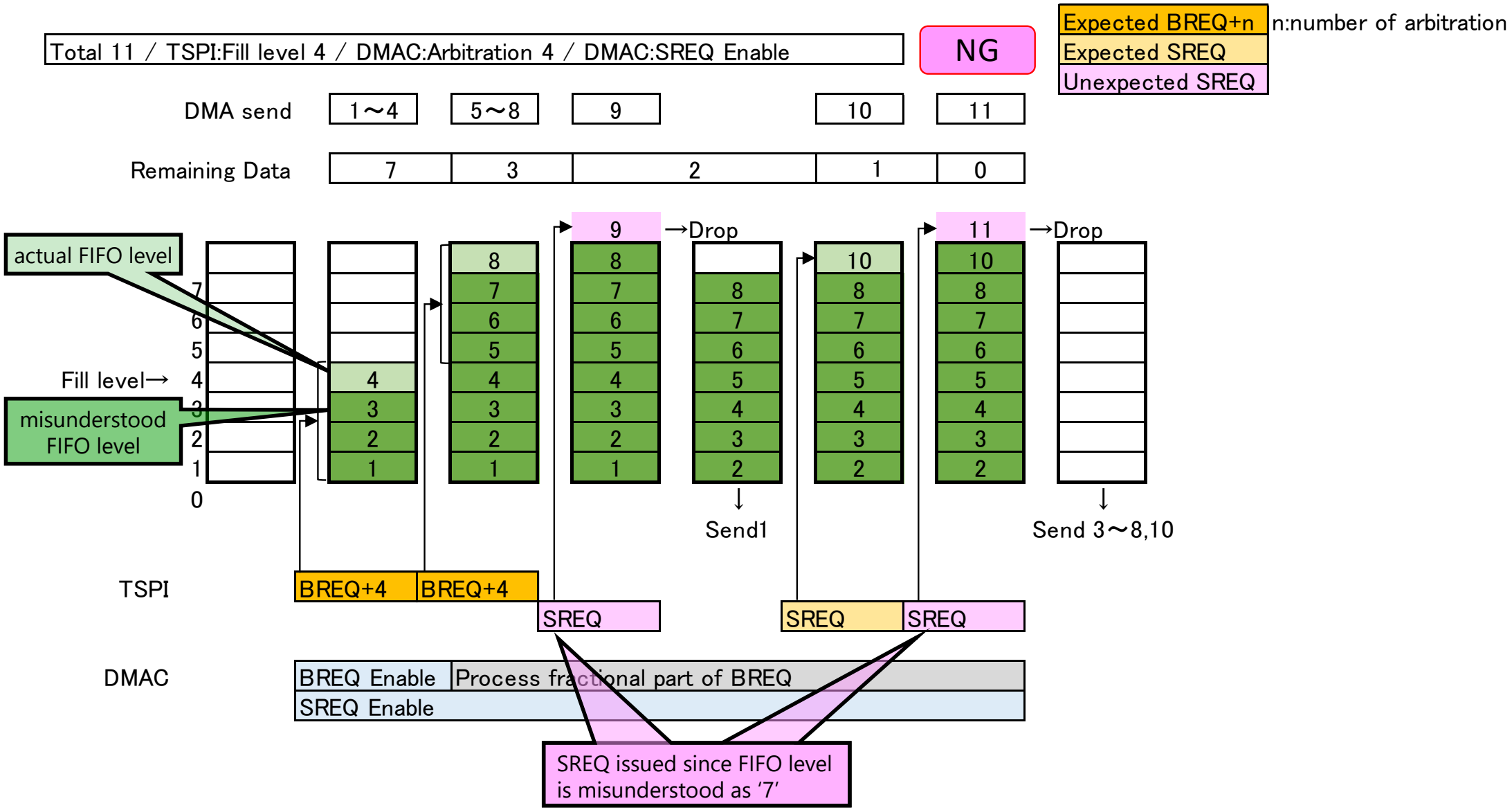
BREQ is sent as FIFO level3 because release cycle of DMACLR is early. It is NOT a problem because FIFO has still empty.

SREQ is sent as FIFO level 7 because release cycle of DMACLR is early. Then FIFO level changes to 8(Full) after finishing data write.

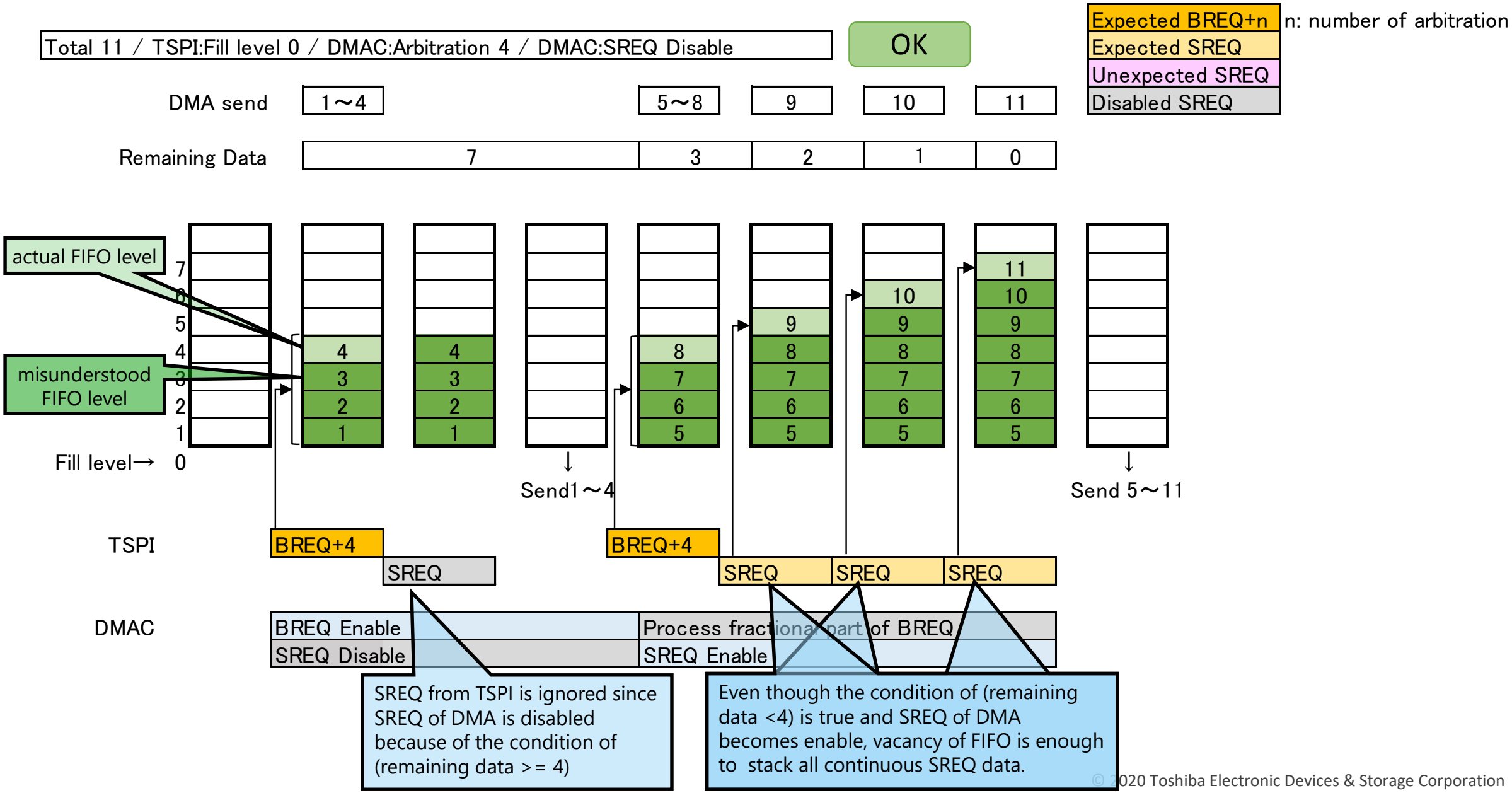
This data is discarded because of FIFO level 8.

Setting
TSPI TX (FIFO : 8 stages)
Fill Level : 4
(BREQ is send with less than FIFO level 4)
Arbitration : 4

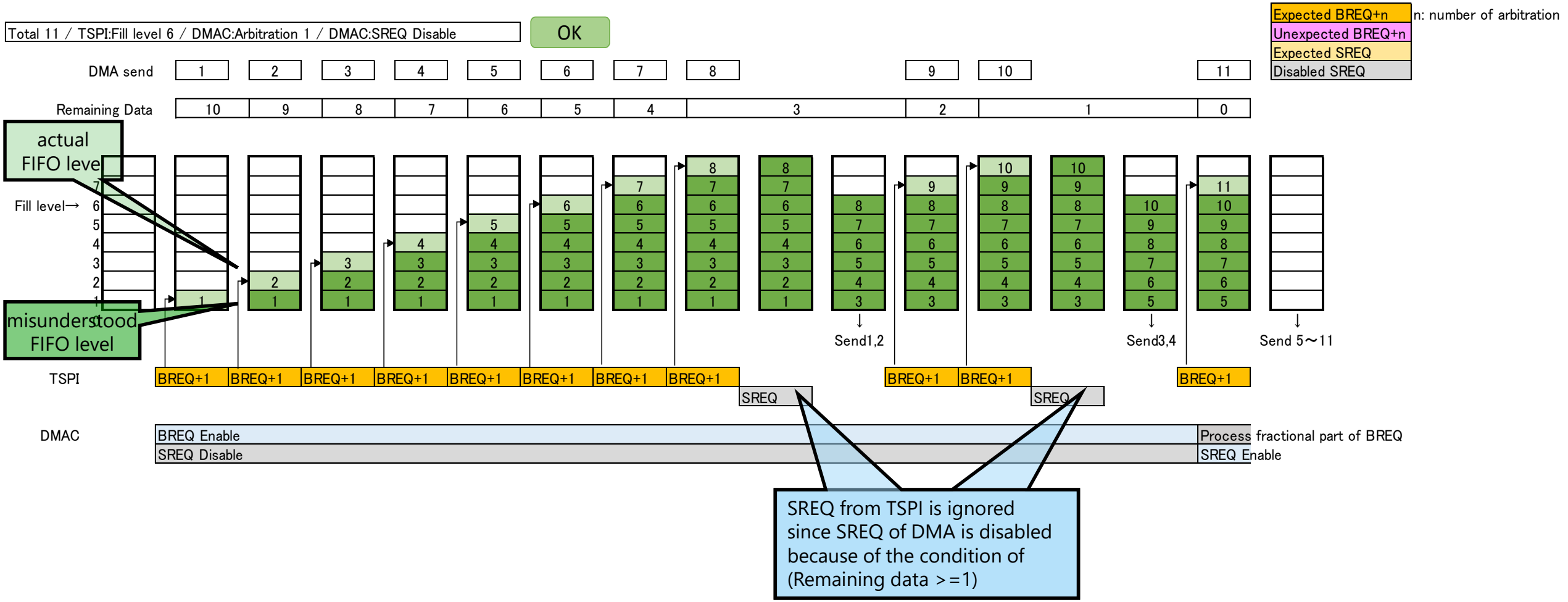
Problematic behavior (FIFO)



Workaround 1 :　SREQ Disable / Arbitration 4 / Fill level 0



Workaround 2: SREQ Disable / Arbitration 1 / Fill level 6



Content to be added in the Reference Manual

Regarding the Product Information in the Reference Manual, the items on the right will be added.

Example of TMPM3H group(2)

M3H group(1) : 2.17.6.1
M3H group(2) : 2.18.5.1
M4K group(1) : 2.6.7.1
M4K group(2) : 2.17.5.1

2.18.5.1 Notice when performing TSPI transmission using DMA

When performing TSPI transmission using the DMAC, set the DMAC and TSPI to (1) or (2) below.

(1) Set arbitration of DMAC to once

DMAC：

・Write "0000" to the Transfer mode setup(DMAChnlCfg)<R_power> in the Channel control data to set arbitration to 1.

・Write "1" to the bit of the corresponding of the *[DMAxChnlUseburstSet]* to disable the single transfer request operation.

TSPI：

・ set *[TSPIxCR2]*<TIL[3:0]> as below

7-16bit: set the Fill level less or equal 6

17-32bit: set the Fill level less or equal 2

(2) Set arbitration of DMAC to more than once

DMAC：

・ Write "0001"(twice) or "0010"(4 times) to the Transfer mode setup(DMAChnlCfg)<R_power> in the Channel control data.

・ Write "1" to the bit of the corresponding channel of the *[DMAxChnlUseburstSet]* to disable the single transfer request operation.

TSPI：

・ set *[TSPIxCR2]*<TIL[3:0]> as below

Fill ≦ FillMax − (arbitration × 2 − 1)

7-16bit: FillMax = 7

17-32bit: FillMax = 3

List of the products

M3H group (1)

TMPM3H6FSFG, TMPM3H6FUFG, TMPM3H6FWFG, TMPM3H5FSFG, TMPM3H5FUFG, TMPM3H5FWFG, TMPM3H4FSUG, TMPM3H4FUUG, TMPM3H4FWUG, TMPM3H2FSDUG, TMPM3H2FUDUG, TMPM3H2FUQG, TMPM3H2FWDUG, TMPM3H2FWQG

M3H group (2)

TMPM3HQFDFG, TMPM3HQFYFG, TMPM3HQFZFG, TMPM3HPFDFG, TMPM3HPFYFG, TMPM3HPFZFG,TMPM3HNFDDFG, TMPM3HNFDFG, TMPM3HNFYDFG, TMPM3HNFYFG, TMPM3HNFZDFG, TMPM3HNFZFG, TMPM3HMFDFG, TMPM3HMFYFG, TMPM3HMFZFG, TMPM3HLFDUG, TMPM3HLFYUG, TMPM3HLFZUG, TMPM3H2FSQG,

M4K group(1)

TMPM4K4FSAFG, TMPM4K4FSAUG, TMPM4K4FUAFG, TMPM4K4FUAUG, TMPM4K4FWAFG, TMPM4K4FWAUG, TMPM4K4FYAFG, TMPM4K4FYAUG, TMPM4K2FSADUG, TMPM4K2FUADUG, TMPM4K2FWADUG, TMPM4K2FYADUG,TMPM4K1FSAUG, TMPM4K1FUAUG, TMPM4K1FWAUG, TMPM4K1FYAUG, TMPM4K0FSADUG

M4K group (2)

TMPM4KQFDFG, TMPM4KQFWFG, TMPM4KQFYFG, TMPM4KPFDDFG, TMPM4KPFWDFG, TMPM4KPFYDFG, TMPM4KNFDDFG, TMPM4KNFDFG, TMPM4KNFWDFG, TMPM4KNFWFG, TMPM4KNFYDFG, TMPM4KNFYFG, TMPM4KMFDDFG, TMPM4KMFDFG, TMPM4KMFWDFG, TMPM4KMFWFG, TMPM4KMFYDFG, TMPM4KMFYFG, TMPM4KLFDFG, TMPM4KLFDUG, TMPM4KLFWFG, TMPM4KLFWUG, TMPM4KLFYFG, TMPM4KLFYUG

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To: Distributors

Product defect related to Serial Periferal Interface (TSPI) utilize DMA Controler (DMAC)

TOSHIBA

2020/May/28

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	Single-transfer is disabled	DMAC can ignore SERQ when burst transfer is possible by single-transfer is disable. However, if the remaining transfer count is a fraction less than the burst transfer count, single transfer is automatically enabled.
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Conditions/phenomena and product

【 Applicable products 】

TMPM066FWUG

【 Configuration that occur 】

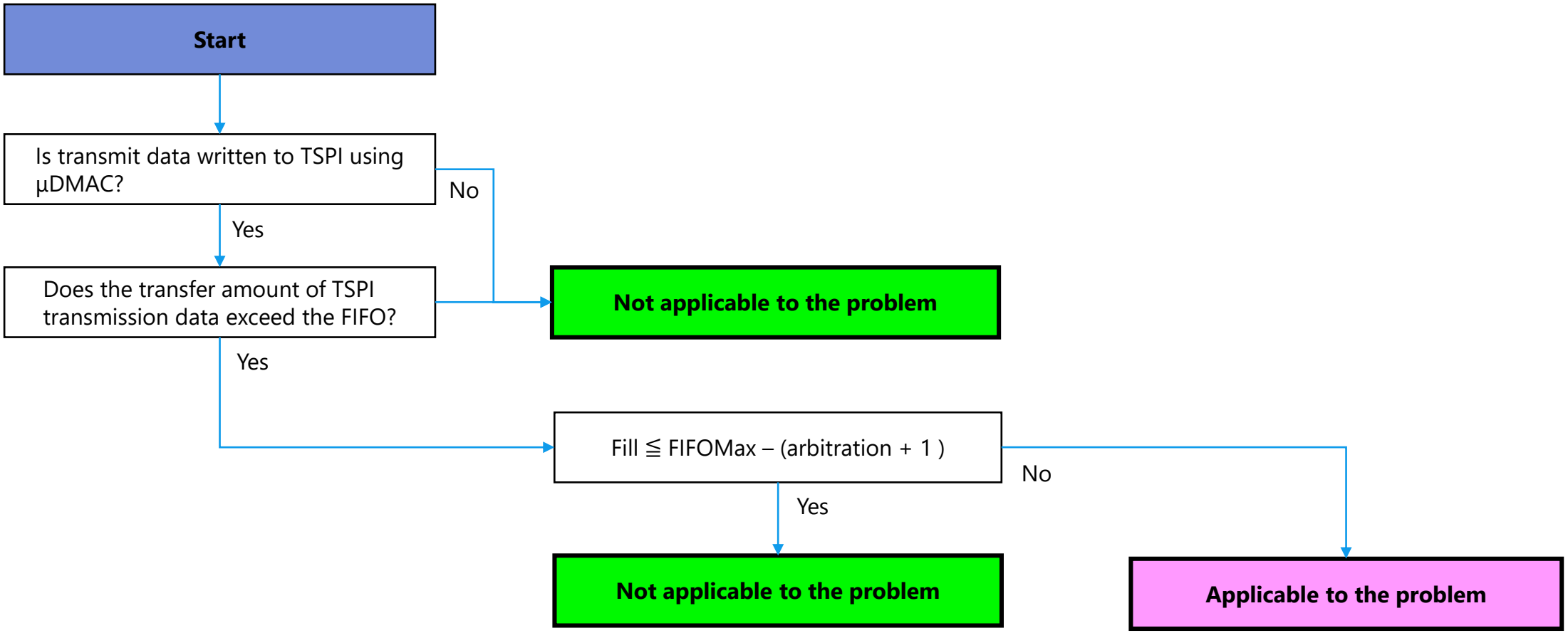
Combination of µDMAC + APBIF + TSPI

【 Phenomenon 】

When transmitting data to TSPI using the DMAC, FIFO control may not be performed correctly depends on the DMAC and TSPI setting conditions, and the data transferred by the DMAC to the TSPI may be discarded.

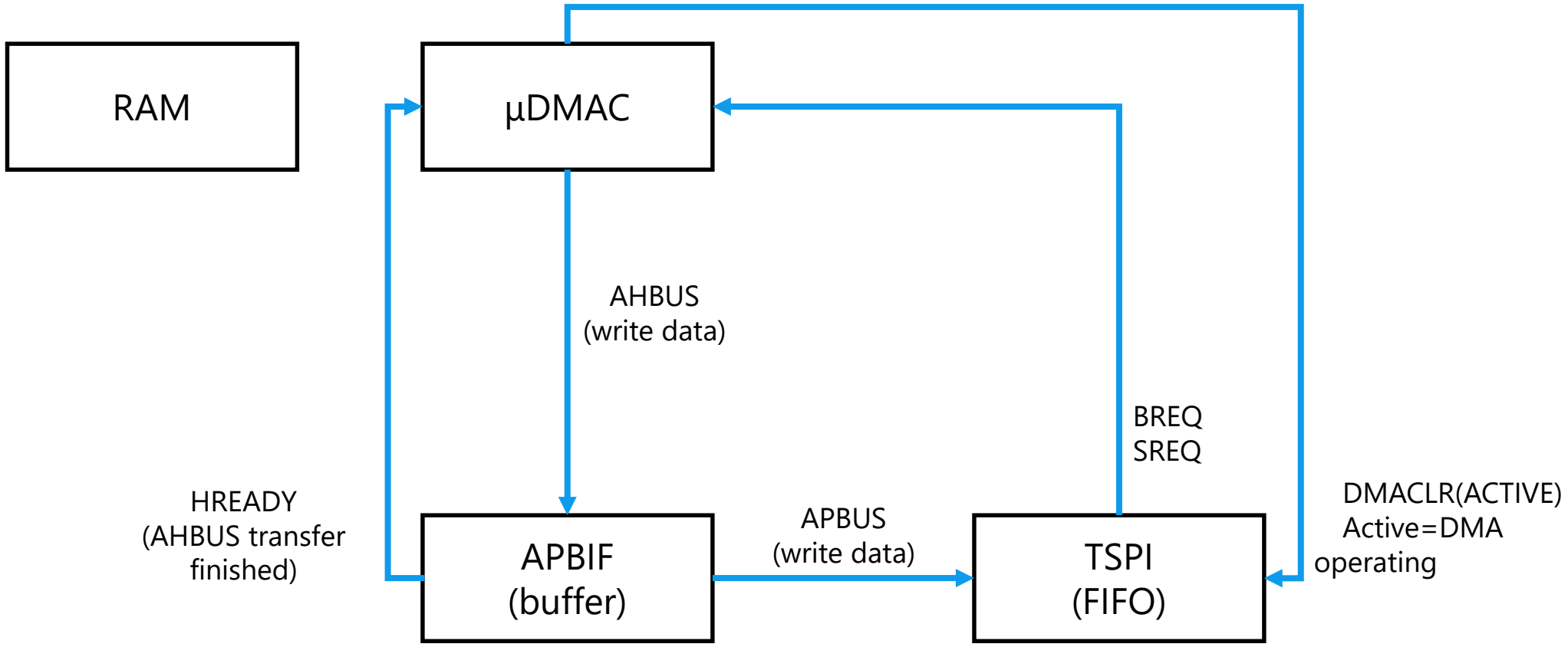
The following page shows the check flow of the occurrence conditions.

DMAC+TSPI チェック



Block diagram µDMAC+APBIF+TSPI

Related block diagram



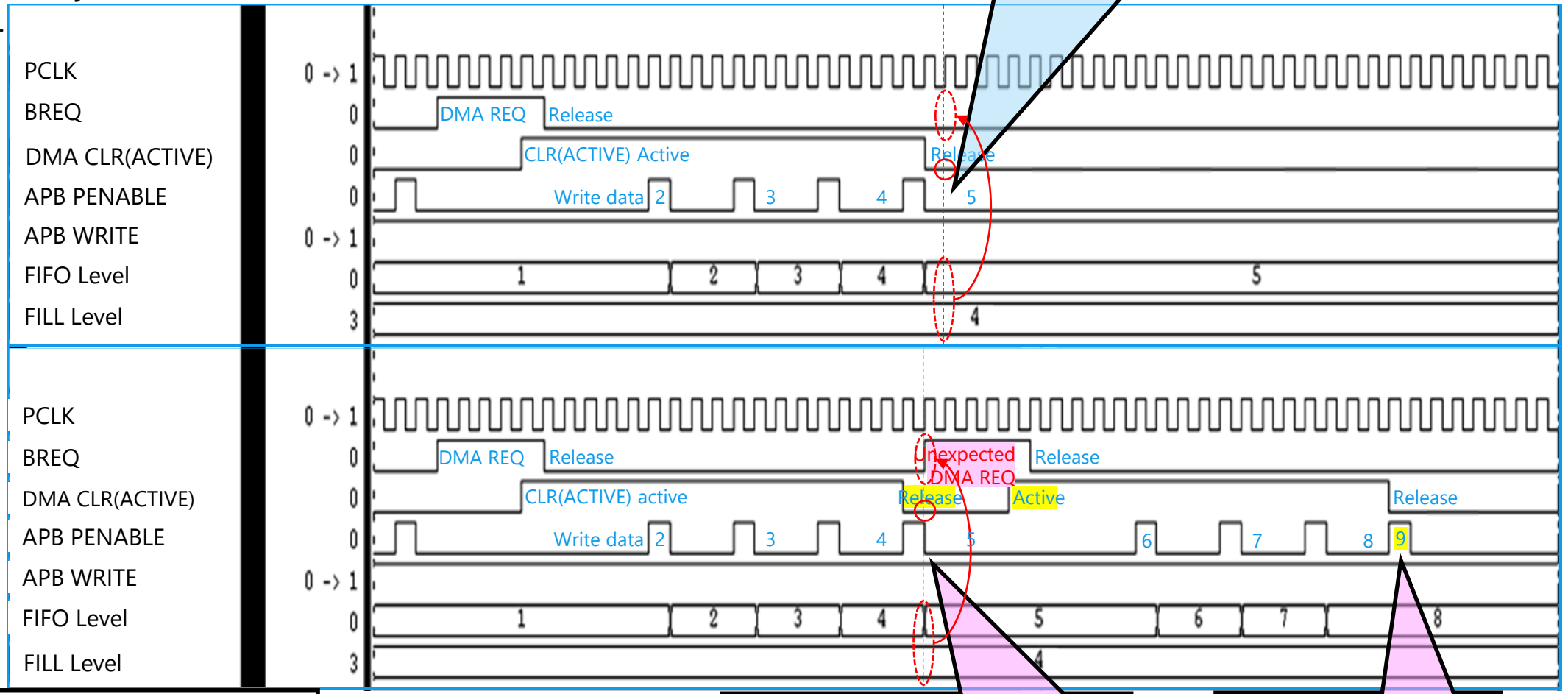
The problem will be described to next slide.

Problem (waveform)

[Problem] Unexpected DMA REQ is generated with a certain setting. The data sent by this REQ are discarded when the FIFO of TSPI is full.

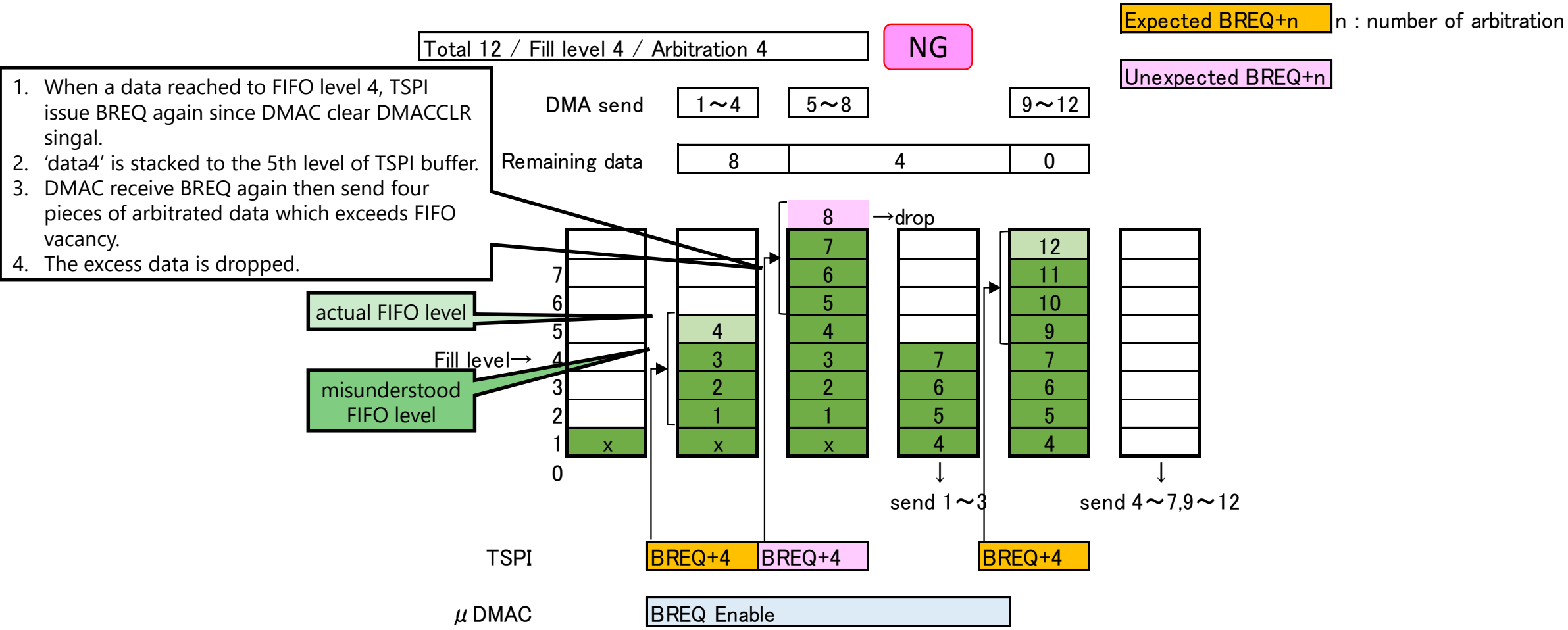
Expected Operation

Unexpected Operation

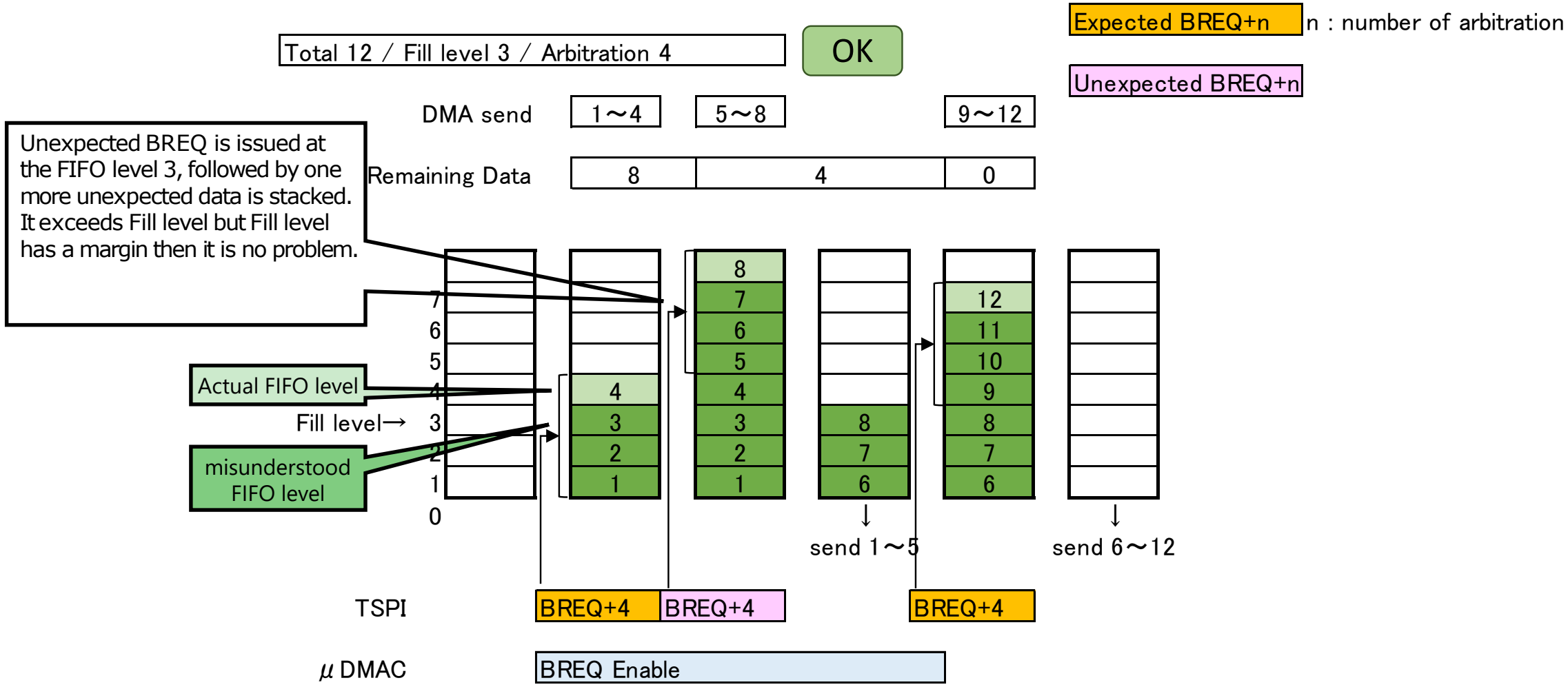


Setting
TSPI TX (FIFO : 8 stages)
Fill Level : 4
(BREQ is send with less than FIFO level 4)
Arbitration : 4

Problematic behavior (FIFO)



Workaround:　case of Fill ≦ FIFOMax – (arbitration + 1)



Content to be added in the Reference Manual

The below will be added to the Reference Manual.

2.1.7.1 Notice when performing TSPI transmission using µDMAC

When performing TSPI transmission using the DMAC, set the DMAC and TSPI as below.

µDMAC:

・Write to the Transfer mode setup(DMAChnlCfg)<R_power> in the Channel control data to set arbitration.

<R_power> = "0000"、"0001"、or "0010"
Arbitration = once, twice, or four times

TSPI :

・set <TIL[3:0]> of [TSPIxCR2]register as below.

Fill ≦ FIFOMax − (arbitration + 1）

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