TMD3702VC

Narrow ALS, Color and Proximity Sensor Module

General Description

The TMD3702VC features proximity detection, color sense (RGBC+IR), and digital ambient light sensing (ALS). The extremely narrow 1.44mm module incorporates an IR VCSEL and factory calibrated VCSEL driver. The proximity detection feature provides object detection (e.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated VCSEL). Detect/release events are interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction. The color photodiodes have UV and IR blocking filters and dedicated data converters producing 16-bit data. This architecture allows applications to accurately measure ambient light which enables devices to calculate illuminance and color temperature to control display backlight and chromaticity.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD3702VC, Narrow ALS, Color and Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMD3702VC

Benefits	Features
• Single device integrated optical solution	• ALS + color + proximity • 1.44mm x 2.84mm x 0.65mm module • ±48° field of view • Integrated 940nm IR VCSEL • Power management features • I^2C fast mode interface compatible
• Accurate ambient light sensing	• 5 channels (RGBC + IR) • UV / IR blocking filters • Programmable gain and integration time
• Reduced power consumption	• 1.8V power supply with 1.8V I^2C bus • Sleep mode

Applications

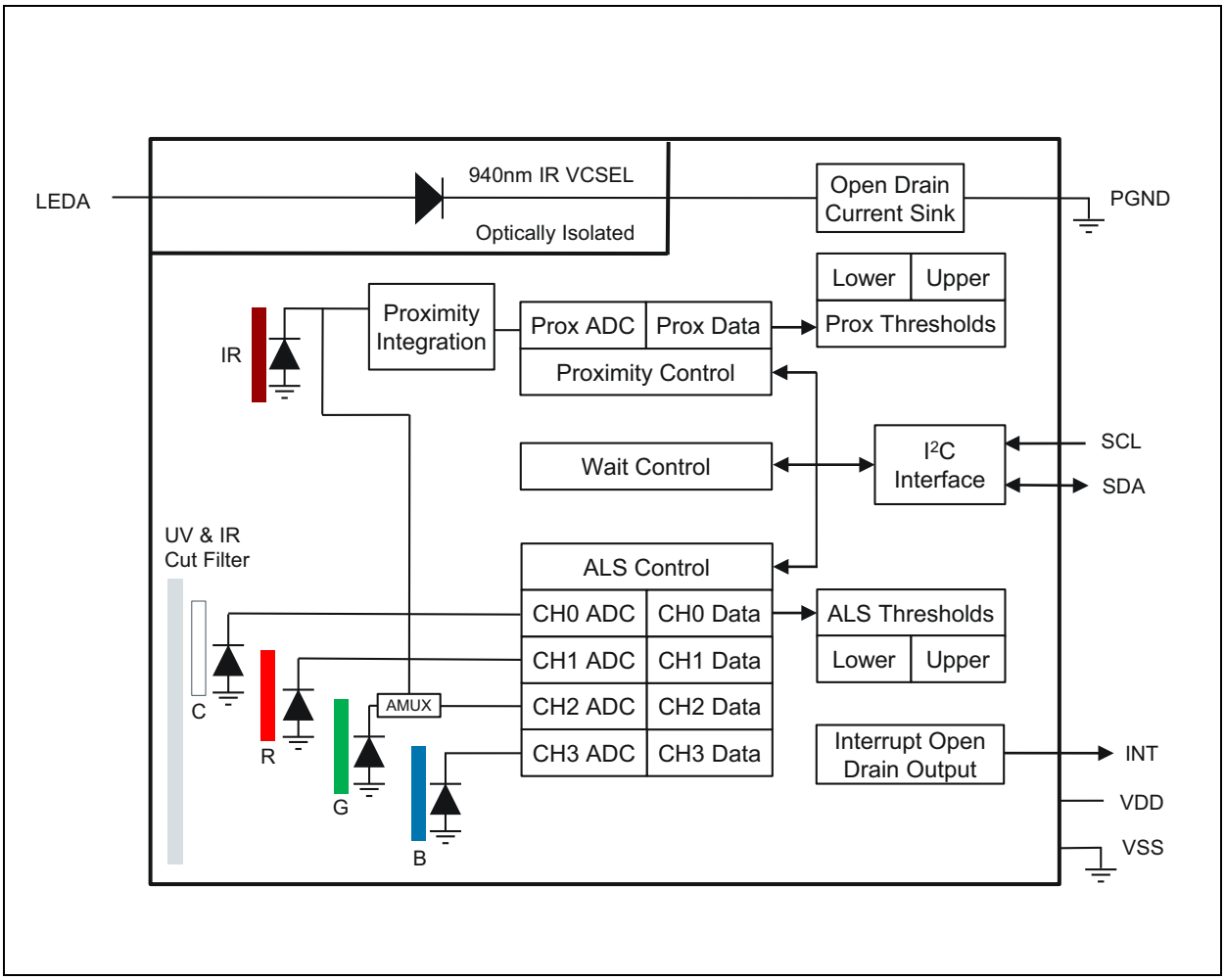
The TMD3702VC applications include:

- Ambient light sensing
- Proximity sensing
- Mobile phone touch screen disable
- Color temperature measurement to assist display, backlight, camera, and flash control

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
TMD3702VC Block Diagram



Pin Assignment

Figure 3:
Pin Diagram

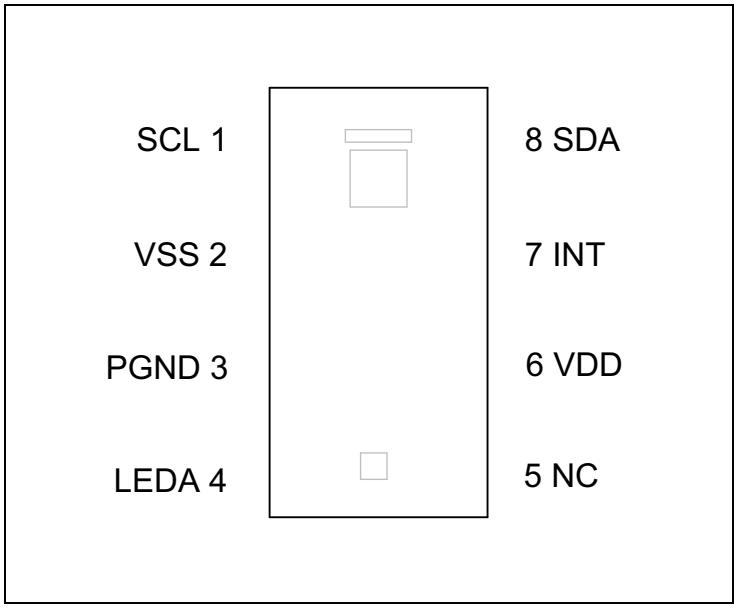


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	SCL	I^2C serial clock input terminal
2	VSS	Ground. All voltages are referenced to VSS/PGND and both pins must be connected to ground.
3	PGND	
4	LEDA	VCSEL anode
5	NC	No connect. No internal electrical connection. For improved device ESD protection, connect to ground.
6	VDD	Supply voltage (1.8V)
7	INT	Interrupt. Open drain output (active low)
8	SDA	I^2C serial data I/O terminal

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other condition beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
VDD	Supply Voltage to Ground	-0.3	2.0	V	
LEDA	VCSEL Voltage to PGND	-0.3	3.6	V	
V_{IO}	Digital I/O Terminal Voltage	-0.3	3.6	V	
I_{IO}	Digital Output Terminal Current	-1	20	mA	
I_{VCSEL}	VCSEL Current		30	mA	
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78D
ESD_{HBM}	HBM Electrostatic Discharge	± 2000		V	JS-001-2014
ESD_{CDM}	CDM Electrostatic Discharge	± 500		V	JEDEC JESD22-C101F
T_{STRG}	Storage Temperature Range	-40	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
P_{DISS}	Power Dissipation		200	mW	Average power dissipation over a 1 second period

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD	Supply Voltage	1.7	1.8	2.0	V
V_{LEDA}	Supply Voltage to VCSEL Anode (PLDRIVE = 19mA)	3.0	3.3	3.6	V
	Supply Voltage to VCSEL Anode (PLDRIVE = 14mA)	2.8	3.3	3.6	V
P_{DISS}	Average Power Dissipation(1)			100	mW
T_A	Operating Ambient Temperature	-30		85	°C

Note(s):

1. Power dissipation averaged over 1 second period.

Figure 7:
Operating Characteristics (V_{DD} = 1.8V, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator frequency			8.1		MHz
I_{DD}	Supply current (1)	Active ALS State (PON=AEN=1, PEN=0) (2)	50	105	150	µA
		Idle State (PON=1,AEN=PEN=0) (3)		35		
		Sleep State (4)		0.54		
V_{OL}	INT, SDA output low voltage	6mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA,SCL,INT		-5		5	µA
V_{IH}	SCL, SDA input high voltage (5)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR VCSEL.
2. This parameter indicates the supply current during periods of ALS integration. If Wait is enabled (WEN=1), the supply current is lower during the Wait period.
3. Idle state occurs when PON=1 and all functions are not enabled.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
5. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.0V.

Figure 8:
Optical Characteristics (V_{DD} = 1.8V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Re Irradiance responsivity Settings: AGAIN = 16x ATIME = 150ms	**Clear Channel**				
	λ_D = 465 nm LED, 53.8µW/cm^2		44.8		Count/ (µW/cm^2)
	λ_D = 530 nm LED, 43.9µW/cm^2		86.0		
	λ_D = 620 nm LED, 37.5µW/cm^2		104		
	Warm White LED, 45.6µW/cm^2		83.2		
	Warm White LED, 45.6µW/cm^2	3323	3792	4361	Counts
	IR Channel				
	λ_D = 940 nm LED, 21.1µW/cm^2		44.0		Count/ (µW/cm^2)

Figure 9:
Color/ALS Sensor Characteristics (V_{DD} = 1.8V, T_A = 25°C unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Integration time step size		2.68	2.78	2.90	ms
Dark ADC count value	Ee = 0µW/cm^2 AGAIN: 512x ATIME = 100ms	0	1	2	Counts(3)
Gain scaling, relative to 64x gain setting (1)	AGAIN = 1x	0.0145	0.016	0.0175	x
	AGAIN = 4x	0.060	0.064	0.068	
	AGAIN = 16x	0.240	0.255	0.270	
	AGAIN = 128x	1.8	2.0	2.2	
	AGAIN = 256x	3.6	4.0	4.4	
	AGAIN = 512x	7.0	7.7	8.4	
ADC noise (2)	AGAIN = 512x ATIME = 100ms		0.02		% (σ)

Note(s):

1. Test condition integration time = 27.8ms.
2. Representative result by characterization.
3. The typical value on 3-sigma distribution. An AGAIN setting of 16x correlates to a typically dark ADC count value less than or equal to 1.

Figure 10:
Proximity Optical Characteristics (V_{DD} = 1.8V, LEDA = 3.0V, T_A = 25°C, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Part to Part Variation[1]	Conditions: PGAIN = 2 (4x) PLDRIVE = 8 (19mA) PPULSE = 7 (8 pulses) PPULSE_LEN = 3 (32µs) d=23mm round target 30mm target distance	65	100	135	%
Response, Absolute	Basic proximity measurement [2] Conditions: PGAIN = 2 (4x), PLDRIVE = 8 (19mA) PPULSE = 7 (8 pulses) PPULSE_LEN = 3 (32µs) Target material: 90% reflective surface of Kodak gray card Target Size: 100mm x 100mm Target Distance: 100mm	250	312	374	Counts
Noise/Signal [3]	PGAIN = 2 (4x) PLDRIVE = 8 (19mA) PPULSE = 7 (8 pulses) PPULSE_LEN = 3 (32µs) d=23mm round target 30mm target distance			2	%

Note(s):

1. Production tested result is the average of 5 readings expressed relative to a calibrated response.
2. Representative result by characterization.
3. Production tested result is the average of 20 readings divided by the average response.

Typical Operating Characteristics

Figure 11:
ALS Average Angular Response to 2700K White LED (pin1[-90°] to pin4 [90°])

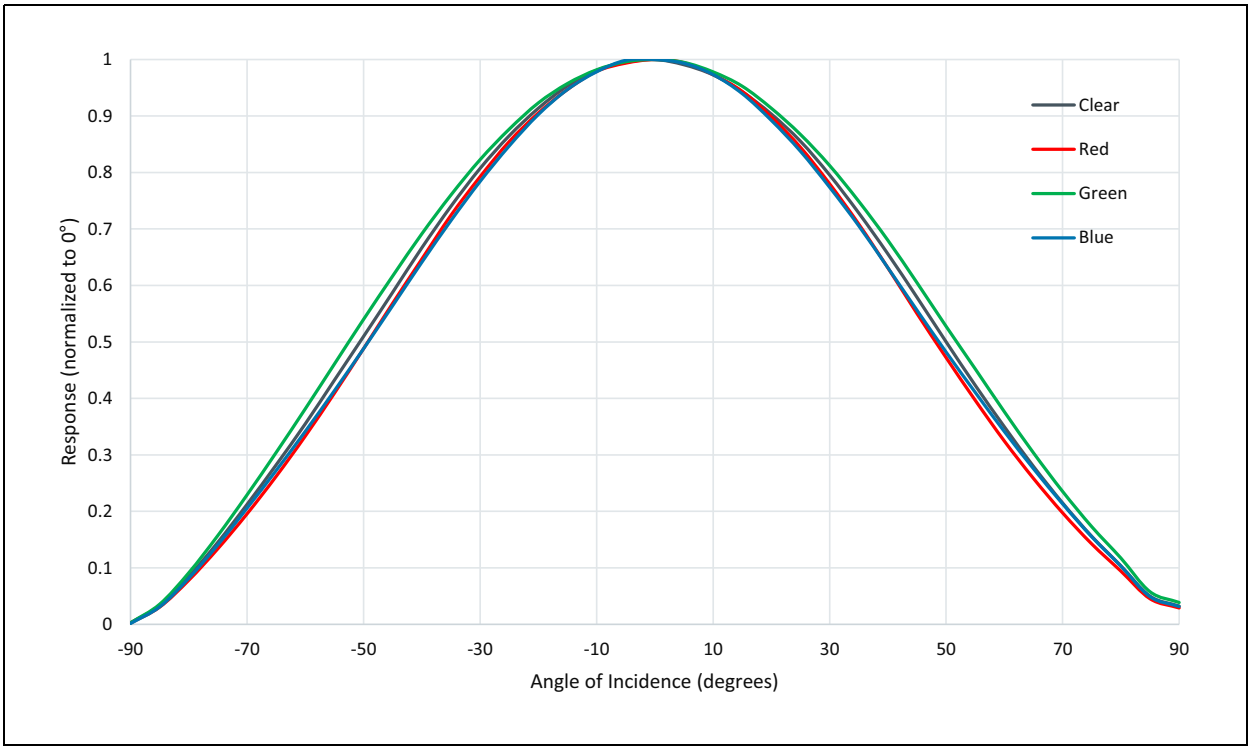


Figure 12:
ALS Average Angular Response to 2700K White LED (pin4 [-90°] to pin5 [90°])

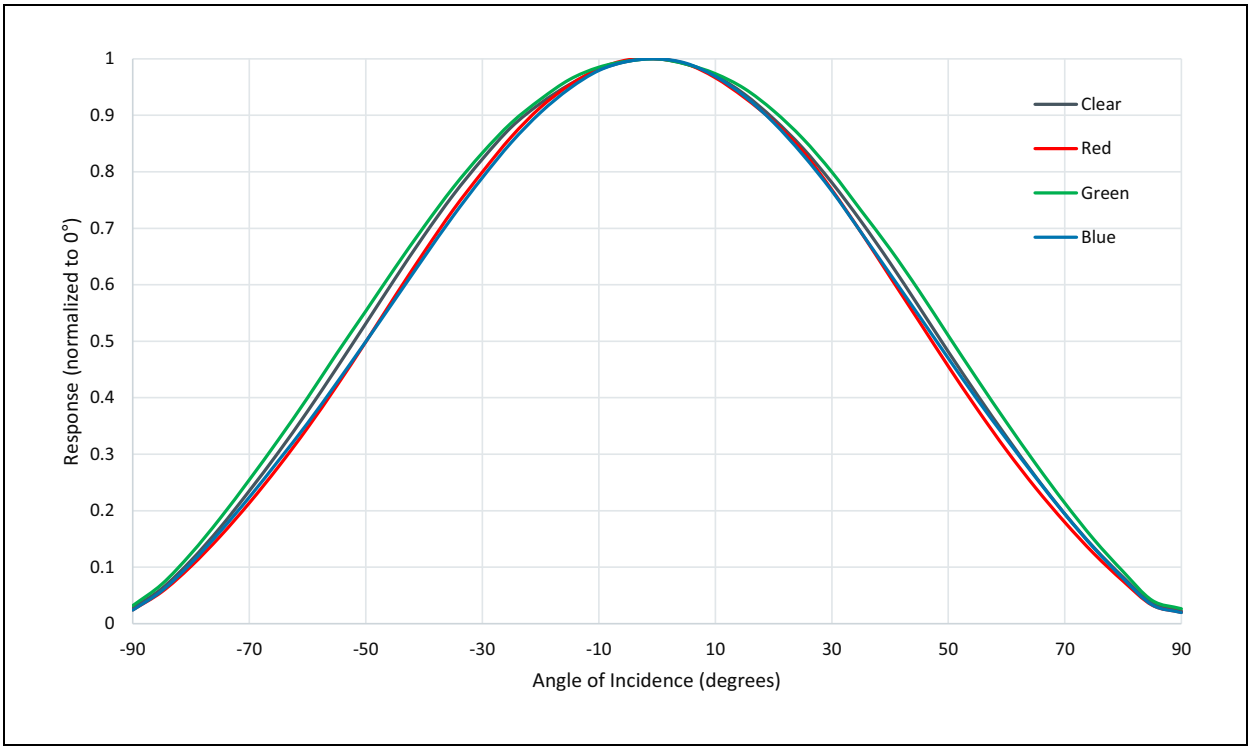


Figure 13:
Spectral Responsivity

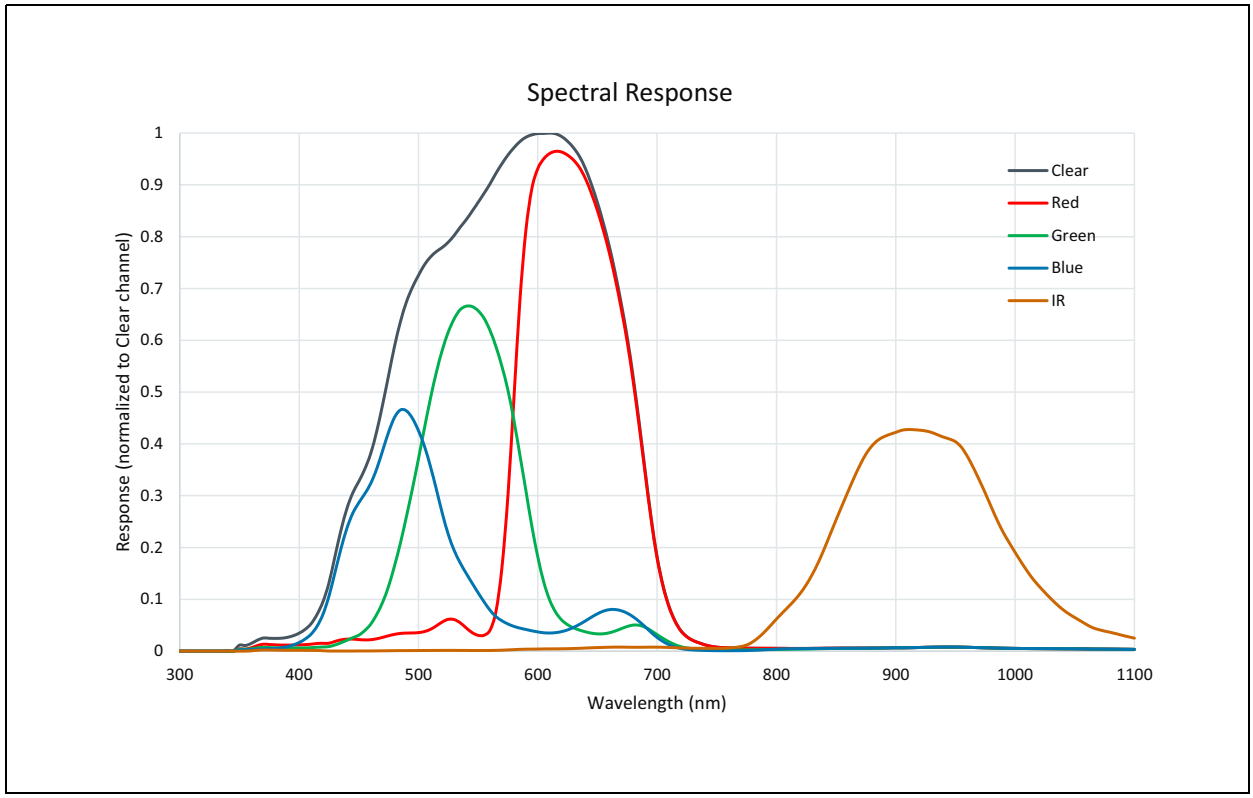


Figure 14:
Illuminance (Lux) vs Counts (Clear Channel)

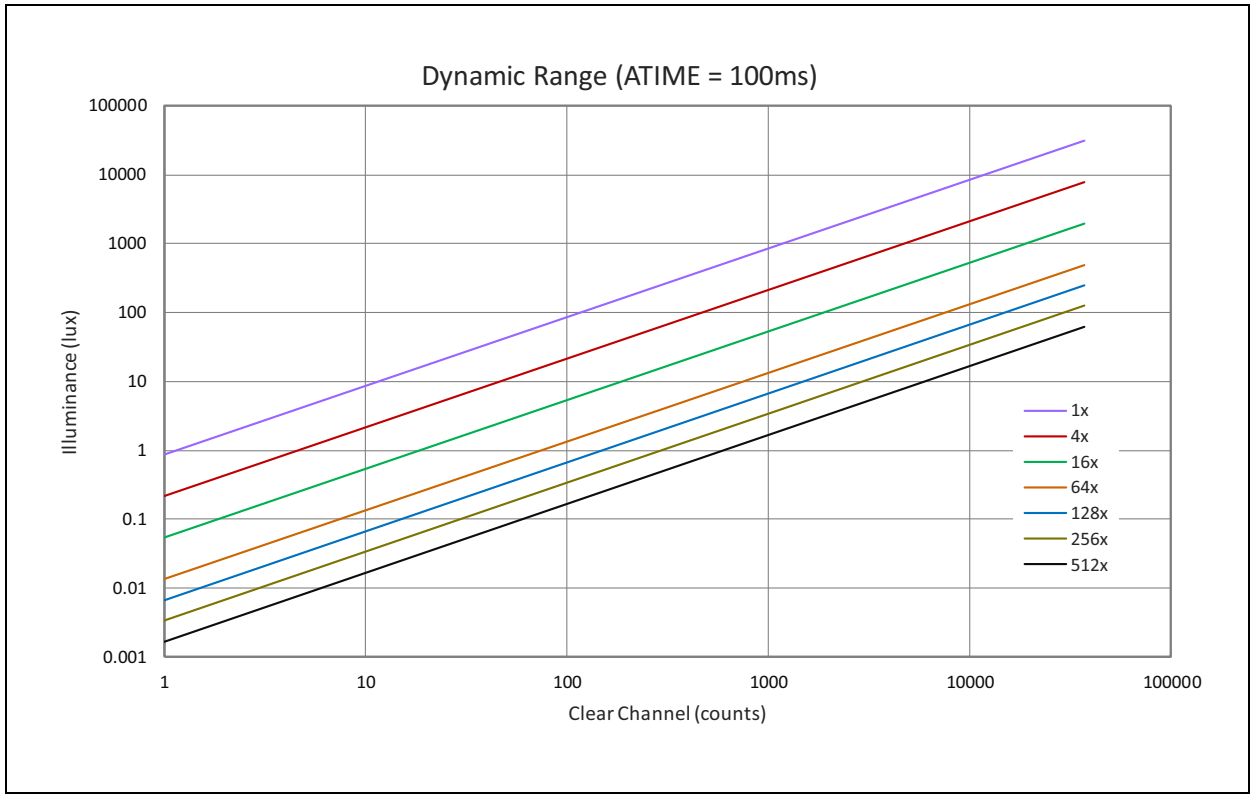


Figure 15:
Proximity Average Angular Response to 940nm IR LED (pin1[-90°] to pin4 [90°])

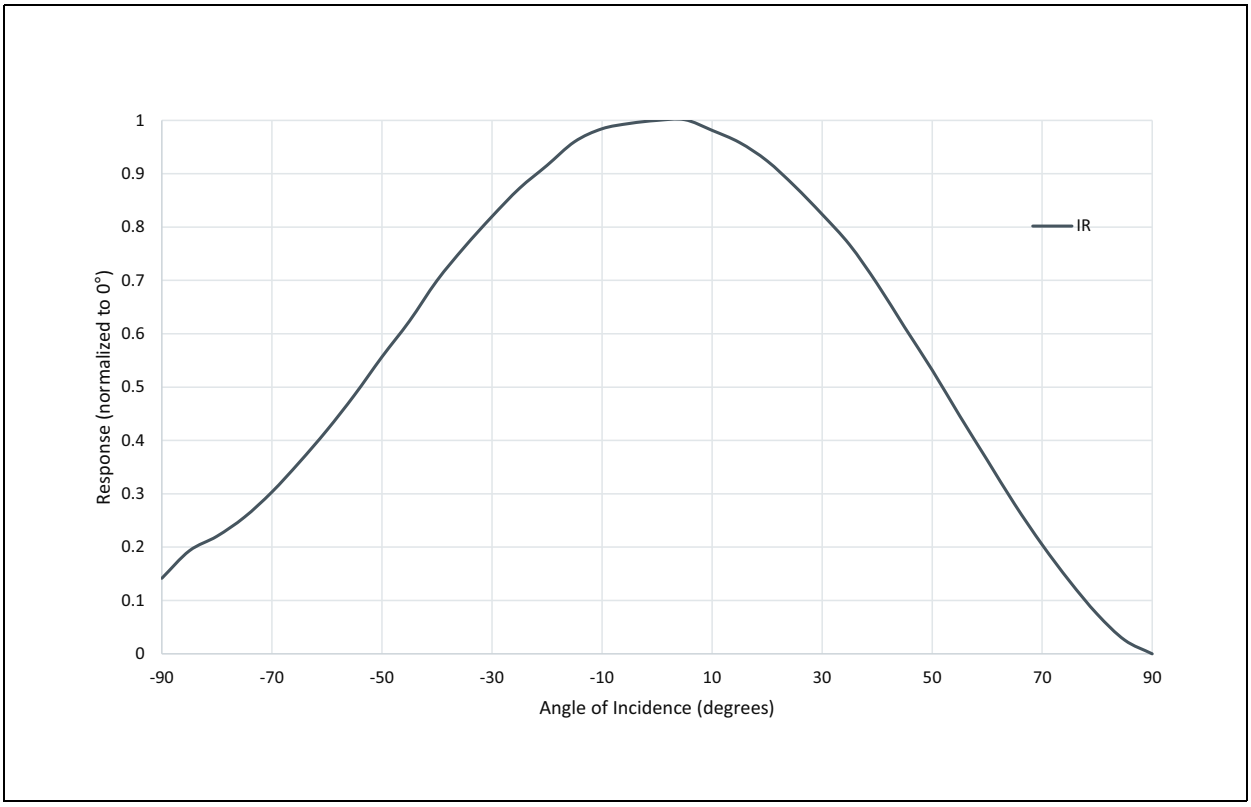


Figure 16:
Proximity Average Angular Response to 940nm IR LED (pin4 [-90°] to pin5 [90°])

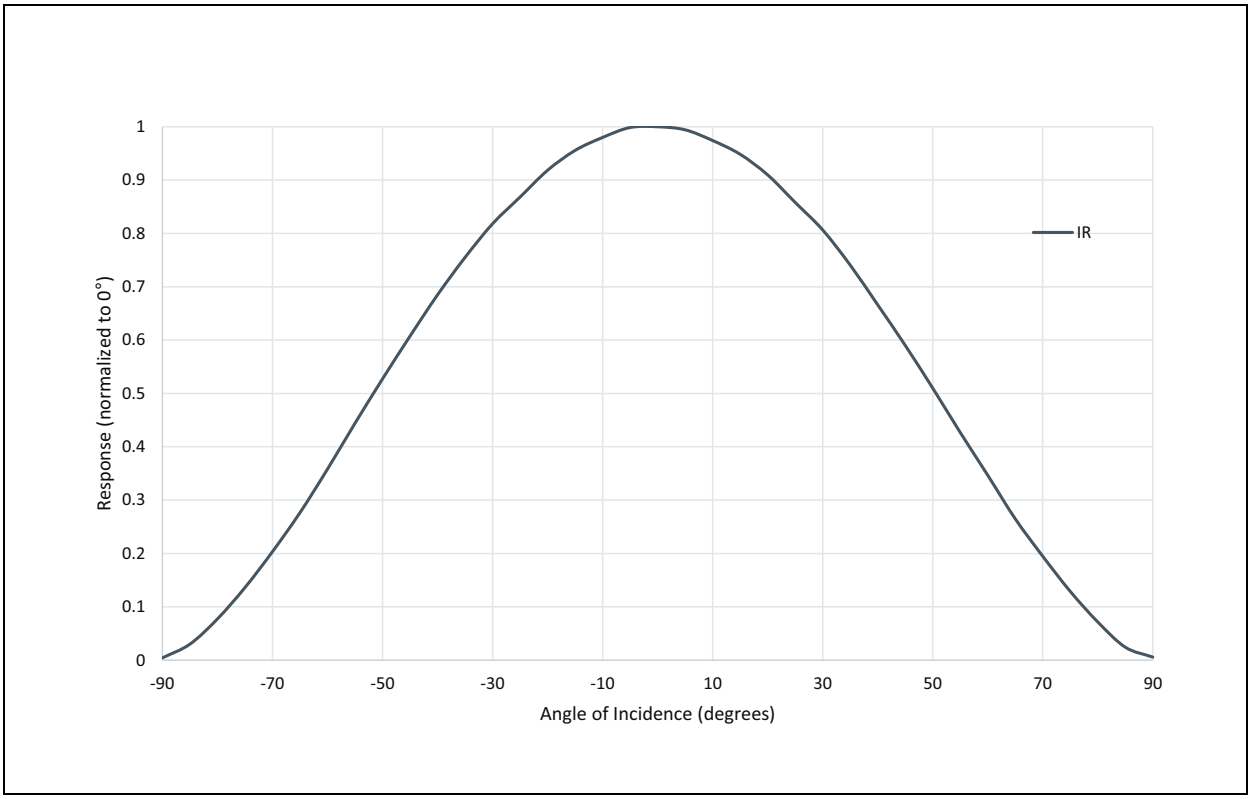
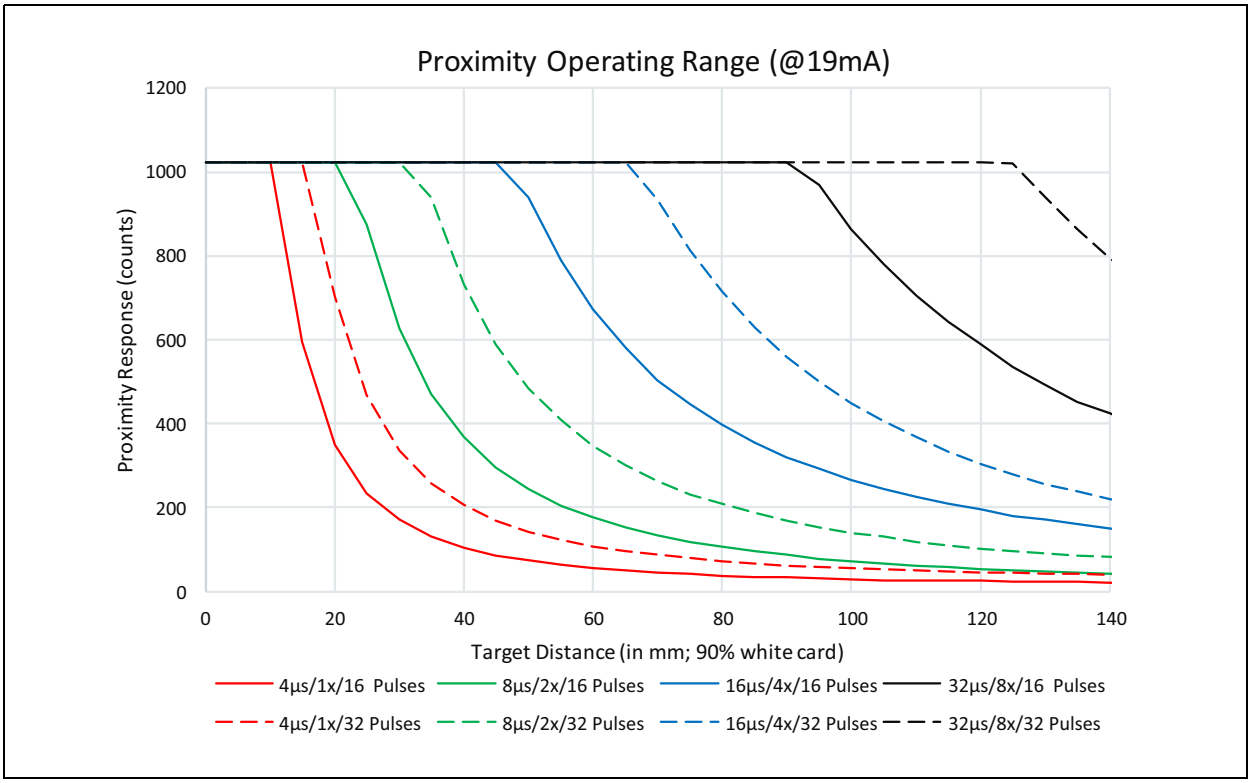


Figure 17:
Proximity Operation



Proximity Operation: By varying Gain, VCSEL drive current, number of VCSEL pulses and VCSEL pulse duration the proximity detection range can be adjusted.

Detailed Description

Proximity

Proximity results are affected by three fundamental factors: the integrated IR VCSEL emission, IR reception, and environmental factors, including target distance and surface reflectivity. The IR reception signal path begins with IR detection from a photodiode and ends with the 10-bit or 14-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Color and Ambient Light Sense

The color and ALS reception signal path begins as photodiodes receive filtered light and ends with 16-bit results. The IR photodiode primarily used for proximity sense, is multiplexed with the green channel's ADC to measure the IR content of ambient light. The color photodiodes are filtered with a UV and IR filters. The IR photodiode is filtered to receive only IR. Signal from the RGBC photodiodes simultaneously accumulate for a period of time set by the value in ATIME before the results are available. Measurement of IR must be done in a separate integration because it shares the ADC with the green photodiode. Gain is adjustable from 1x to 512x to facilitate operation over a wide range of lighting conditions. Based on the optical glass used on top of the device, custom equations are empirically derived to calculate the amount of ambient light, color temperature, as well as, determine the light type (e.g. LED, fluorescent, incandescent, etc.) using the ALS results.

I^2C Characteristics

The device uses I^2C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x49. Read and Write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I^2C bus is released). During consecutive Read transactions, the future/repeated I^2C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

I²C Write Transaction

A Write transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9th clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-ADDRESS$_{WRITE}$, REGISTER-ADDRESS, START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a Read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESS$_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:
www.i2c-bus.org/references/

Figure 18:
I²C Timing Diagrams

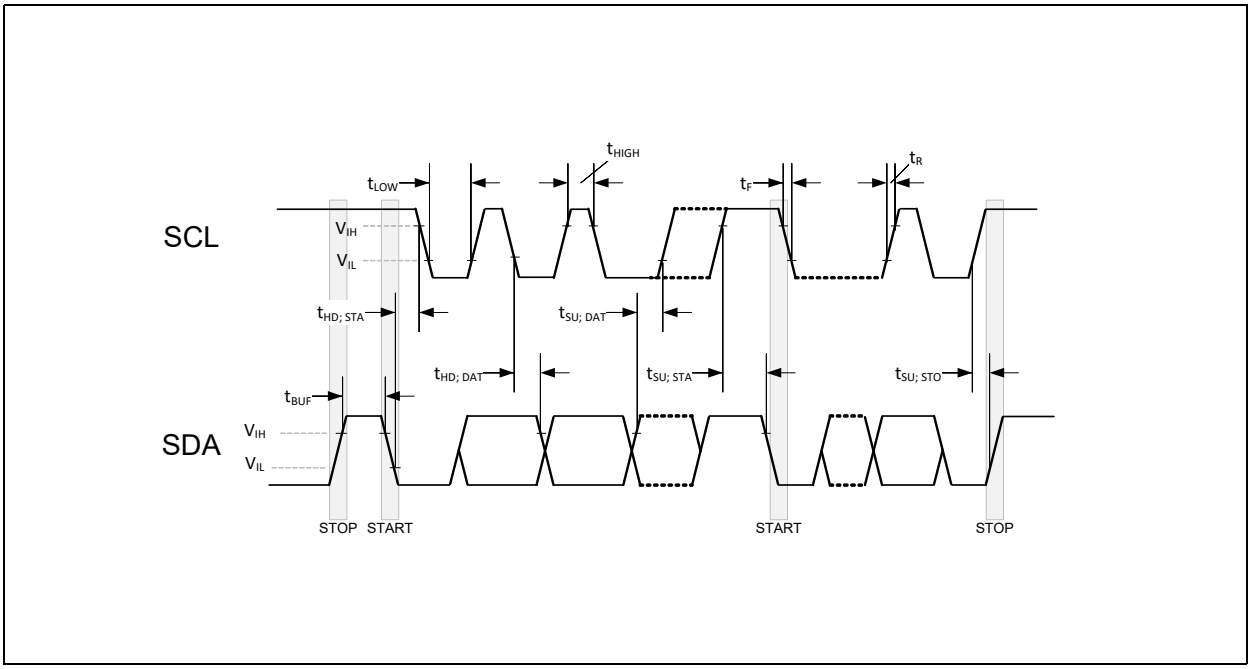
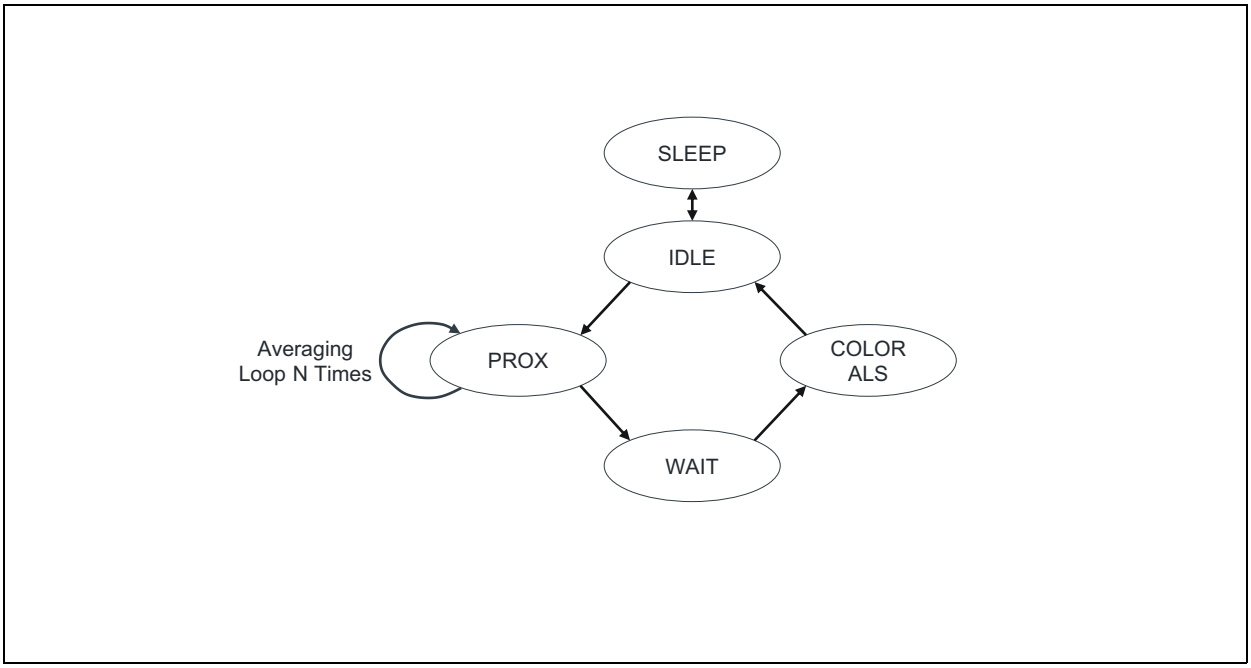


Figure 19:
Simplified State Diagram



Register Description

Figure 20:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states	0x00
0x81	ATIME	R/W	ADC integration time	0x00
0x82	PRATE	R/W	Proximity time	0x1F
0x83	WTIME	R/W	Wait time	0x00
0x84	AILTL	R/W	ALS interrupt low threshold low byte	0x00
0x85	AILTH	R/W	ALS interrupt low threshold high byte	0x00
0x86	AIHTL	R/W	ALS interrupt high threshold low byte	0x00
0x87	AIHTH	R/W	ALS interrupt high threshold high byte	0x00
0x88	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	R/W	ALS and proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x40
0x8E	PCFG0	R/W	Proximity configuration zero	0x4F
0x8F	PCFG1	R/W	Proximity configuration one	0x80
0x90	CFG1	R/W	Configuration one	0x09
0x91	REVID	R	Revision ID	0x01
0x92	ID	R	Device ID	0x10
0x93	STATUS	R, SC	Device status	0x00
0x94	CDATAL	R	Clear ADC low data	0x00
0x95	CDATAH	R	Clear ADC high data	0x00
0x96	RDATAL	R	Red ADC low data	0x00
0x97	RDATAH	R	Red ADC high data	0x00
0x98	GDATAL	R	Green (or IR) ADC low data	0x00
0x99	GDATAH	R	Green (or IR) ADC high data	0x00
0x9A	BDATAL	R	Blue ADC low data	0x00

Address	Register Name	R/W	Register Function	Reset Value
0x9B	BDATAH	R	Blue ADC high data	0x00
0x9C	PDATAL	R	Proximity ADC low data	0x00
0x9D	PDATAH	R	Proximity ADC high data	0x00
0x9E	REVID2	R	Revision ID two	0x07
0x9F	CFG2	R/W	Configuration two	0x00
0xA0	SOFTRST	R/W	Soft reset	0x00
0xAB	CFG3	R/W	Configuration three	0x04
0xAC	CFG4	R/W	Configuration four (must be set to 0x3D)	0x3F
0xAE	CFG6	R/W	Configuration six	0x3F
0xC0	POFFSETL	R/W	Proximity offset low data	0x00
0xC1	POFFSETH	R/W	Proximity offset high data	0x00
0xD7	CALIB	R/W	Proximity offset calibration	0x00
0xD9	CALIBCFG	R/W	Proximity offset calibration control	0x50
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00
0xDD	INTENAB	R/W	Interrupt enables	0x00
0xE6	FAC_L	R	Factory data low (lot code data)	0x00 to 0xFF
0xE7	FAC_H	R	Factory data high (lot code data)	0x00 to 0xFF
0xF2	TEST3	R/W	Test three (must be set to 0xC4)	0x44

Enable Register (Address 0x80)

Figure 21:
Enable Register

Addr:0x80		Enable		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0	RW	Reserved. Must be set to default value.
3	WEN	0	RW	This bit activates the wait feature. Active high.
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	AEN	0	RW	This bit actives the ALS function. Active high.
0	PON	0	RW	This field activates the internal oscillator and ADC channels. Active high.

Before activating AEN or PEN, preset each applicable operating mode registers and bits.

ATIME Register (Address 0x81)

Figure 22:
ATIME Register

Addr:0x81		ATIME					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7:0	ATIME	0x00	RW	ALS/Color value that specifies the integration time in 2.78ms intervals. 0x00 indicates 2.78ms. The maximum ALS value depends on the integration time. For every 2.78ms, the maximum value increases by 1024. This means that to be able to reach ALS full scale, the integration time has to be at least 64*2.78ms.			
				Value	**Integration Cycles**	**Integration Time**	**Maximum ALS Value**
				0x00	1	2.78ms	1023
				0x01	2	5.56ms	2047
				0x11	18	50.0ms	18431
				0x23	36	100ms	36863
				0x3F	64	178ms	65535
				0xFF	256	712ms	65535

The ATIME register controls the integration time of the ALS ADCs. The timer is implemented with a down counter with 0x00 as the terminal count. The timer is clocked at a 2.78ms nominal rate. Loading 0x00 will generate a 2.78ms integration time, loading 0x01 will generate a 5.56ms integration time, and so forth.

PRATE Register (Address 0x82)

Figure 23:
PRATE Register

Addr:0x82		PRATE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PRATE	0x1F	RW	This register defines the duration of 1 Prox Sample, which is (PRATE + 1)*88µs.

WTIME Register (Address 0x83)

Figure 24:
WTIME Register

<table>
<tr><th colspan="2">Addr:0x83</th><th colspan="3">WTIME</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td rowspan="8">7:0</td><td rowspan="8">WTIME</td><td rowspan="8">0x00</td><td rowspan="8">RW</td><td colspan="3">Value that specifies the wait time between ALS and proximity cycles in 2.78ms increments</td></tr>
<tr><td>Value</td><td>Increments</td><td>Wait Time</td></tr>
<tr><td>0x00</td><td>1</td><td>2.78ms (33.4ms)</td></tr>
<tr><td>0x01</td><td>2</td><td>5.56ms (66.7ms)</td></tr>
<tr><td>0x11</td><td>18</td><td>50.0ms (600ms)</td></tr>
<tr><td>0x23</td><td>36</td><td>100ms (1.20s)</td></tr>
<tr><td>0x3F</td><td>64</td><td>178ms (2.14s)</td></tr>
<tr><td>0xFF</td><td>256</td><td>712ms (8.54s)</td></tr>
</table>

The wait timer is implemented using a down counter.
Wait time = Increment x 2.78ms. If WLONG is enabled then,
Wait time = Increment x 2.78ms x 12.

AILTL Register (Address 0x84)

Figure 25:
AILTL Register

Addr:0x84		AILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTL	0x00	RW	This register sets the low byte of the LOW ALS threshold

AILTH Register (Address 0x85)

Figure 26:
AILTH Register

Addr: 0x85		AILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AILTH	0x00	RW	This register sets the high byte of the LOW ALS threshold

The Clear (C) channel is compared against low-going 16-bit threshold value set by AILTL and AILTH.

The contents of the AILTH and AILTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is below the AILTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.
When setting the 16-bit ALS threshold AILTL must be written first, immediately followed by AILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

AIHTL Register (Address 0x86)

Figure 27:
AIHTL Register

Addr: 0x86		AIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTL	0x00	RW	This register sets the low byte of the HIGH ALS threshold.

AIHTH Register (Address 0x87)

Figure 28:
AIHTH Register

Addr: 0x87		AIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	AIHTH	0x00	RW	This register sets the high byte of the HIGH ALS threshold.

The Clear (C) channel is compared against high-going 16-bit threshold value set by AIHTL and AIHTH.

The contents of the AIHTH and AIHTL registers are combined and treated as a sixteen bit threshold value. If the value generated by the C channel is above the AIHTL/H threshold and the APERS value is reached, the AINT bit is asserted. If AIEN is set, then the INT pin will also assert.

When setting the 16-bit ALS threshold AIHTL must be written first, immediately followed by AIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 16-bit value.

PILTL Register (Address 0x88)

Figure 29:
PILTL Register

Addr: 0x88		PILTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PILTL	0x00	RW	This register contains the low byte of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register contains the LOW threshold which is an 8-bit value which is compared against the upper 8-bits of the 10-bit proximity value.

PILTH Register (Address 0x89)

Figure 30:
PILTH Register

Addr: 0x89		PILTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PILTH	0x00	RW	This register contains the upper 6 bits of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PILTH and PILTL registers are combined and treated as a fourteen (14) bit threshold low value. If the value generated by the proximity ADC (PDATA) is below the PILTL/H threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert. When setting the 14-bit proximity threshold, PILTL must be written first, immediately follow by PILTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PILTL contains a 8-bit threshold which is compared against the upper 8-bits of the 10-bit value. PILTH is ignored.

PIHTL Register (Address 0x8A)

Figure 31:
PIHTL Register

Addr: 0x8A		PIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTL	0x00	RW	This register contains the low byte of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register contains the HIGH threshold which is an 8-bit value which is compared against the upper 8-bits of the 10-bit proximity value.

PIHTH Register (Address 0x8B)

Figure 32:
PIHTH Register

Addr: 0x8B		PIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PIHTH	0x00	RW	This register contains the upper 6 bits of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PIHTH and PIHTL registers are combined and treated as a fourteen (14) bit threshold high value. If the value generated by the proximity ADC (PDATA) is above the PIHTL/H threshold and the PPERS value is reached, the PINT bit is asserted. If PIEN is set, then the INT pin will also assert. When setting the 14-bit proximity threshold, PIHTL must be written first, immediately follow by PIHTH. Internally, the lower 8-bits are buffered until the upper 8-bits are written. As the upper 8-bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PIHTL contains a 8-bit threshold which is compared against the upper 8-bits of the 10-bit value. PIHTH is ignored.

PERS Register (Address 0x8C)

Figure 33:
PERS Register

Addr: 0x8C		PERS			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:4	PPERS	0 (0000)	RW	This register sets the proximity persistence filter.	
				Value	**Interrupt**
				0 (0000)	Every proximity cycle
				1 (0001)	Any value outside proximity thresholds
				2 (0010)	2 consecutive proximity values out of range
				3 (0011)	3 consecutive proximity values out of range
				…	….
				15 (1111)	15 consecutive proximity values out of range
3:0	APERS	0 (0000)	RW	This register sets the ALS persistence filter.	
				0 (0000)	Every ALS cycle
				1 (0001)	Any value outside ALS thresholds
				2 (0010)	2 consecutive ALS values out of range
				3 (0011)	3 consecutive ALS values out of range
				4 (0100)	5 consecutive ALS values out of range
				5 (0101)	10 consecutive ALS values out of range
				6 (0110)	15 consecutive ALS values out of range
				7 (0111)	20 consecutive ALS values out of range
				…	…
				13 (1101)	50 consecutive ALS values out of range
				14 (1110)	55 consecutive ALS values out of range
				15 (1111)	60 consecutive ALS values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.

The frequency of consecutive Clear (C) channel results outside of threshold limits are counted; this count value is compared against the APERS value. If the counter is equal to the APERS setting an interrupt is asserted. Any time a Clear (C) channel result is inside the threshold values the counter is cleared.

CFG0 Register (Address 0x8D)

Figure 34:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	01000	RW	Reserved. Must be set to default value.
2	WLONG	0	RW	When WLONG (Wait Long) is asserted the wait period as set by WTIME is increased by a factor of 12.
1	Reserved	0	RW	Reserved. Must be set to default value.
0	PPULSE_ LEN_16x	0	RW	When PPULSE_LEN_16X is asserted, the proximity pulse length is extended by a factor of 16. See the PPULSE_LEN bit description in the PCFG0 register.

PCFG0 Register (Address 0x8E)

Figure 35:
PCFG0 Register

<table>
<tr><th colspan="2">Addr: 0x8E</th><th colspan="4">PCFG0</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">PPULSE_LEN</td><td rowspan="6">1
(01)</td><td rowspan="6">RW</td><td colspan="2">Proximity pulse length. The pulse length can be extended by a factor of 16x with the assertion of the PPULSE_LEN_16x bit in CFG0.</td></tr>
<tr><td>Value</td><td>Pulse Length</td></tr>
<tr><td>0 (00)</td><td>4µs / 64µs</td></tr>
<tr><td>1 (01)</td><td>8µs / 128µs</td></tr>
<tr><td>2 (10)</td><td>16µs / 256µs</td></tr>
<tr><td>3 (11)</td><td>32µs / 512µs</td></tr>
</table>

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
5:0	PPLUSE	15 (001111)	RW	Maximum number of pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0 (000000)	1
				1 (000001)	2
				2 (000010)	3
				…	…
				63 (111111)	64

The PPULSE_LEN field sets the length (width) of all IR VCSEL pulses within the proximity cycle. Longer pulses result in increased proximity range and typically result in less electrical noise generated in the analog front end. If the PPULSE_LEN_16x bit in CFG0 is asserted, then the pulse length is extended by a factor of 16 times.

The PPULSE field sets the maximum number of IR VCSEL pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR VCSEL pulses, up to the value set in PPULSE or if a near-saturation condition occurs. The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets. This operation also reduces power consumption because proximity integration period is automatically shortened when a target is either too close or far from the sensor.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then PPULSE always determines the number of proximity to be transmitted.

PCFG1 Register (Address 0x8F)

Figure 36:
PCFG1 Register

<table>
<tr><th colspan="2">Addr: 0x8F</th><th colspan="3">PCFG1</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">PGAIN</td><td rowspan="6">2
(10)</td><td rowspan="6">RW</td><td colspan="2">This field sets the gain of the proximity IR sensor.</td></tr>
<tr><td>Value</td><td>Gain</td></tr>
<tr><td>0 (00)</td><td>1x</td></tr>
<tr><td>1 (01)</td><td>2x</td></tr>
<tr><td>2 (10)</td><td>4x</td></tr>
<tr><td>3 (11)</td><td>8x</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>00</td><td>RW</td><td colspan="2">Reserved. Must be set to default value.</td></tr>
<tr><td rowspan="12">3:0</td><td rowspan="12">PLDRIVE</td><td rowspan="12">0
(0000)</td><td rowspan="12">RW</td><td colspan="2">This field sets the drive strength of the IR VCSEL current. Values are approximate; actual current through VCSEL is factory trimmed to normalize IR intensity.
Note: Bit 5 in CFG1 must be set to a 1 or the VCSEL currents will be 2x the nominal values.</td></tr>
<tr><td>Value</td><td>VCSEL Current</td></tr>
<tr><td>0 (0000)</td><td>2mA</td></tr>
<tr><td>1 (0001)</td><td>4mA</td></tr>
<tr><td>2 (0010)</td><td>6mA</td></tr>
<tr><td>3 (0011)</td><td>8mA</td></tr>
<tr><td>4 (0100)</td><td>10mA</td></tr>
<tr><td>5 (0101)</td><td>12mA</td></tr>
<tr><td>6 (0110)</td><td>14mA</td></tr>
<tr><td>7 (0111)</td><td>17mA</td></tr>
<tr><td>8 (1000)</td><td>19mA</td></tr>
<tr><td>All other values</td><td>Reserved</td></tr>
</table>

CFG1 Register (Address 0x90)

Figure 37:
CFG1 Register

Addr: 0x90		CFG1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	IR_MUX	0	RW	If set high, the IR (proximity) photodiode is switched into the Green channel's data converter. GDATAL/H register will report IR content. Green photodiode is not connected in this mode. (1)
5	Reserved	0	RW	Reserved. **Must be set to 1.** If this bit is 0, the VCSEL current will be 2x the nominal value.
4:0	AGAIN	9 (01001)	RW	This field sets the gain of the ALS/Color sensor.

Value	ALS Gain
1 (00001)	1x
3 (00011)	4x
5 (00101)	16x
7 (00111)	64x
8 (01000)	128x
9 (01001)	256x
10 (01010)	512x
All other values	Reserved

Note(s):

1. The IR multiplexer is not synchronized to the ALS/Color measurement sequencer. It is recommended that after the IR_MUX bit is changed, to either discard the first ALS/color measurement or wait at least two ALS/color integration times before reading the results.

REVID Register (Address 0x91)

Figure 38:
REVID Register

Addr: 0x91		REVID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	00000	RO	Reserved.
2:0	REV_ID	001	RO	Device revision number.

ID Register (Address 0x92)

Figure 39:
ID Register

Addr: 0x92		ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	ID	000100	RO	Device type identification.
1:0	Reserved	00	RO	Reserved

Status Register (Address 0x93)

Figure 40:
Status Register

Addr: 0x93		Status Register		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASAT	0	R, SC	Analog saturation flag signals that the ALS/Color results may be unreliable due to saturation of the AFE.
6	PSAT	0	R, SC	Proximity saturation flag indicates that an ambient- or reflective-saturation event occurred during a previous proximity cycle.
5	PINT	0	R, SC	Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
4	AINT	0	R, SC	ALS interrupt flag indicates that ALS/Color results (clear channel) have exceeded thresholds and persistence settings.
3	CINT	0	R, SC	Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	R, SC	Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
1	PSAT_REFLECTIVE	0	R, SC	The reflective proximity saturation interrupt flag signals that the AFE has saturated during the IR VCSEL active portion of proximity integration.
0	PSAT_AMBIENT	0	R, SC	The ambient proximity saturation interrupt flag signals that the AFE has saturated during the IR VCSEL inactive portion of proximity integration.

All flags in this register can be cleared by setting the bit high. Alternatively, if the INT_READ_CLEAR in the CFG3 register bit is set, then simply reading this register automatically clears all eight flags.

CDATAL Register (Address 0x94)

Figure 41:
CDATAL Register

Addr: 0x94		CDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CDATAL	0x00	RO	This register contains the low byte of the 16-bit clear channel data.

CDATAH Register (Address 0x95)

Figure 42:
CDATAH Register

Addr: 0x95		CDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	CDATAH	0x00	RO	This register contains the high byte of the 16-bit clear channel data.

RDATAL Register (Address 0x96)

Figure 43:
RDATAL Register

Addr: 0x96		RDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RDATAL	0x00	RO	This register contains the low byte of the 16-bit red channel data.

RDATAH Register (Address 0x97)

Figure 44:
RDATAH Register

Addr: 0x97		RDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	RDATAH	0x00	RO	This register contains the high byte of the 16-bit red channel data.

GDATAL Register (Address 0x98)

Figure 45:
GDATAL Register

Addr: 0x98		GDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	GDATAL	0x00	RO	This register contains the low byte of the 16-bit green channel data (or IR data if IR_MUX bit in CFG1 = 1).

GDATAH Register (Address 0x99)

Figure 46:
GDATAH Register

Addr: 0x99		GDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	GDATAH	0x00	RO	This register contains the high byte of the 16-bit green channel data (or IR data if IR_MUX bit in CFG1 = 1).

BDATAL Register (Address 0x9A)

Figure 47:
BDATAL Register

Addr: 0x9A		BDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	BDATAL	0x00	RO	This register contains the low byte of the 16-bit blue channel data.

BDATAH Register (Address 0x9B)

Figure 48:
BDATAH Register

Addr: 0x9B		BDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	BDATAH	0x00	RO	This register contains the high byte of the 16-bit blue channel data.

PDATAL Register (Address 0x9C)

Figure 49:
PDATAL Register

Addr: 0x9C		PDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAL	0x00	RO	This register contains the low byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, this register contains the upper 8 most significant bits of the 10-bit proximity value.

PDATAH Register (Address 0x9D)

Figure 50:
PDATAH Register

Addr: 0x9D		PDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAH	0x00	RO	This register contains the high byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, bits 1:0 contain the lower 2 bits of the 10-bit proximity value.

Proximity data is stored as a 14-bit value (two bytes). Reading the low byte first latches the high byte. Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases. Proximity detection uses a 10-bit ADC that is extended to a 14-bit dynamic range for PDATA using the following formula:

$PDATA = ADC_{value} \times (16 / \text{actual number of pulses transmitted})$

PDATA is therefore proportional to the reflected energy independent of the number of pulses transmitted.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PDATAL contains the 8 most significant bits of the 10-bit value and PDATAH bit locations 1:0 contain the lower 2-bits. When APC is disabled, only the upper 8-bits are compared against the threshold values contained in PILTL and PIHTL.

REVID2 Register (Address 0x9E)

Figure 51:
REVID2 Register

Addr: 0x9E		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RO	Reserved.
3:0	REV_ID	0111	RO	Device revision number.

CFG2 Register (Address 0x9F)

Figure 52:
CFG2 Register

Addr: 0x9F		CFG2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0	RW	Reserved. Must be set to default value.

SOFTRST Register (Address 0xA0)

Figure 53:
SOFTRST Register

Addr: 0xA0		SOFTRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved. Must be set to default value.
0	SOFTRST	0	RW	Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state.

CFG3 Register (Address 0xAB)

Figure 54:
CFG3 Register

Addr: 0xAB		CFG3					
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**			
7	INT_READ_CLEAR	0	RW	If set, then all flag bits in the STATUS register will be reset whenever the STATUS register is read over I^2C.			
6:5	Reserved	0	RW	Reserved. Must be set to default value.			
4	SAI	0	RW	The Sleep After Interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.			
				PON	**SAI**	**INT**	**Oscillator**
				0	X	X	OFF
				1	0	X	ON
				1	1	1	ON
				1	1	0	OFF
3:0	Reserved	0100	RW	Reserved. Must be set to default value.			

The SAI bit sets the device operational mode following the completion of an ALS or proximity cycle. If AINT and AIEN are both set or if PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

CFG4 Register (Address 0xAC)

Figure 55:
CFG4 Register

Addr: 0xAC		CFG4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x3F	RW	Reserved. Must be set to 0x3D.

CFG6 Register (Address 0xAE)

Figure 56:
CFG6 Register

Addr: 0xAE		CFG6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Reserved	0	RW	Reserved. Must be set to default value.
6	APC Disable	0	RW	Proximity automatic pulse control (APC) disable. 0 = APC enabled 1 = APC disabled
5:0	Reserved	111111	RW	Reserved. Must be set to default value.

POFFSETL Register (Address 0xC0)

Figure 57:
POFFSETL Register

Addr: 0xC0		POFFSETL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSETL	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

POFFSETH Register (Address 0xC1)

Figure 58:
POFFSETH Register

Addr: 0xC1		POFFSETH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0	RW	Reserved. Must be set to default value.
0	POFFSETH	0	RW	This register contains the sign portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 255 is possible.

CALIB Register (Address 0xD7)

Figure 59:
CALIB Register

Addr: 0xD7		CALIB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	0	RW	Reserved. Must be set to default value.
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 0 = Electrical and optical crosstalk. 1 = Electrical crosstalk only.
4:1	Reserved	0	RW	Reserved. Must be set to default value.
0	START_OFFSET_ CAL	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a portion of the VCSEL IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in POFFSETL/H until the proximity result is as close to the binary search target as possible. Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

An electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CAL bits. To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_ OFFSET_CALIB. The CINT flag will assert after calibration has finished. Upon completion proximity offset registers are automatically loaded with calibration result.

CALIBCFG Register (Address 0xD9)

Figure 60:
CALIBCFG Register

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_ TARGET	2 (010)	RW	Proximity offset calibration result target.	
				Value	**PDATA Target**
				0 (000)	3
				1 (001)	7
				2 (010)	15
				3 (011)	31
				4 (100)	63
				5 (101)	127
				6 (110)	255
				7 (111)	511
4	Reserved	1	RW	Reserved. Must be set to default value.	
3	AUTO_ OFFSET_ADJ	0	RW	If set, this bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero.	
2:0	PROX_ AVG	0 (000)	RW	PROX_AVG defines the number of ADC samples collected and averaged during a cycle which become the proximity result.	
				Value	**Sample Size**
				0 (000)	Disable
				1 (001)	2
				2 (010)	4
				3 (011)	8
				4 (100)	16
				5 (101)	32
				6 (110)	64
				7 (111)	128

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target, and BINSEARCH_TARGET setting of 2 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_AVG field sets the number of ADC samples that are averaged to calculate the PDATA result.

CALIBSTAT Register (Address 0xDC)

Figure 61:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	Reserved	0	RW	Reserved. Must be set to default value.
2	OFFSET_ ADJUSTED	0	RW	Bit is set when the proximity offset has been automatically decremented if AUTO_OFFSET_ ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_ OFFSET_ADJ to 0.
1	Reserved	0	RW	Reserved. Must be set to default value.
0	CALIB_FINISHED	0	RW	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

INTENAB Register (Address 0xDD)

Figure 62:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ASIEN	0	RW	ALS Saturation Interrupt Enable
6	PSIEN	0	RW	Proximity Saturation Interrupt Enable
5	PIEN	0	RW	Proximity Interrupt Enable
4	AIEN	0	RW	ALS/Color Interrupt Enable
3	CIEN	0	RW	Calibration Interrupt Enable
2	ZIEN	0	RW	Zero Detect Interrupt Enable
1:0	Reserved	0	RW	Reserved. Must be set to default value.

FAC_L Register (Address 0xE6)

Figure 63:
FAC_L Register

Addr: 0xE6		FAC_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x00 – 0xFF	R	Reserved for lot code data

FAC_H Register (Address 0xE7)

Figure 64:
FAC_H Register

Addr: 0xE7		FAC_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x00 – 0xFF	R	Reserved for lot code data

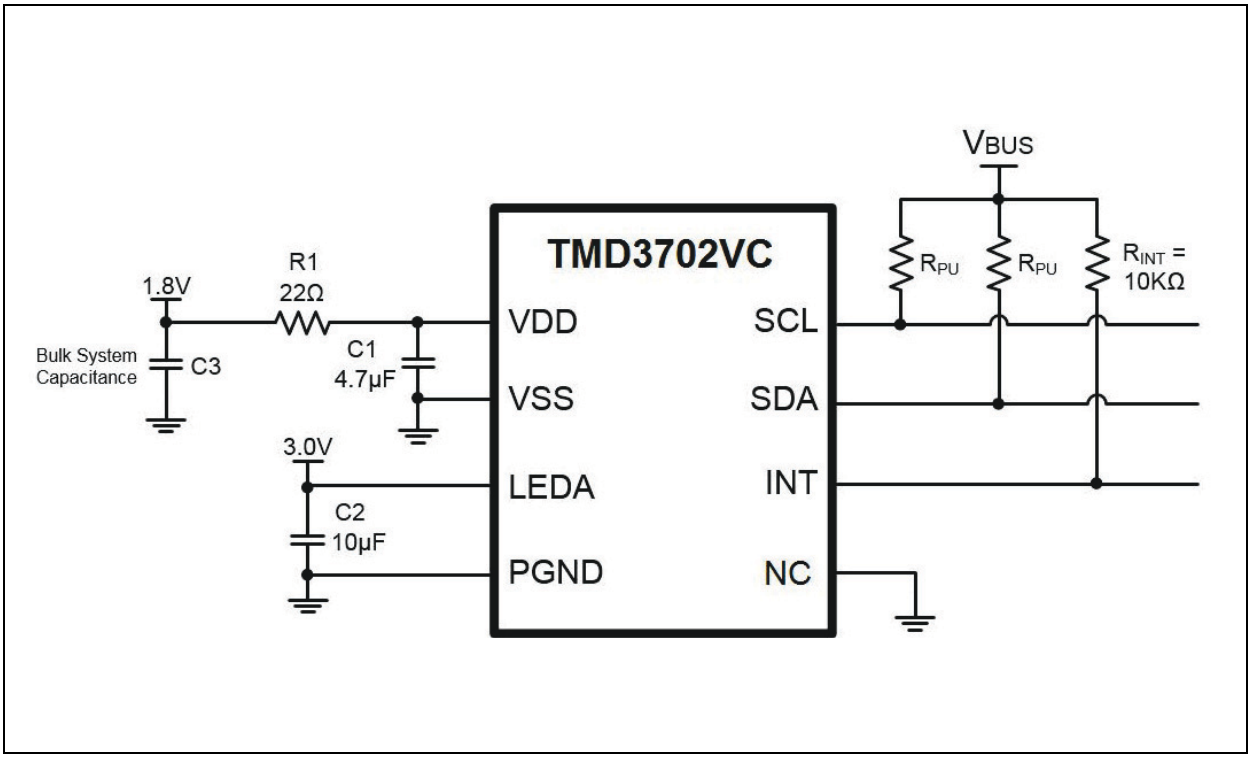
TEST3 Register (Address 0xF2)

Figure 65:
TEST3 Register

Addr: 0xF2		TEST3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x44	RW	Reserved. Must be set to 0xC4.

Application Information

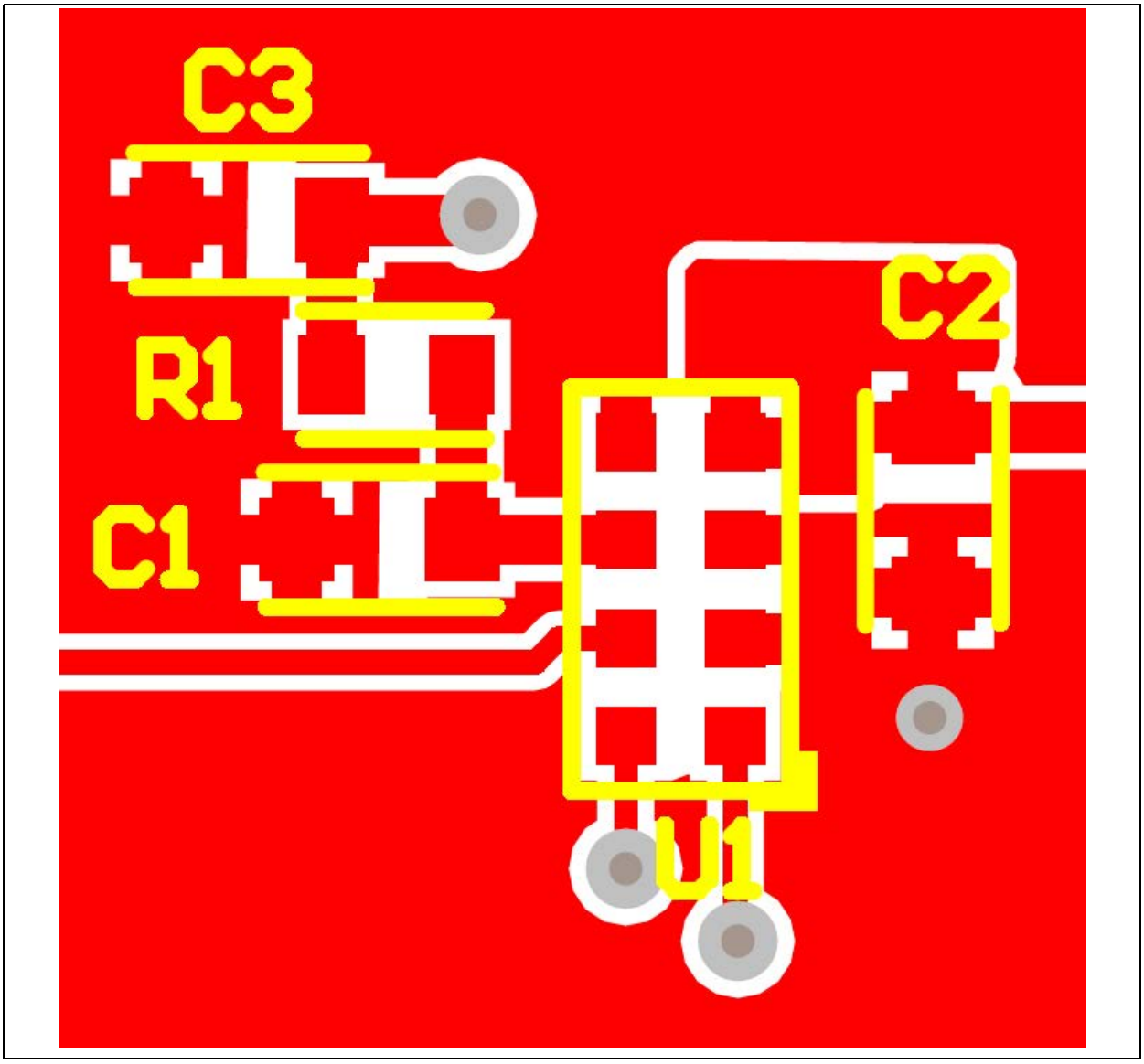
Figure 66:
Schematic



Note(s):

1. The bulk capacitor (C3) can affect the stability of a regulated supply output and should be chosen with the regulator characteristics in mind.
2. Place the 4.7µF VDD (C1) and 10µF LEDA (C2) capacitors within 5mm of the module.
3. The value of the I^2C pull up resistors RPU should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
4. VSS and PGND should be connected to the same solid ground plane as close to the device as possible.
5. To improve device ESD protection, it is recommended to connect NC to ground.

Figure 67:
TMD3702VC Recommended Circuit Layout

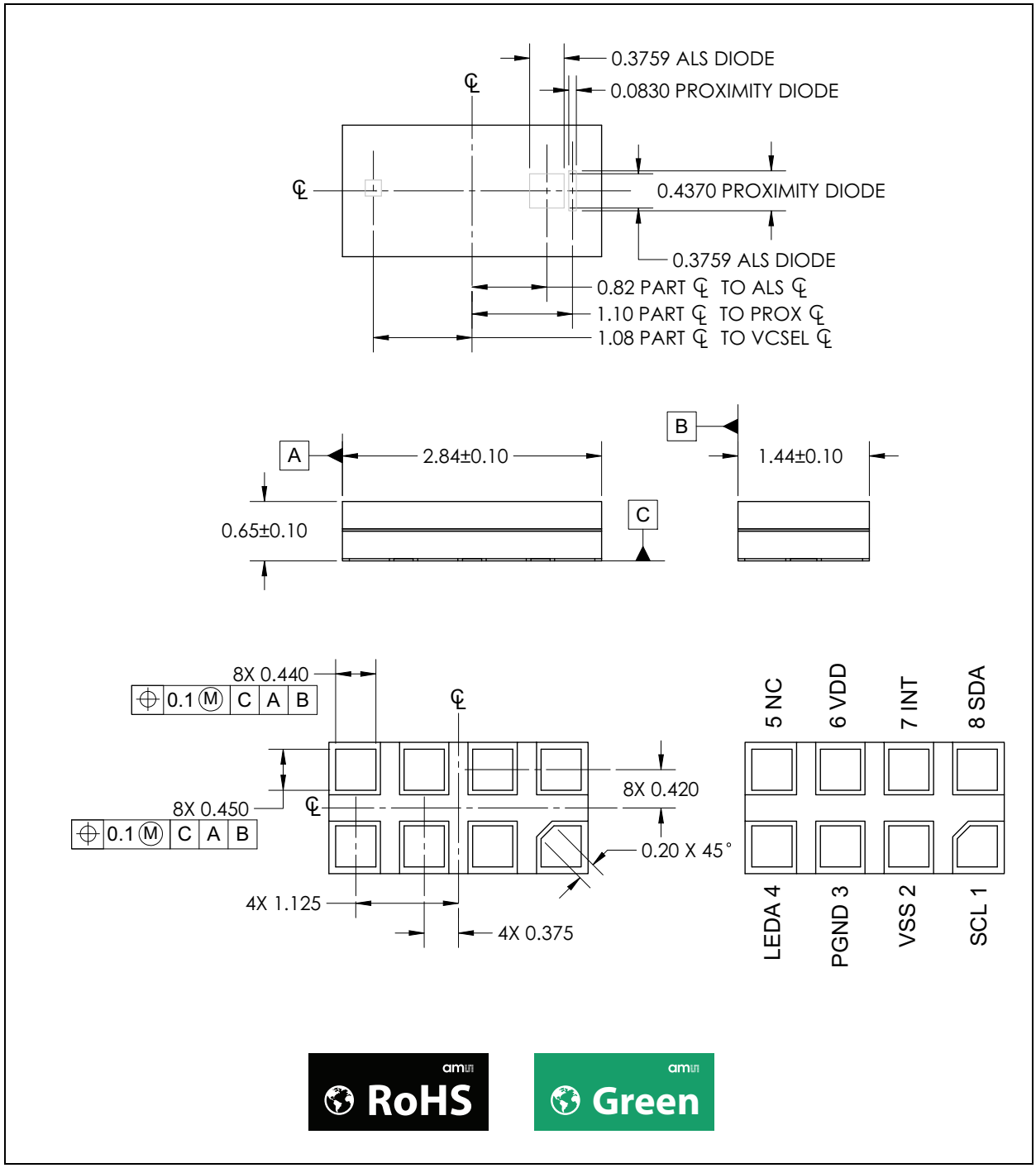


Note(s):

1. The dominant factor governing device performance is the component placement, not necessarily component value. The placement of the decoupling capacitor, C2, is the most critical. Place the component on the same side of PCB as device as shown in the figure above. Make connection as close as possible to minimize series inductance and resistance. This is critical.

Package Drawings & Markings

Figure 68:
Package Drawing



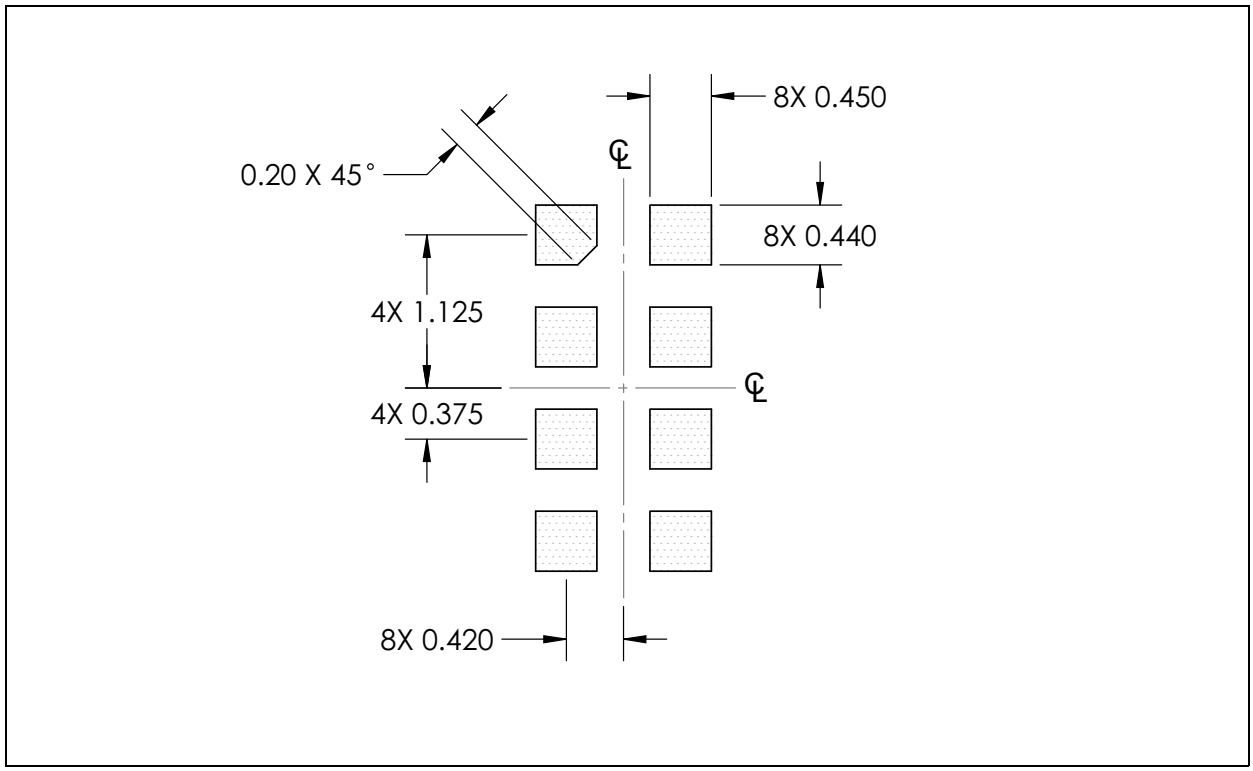
Note(s):

1. All linear dimensions are in millimeters.
2. Contact finish is Au.
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 69:
Recommended PCB Pad Layout

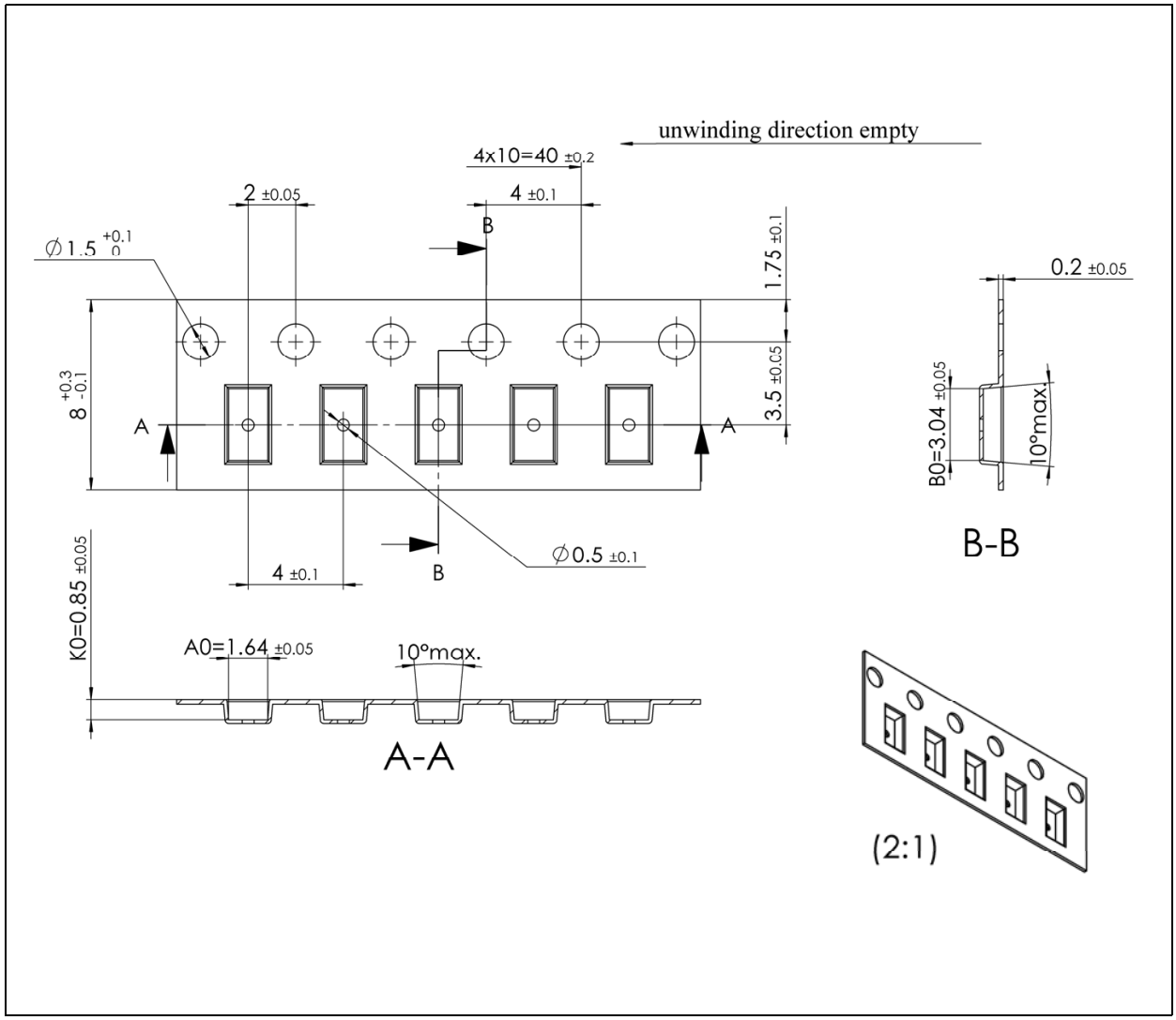


Note(s):

1. All dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Tape & Reel Information

Figure 70:
Tape & Reel Information



Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481-B 2001.
4. Each reel is 330mm in diameter and contains 10000 parts.
5. **ams** packaging tape and reel conform to the requirements of EIA Standard 481-B.
6. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering & Storage Information

The FN package has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate.

The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

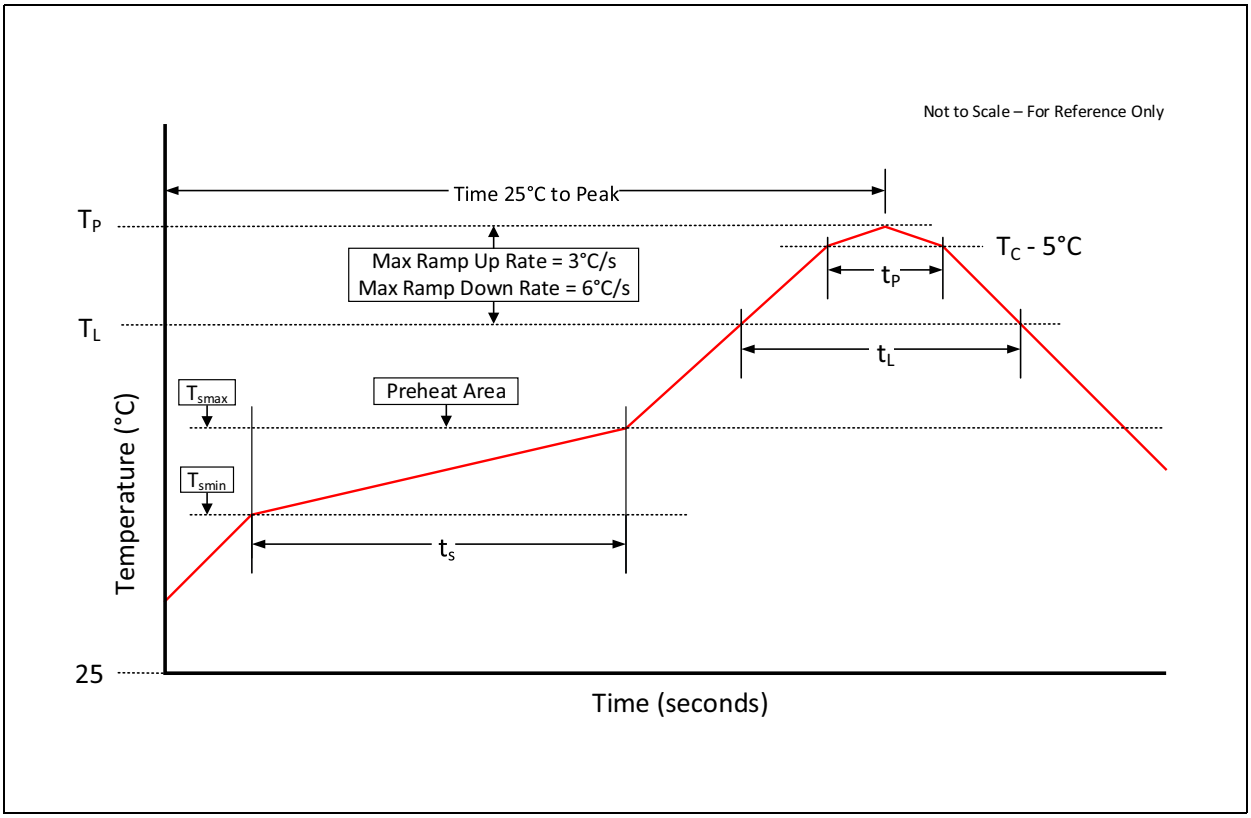
Figure 71:
Solder Reflow Profile

Profile Feature Preheat/ Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100 °C	150 °C
Temperature Max (T_{smax})	150 °C	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp. of 235 °C For suppliers T_P must equal or exceed the classification temp of 235 °C	For users T_P must not exceed the classification temp. of 260 °C For suppliers T_P must equal or exceed the classification temp of 260 °C
Time (t_P) (1) within 5 °C of the specified classification temperature (T_C)	20 (1) seconds	30 (1) seconds
Ramp-down rate (T_P to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 72:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: < 40°C
- Relative Humidity: < 90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: < 30°C
- Relative Humidity: < 60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Laser Eye Safety

Complies with IEC/EN 60825-1:2014 and 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated June 24, 2007

The TMD3702VC is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC/EN 60825-1:2014. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions. Use outside of the recommended condition or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Ordering & Contact Information

Figure 73:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD37024VC	1.8V	0x49	Tape & Reel (13”)	10000pcs/reel
TMD37024VCM	1.8V	0x49	Tape & Reel (7”)	1000pcs/reel

Buy our products or get free samples online at:
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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1-03 (2018-Nov-27) to current revision 1-04 (2020-Apr-07)	Page
Updated Figure 6	5

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide