Si5380
Data Sheet Errata

This document contains information on the errata of product revision B of Si5380.

The device data sheet explains how to identify chip revision, either from package marking or electronically.

Errata effective date: 15 June 2015. Applies to the Si5380 data sheet revision 0.96.

Note: This document applies to Ordering Part Numbers (OPNs) which refer to product revision **B** (silicon revision A2). For example: Si5380A-**B**-GM or Si5380A-**B**xxxxx-GM, where xxxxx is the custom OPN ID, and B refers to the product revision.

ERRATA DEFINITIONS

Impact Definition: Each erratum is marked with an impact, as defined below:

- Minor—Workaround exists.
- Major—Errata that do not conform to the data sheet or standard.
- Information—The device behavior is not ideal but acceptable. Typically, the data sheet and/or ClockBuilder Pro may be changed to match the device behavior.

Table .1. Errata Status Summary

Erratum	Title/Problem	Impact	Workarounds	Resolution
1	LVCMOS high-impedance mode is too low	Information	Yes	Data sheet and CBPro have been updated. Will also be fixed in the next silicon revision.
2	LOS sticky status bits cannot be cleared unless the fault monitors are temporarily disabled	Minor	Yes	Will be fixed in the next silicon revision.
3	Output-to-output clock skew between clocks generated from different MultiSynth dividers is not consistent at high junction temperatures	Major	No	Will be fixed in the next silicon revision.
4	Input-to-output clock delay variation is not consistent at high junction temperatures	Minor	Yes	Will be fixed in the next silicon revision.
5	SMBus timeout	Major	No	Will be fixed in the next silicon revision.

1. LVCMOS High-Impedance Mode is Too Low

Description

LVCMOS high-impedance is too low.

Impact without Workarounds

In earlier versions of ClockBuilder Pro (e.g., prior to v1.0), LVCMOS and differential output formats could be user-configured to disable in a low logic state, a high logic state, or in a stop mid (high-impedance or Hi-Z) state. The LVCMOS high-impedance mode should not be used.

Woraround

Select the disable state as stop-high or stop-low.

Resolution

This erratum will be fixed in the next silicon revision. ClockBuilder Pro (prior to v1.0) no longer allowed users to select the Hi-Z disable state. The Si5380 data sheet, beginning with v0.96, also removes support for Hi-Z mode.

2. LOS Sticky Status Bits Cannot Be Cleared

Description

LOS sticky status bits cannot be cleared unless the fault monitors are temporarily disabled.

Impact

When two or more LOS sticky status bits are asserted, clearing either one or both requires disabling all the LOS fault monitors. LOS sticky (flag) bits will always remain set whenever asserted. Clearing the sticky bit(s) will have no effect.

Workaround

It is possible to clear a sticky bit by temporarily disabling all LOS fault monitors. Once disabled, the bit can be cleared and the fault monitor re-enabled.

Resolution

This erratum will be fixed in the next silicon revision.

3. Output-to-Output Clock Skew

Description

Output-to-output clock skew between clocks generated from **different** N dividers is not consistent at high junction temperatures.

Impact

If the chip is powered-up, or a hard or soft reset is performed when the junction temperature exceeds 100 °C, the output-to-output skew may exceed the data sheet specification (for all outputs connected to **different** N dividers). Consult the data sheet addendum generated from ClockBuilder Pro to determine which output clocks in your plan are connected to one of the various MultiSynth dividers.

Note: When clock outputs are connected to the **same** N divider, data sheet specifications have been added for output-to-output skew. In this case, the output-to-output skew specifications are 20 ps (typical) and 50 ps (max).

Workaround

None.

Resolution

This erratum will be fixed in the next silicon revision.

4. Input-to-Output Clock Delay Variation

Description

The input-to-output clock delay variation performance is not consistent when operating the chip at high junction temperatures.

Impact

If the chip is powered-up, or a hard or soft reset is performed when the junction temperature exceeds 90 °C, the input-to-output clock delay variation may exceed the data sheet specification of 2 ns (typical).

Note: The input-to-output delay variation specification (previously and erroneously referred to as input-to-output delay in preliminary documentation prior to v0.96) is 2 ns (typical).

Workaround

Configure the device in Zero Delay Mode. All clock outputs connected to the **same** N dividers will have consistent input-to-output delay variation performance from -25 to +125 °C.

Resolution

This erratum will be fixed in the next silicon revision.

5. SMBUS Timeout Register Setting (SMBUS_TIMEOUT) Does Not Assert

Description

The SMBus timeout register setting (SMBUS_TIMEOUT) does not assert when the device exceeds the 35 ms maximum value prescribed by the standard.

Impact

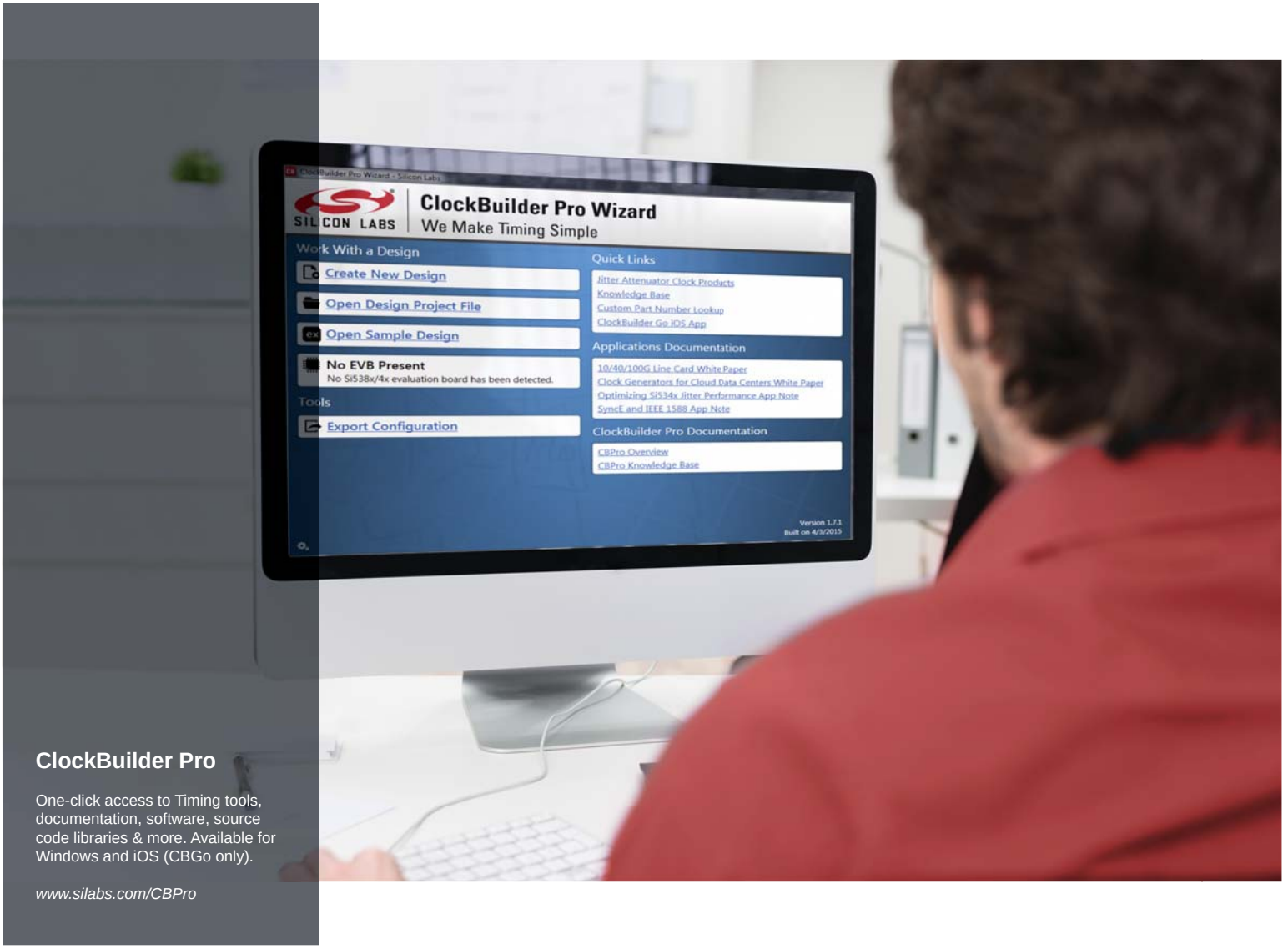
If SMBUS_TIMEOUT is mapped to affect the hardware interrupt pin (INTR#), the SDA bus will not be released as expected and required by the SMBus standard.

Workaround

None. Avoid reliance on the SMBus timeout feature.

Resolution

This erratum will be fixed in the next silicon revision.



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro

Timing Portfolio
www.silabs.com/timing

SW/HW
www.silabs.com/CBPro

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com