MUN5313DW1, NSBC144EPDXV6, NSBC144EPDP6

Complementary Bias Resistor Transistors
R1 = 47 kΩ, R2 = 47 kΩ

NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

$(T_A = 25°C$ both polarities Q_1 (PNP) & Q_2 (NPN), unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current – Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	40	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

| Device	Package	Shipping[†]
MUN5313DW1T1G, SMUN5313DW1T1G*	SOT–363	3,000/Tape & Reel
SMUN5313DW1T3G*	SOT–363	10,000/Tape & Reel
NSBC144EPDXV6T1G NSVBC144EPDXV6T1G*	SOT–563	4,000/Tape & Reel
NSBC144EPDXV6T5G	SOT–563	8,000/Tape & Reel
NSBC144EPDP6T5G	SOT–963	8,000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
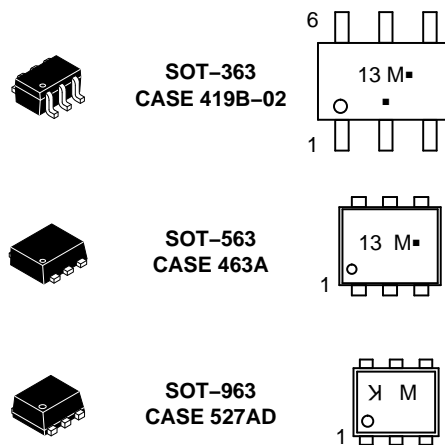
ON Semiconductor®

PIN CONNECTIONS

MARKING DIAGRAMS

SOT–363
CASE 419B–02

SOT–563
CASE 463A

SOT–963
CASE 527AD
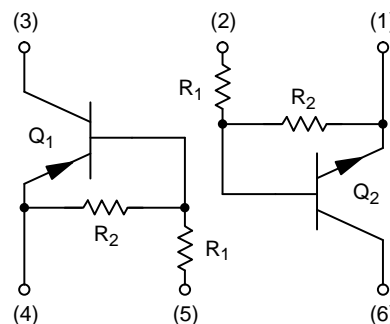
13/K = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

1

THERMAL CHARACTERISTICS

| Characteristic	Symbol	Max	Unit
MUN5313DW1 (SOT−363) ONE JUNCTION HEATED			

Total Device Dissipation
   $T_A = 25°C$ (Note 1)
       (Note 2)
   Derate above 25°C   (Note 1)
       (Note 2)
	P_D	187
		256
		1.5
		2.0
			mW
			
			mW/°C

Thermal Resistance, (Note 1) Junction to Ambient (Note 2)	$R_{θJA}$	670 490	°C/W
MUN5313DW1 (SOT−363) BOTH JUNCTION HEATED (Note 3)			

Total Device Dissipation
   $T_A = 25°C$ (Note 1)
       (Note 2)
   Derate above 25°C   (Note 1)
       (Note 2)
	P_D	250
		385
		2.0
		3.0
			mW
			
			mW/°C

Thermal Resistance,
   Junction to Ambient   (Note 1)
       (Note 2)
	$R_{θJA}$	493
		325
			°C/W

Thermal Resistance,
   Junction to Lead   (Note 1)
       (Note 2)
	$R_{θJL}$	188
		208
			°C/W

Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
NSBC144EPDXV6 (SOT−563) ONE JUNCTION HEATED			

Total Device Dissipation
   $T_A = 25°C$ (Note 1)
   Derate above 25°C   (Note 1)
	P_D	357
		2.9
			mW
			mW/°C

Thermal Resistance, Junction to Ambient (Note 1)	$R_{θJA}$	350	°C/W
NSBC144EPDXV6 (SOT−563) BOTH JUNCTION HEATED (Note 3)			

Total Device Dissipation
   $T_A = 25°C$ (Note 1)
   Derate above 25°C   (Note 1)
	P_D	500
		4.0
			mW
			mW/°C

Thermal Resistance, Junction to Ambient (Note 1)	$R_{θJA}$	250	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
NSBC144EPDP6 (SOT−963) ONE JUNCTION HEATED			

Total Device Dissipation
   $T_A = 25°C$ (Note 4)
       (Note 5)
   Derate above 25°C   (Note 4)
       (Note 5)
	P_D	231
		269
		1.9
		2.2
			MW
			
			mW/°C

Thermal Resistance,
   Junction to Ambient   (Note 4)
       (Note 5)
	$R_{θJA}$	540
		464
			°C/W

NSBC144EPDP6 (SOT−963) BOTH JUNCTION HEATED (Note 3)			

Total Device Dissipation
   $T_A = 25°C$ (Note 4)
       (Note 5)
   Derate above 25°C   (Note 4)
       (Note 5)
	P_D	339
		408
		2.7
		3.3
			MW
			
			mW/°C

Thermal Resistance,
   Junction to Ambient   (Note 4)
       (Note 5)
	$R_{θJA}$	369
		306
			°C/W

Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0×1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR−4 @ 100 mm^2, 1 oz. copper traces, still air.
5. FR−4 @ 500 mm^2, 1 oz. copper traces, still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C both polarities Q_1 (PNP) & Q_2 (NPN), unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
Collector-Base Breakdown Voltage (I_C = 10 µA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 6) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 6) (I_C = 5.0 mA, V_{CE} = 10 V)	h_{FE}	80	140	–	
Collector-Emitter Saturation Voltage (Note 6) (I_C = 10 mA, I_B = 0.3 mA)	$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (Off) (V_{CE} = 5.0 V, I_C = 100 µA) (NPN) (V_{CE} = 5.0 V, I_C = 100 µA) (PNP)	$V_{i(off)}$	– –	1.2 1.2	– –	Vdc
Input Voltage (On) (V_{CE} = 0.2 V, I_C = 3.0 mA) (NPN) (V_{CE} = 0.2 V, I_C = 3.0 mA) (PNP)	$V_{i(on)}$	– –	1.9 2.0	– –	Vdc
Output Voltage (On) (V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (Off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	32.9	47	61.1	kΩ
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

6. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.
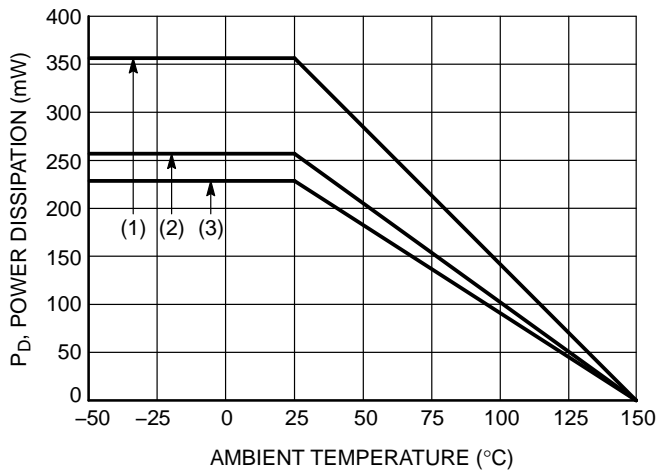
(1) SOT−363; 1.0 × 1.0 Inch Pad
(2) SOT−563; Minimum Pad
(3) SOT−963; 100 mm^2, 1 oz. Copper Trace

Figure 1. Derating Curve

MUN5313DW1, NSBC144EPDXV6, NSBC144EPDP6

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
MUN5313DW1, NSBC144EPDXV6
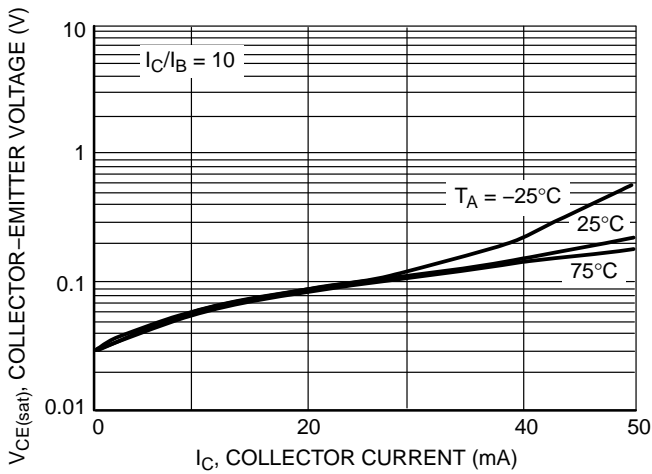
Figure 2. $V_{CE(sat)}$ vs. I_C
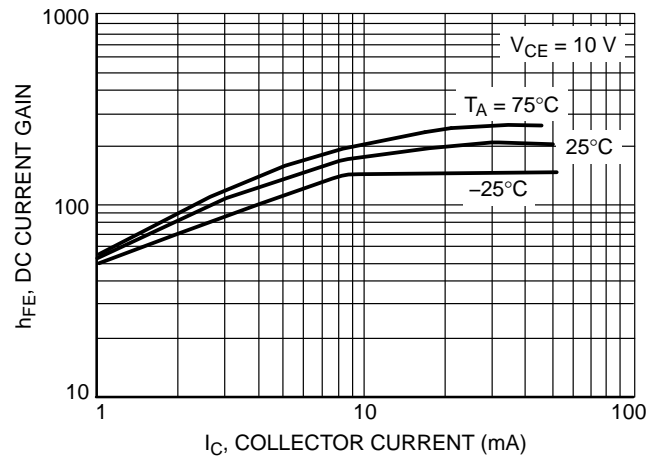
Figure 3. DC Current Gain
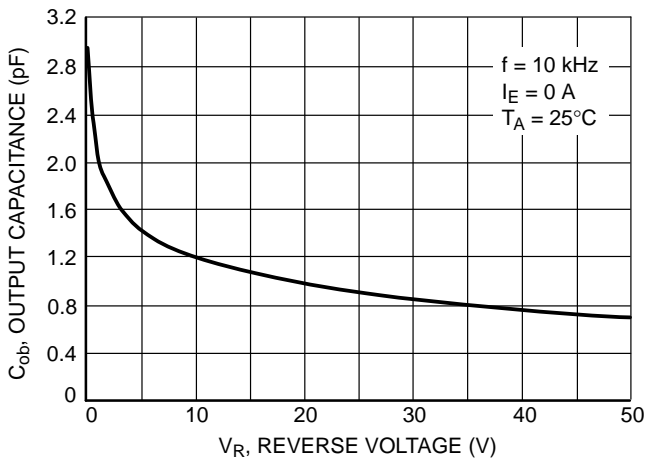
Figure 4. Output Capacitance
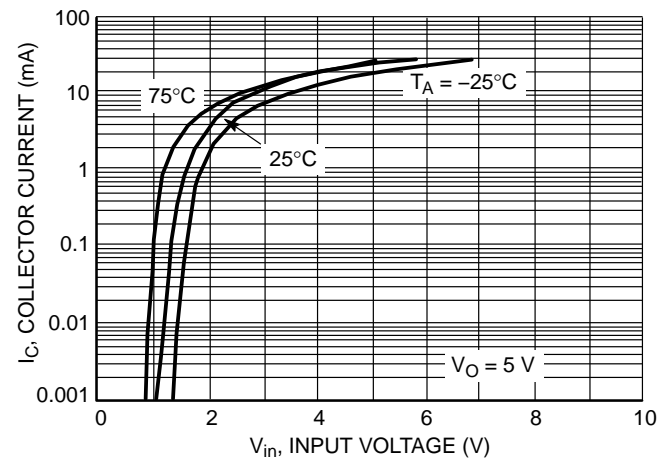
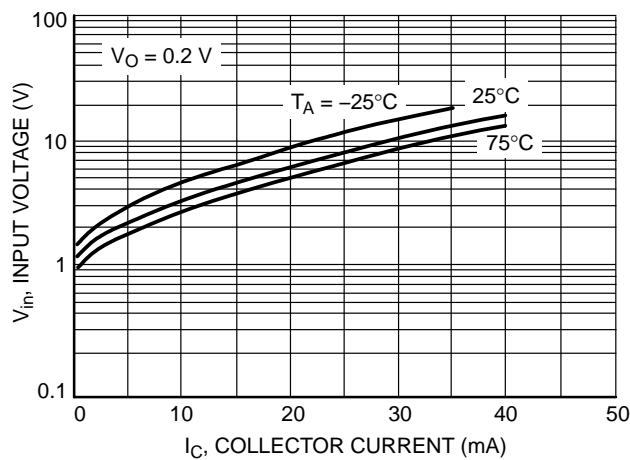**Figure 5. Output Current vs. Input Voltage**

Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
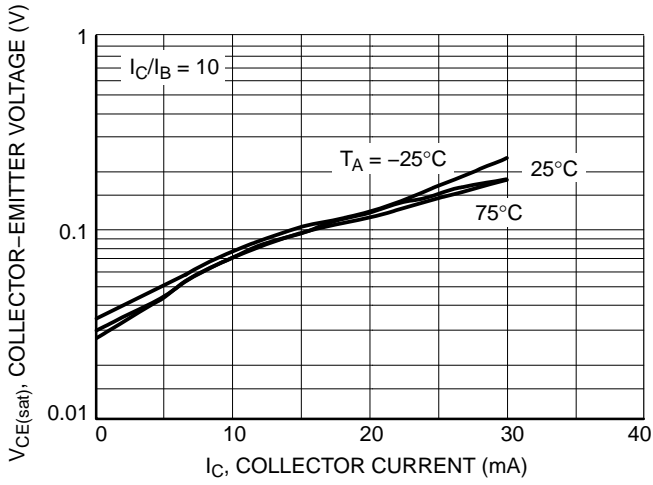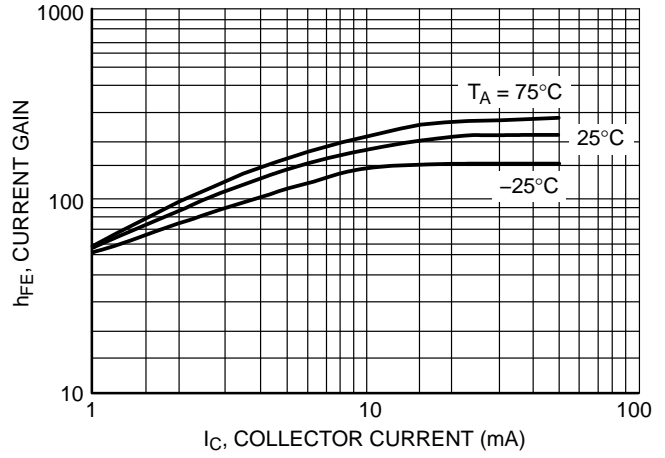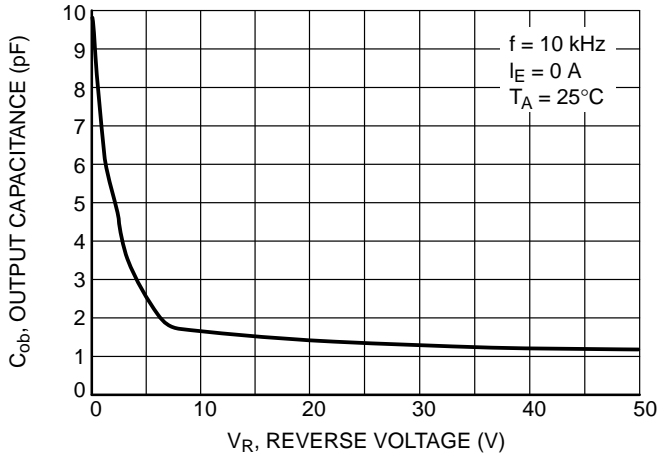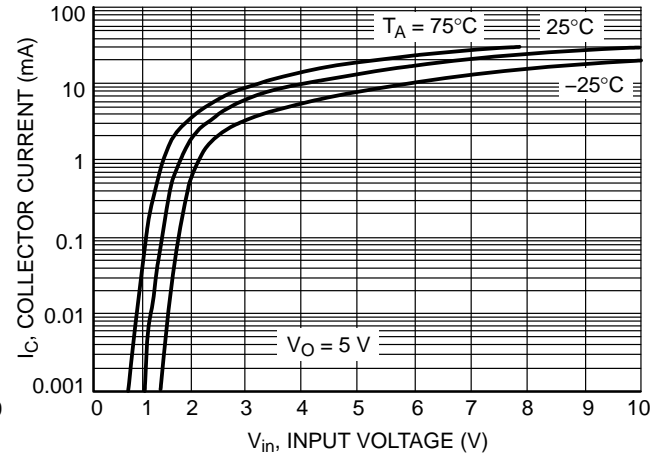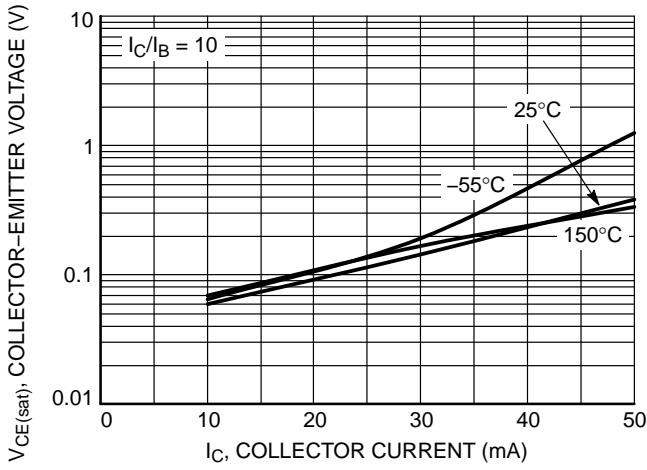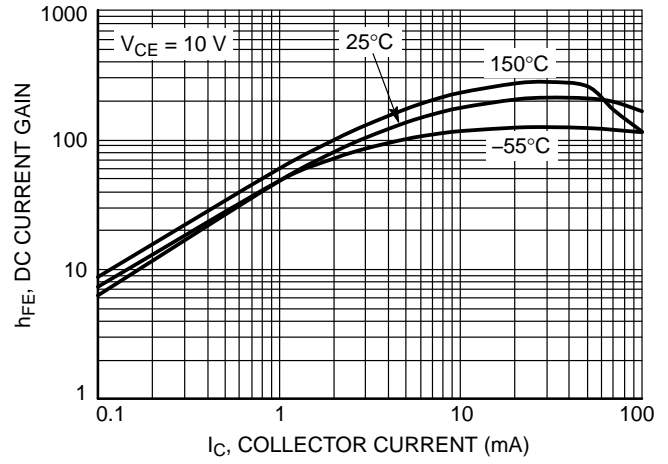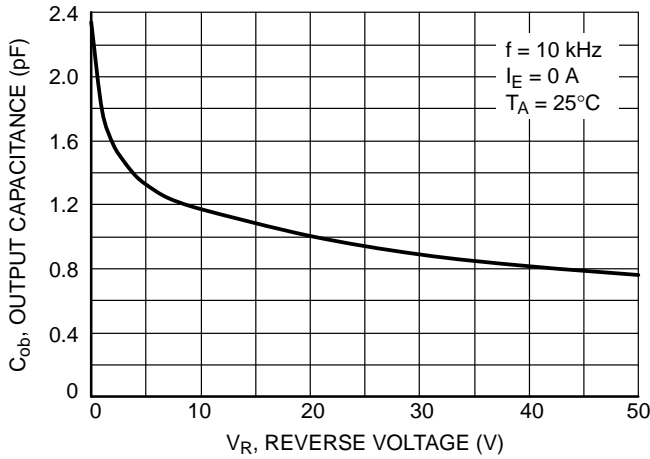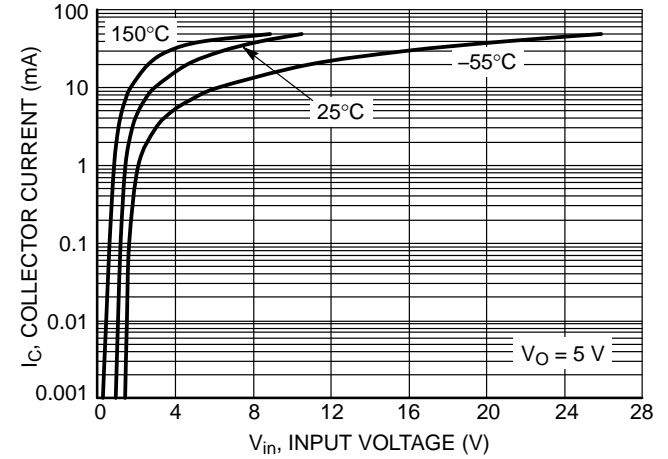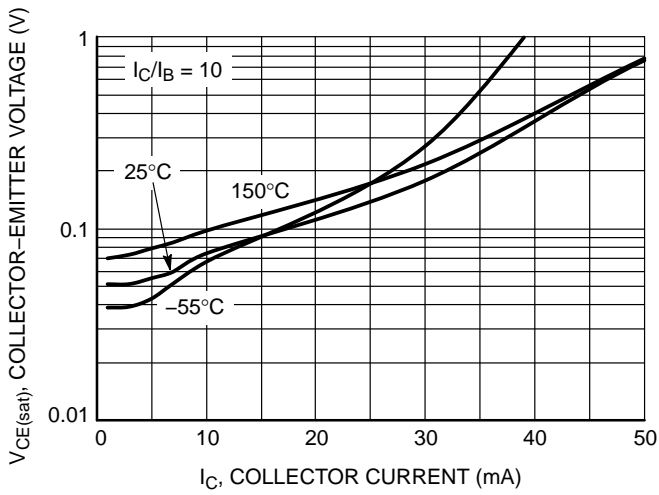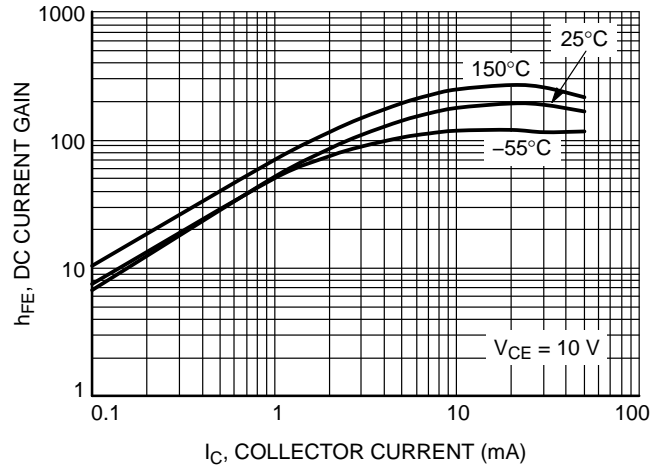### MUN5313DW1, NSBC144EPDXV6

Figure 7. $V_{CE(sat)}$ vs. I_C

Figure 8. DC Current Gain

Figure 9. Output Capacitance

Figure 10. Output Current vs. Input Voltage
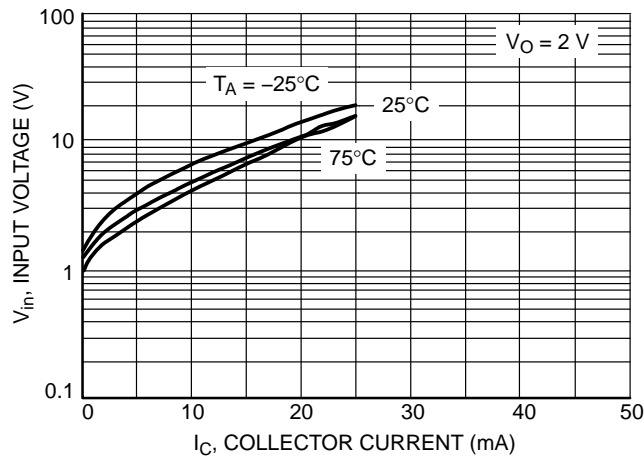
Figure 11. Input Voltage vs. Output Current

MUN5313DW1, NSBC144EPDXV6, NSBC144EPDP6

TYPICAL CHARACTERISTICS – NPN TRANSISTOR
NSBC144EPDP6

Figure 12. $V_{CE(sat)}$ vs. I_C

Figure 13. DC Current Gain

Figure 14. Output Capacitance

Figure 15. Output Current vs. Input Voltage
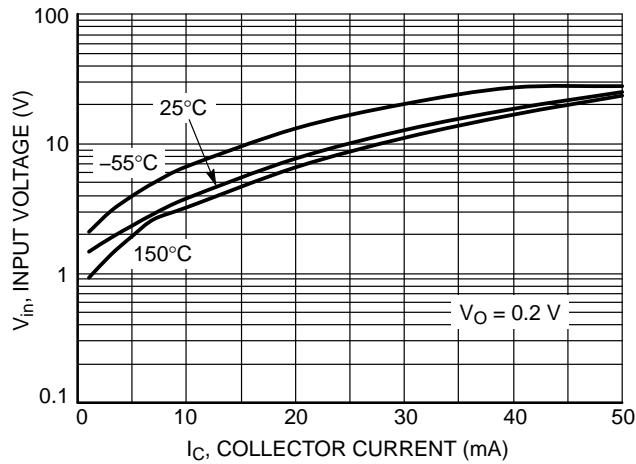
Figure 16. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – PNP TRANSISTOR
NSBC144EPDP6

Figure 17. $V_{CE(sat)}$ vs. I_C

Figure 18. DC Current Gain
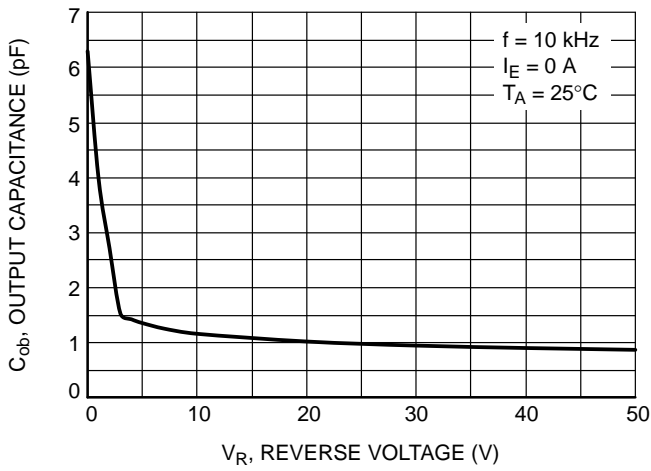
Figure 19. Output Capacitance
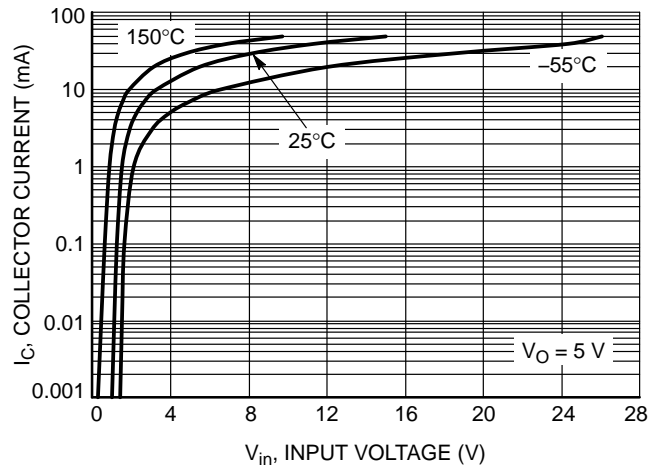
Figure 20. Output Current vs. Input Voltage
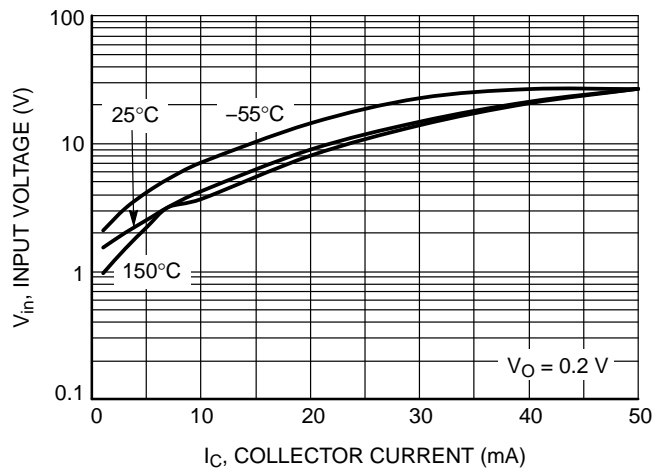
Figure 21. Input Voltage vs. Output Current

onsemi

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

1
SCALE 2:1

DATE 11 DEC 2012

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

TOP VIEW

DETAIL A

SIDE VIEW

END VIEW

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

RECOMMENDED
SOLDERING FOOTPRINT*

6X
0.30

6X
0.66

2.50

0.65
PITCH

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

6

XXXM■

1

XXX = Specific Device Code
M = Date Code*
■ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42985B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SC−88/SC70−6/SOT−363		PAGE 1 OF 2

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.
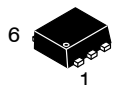
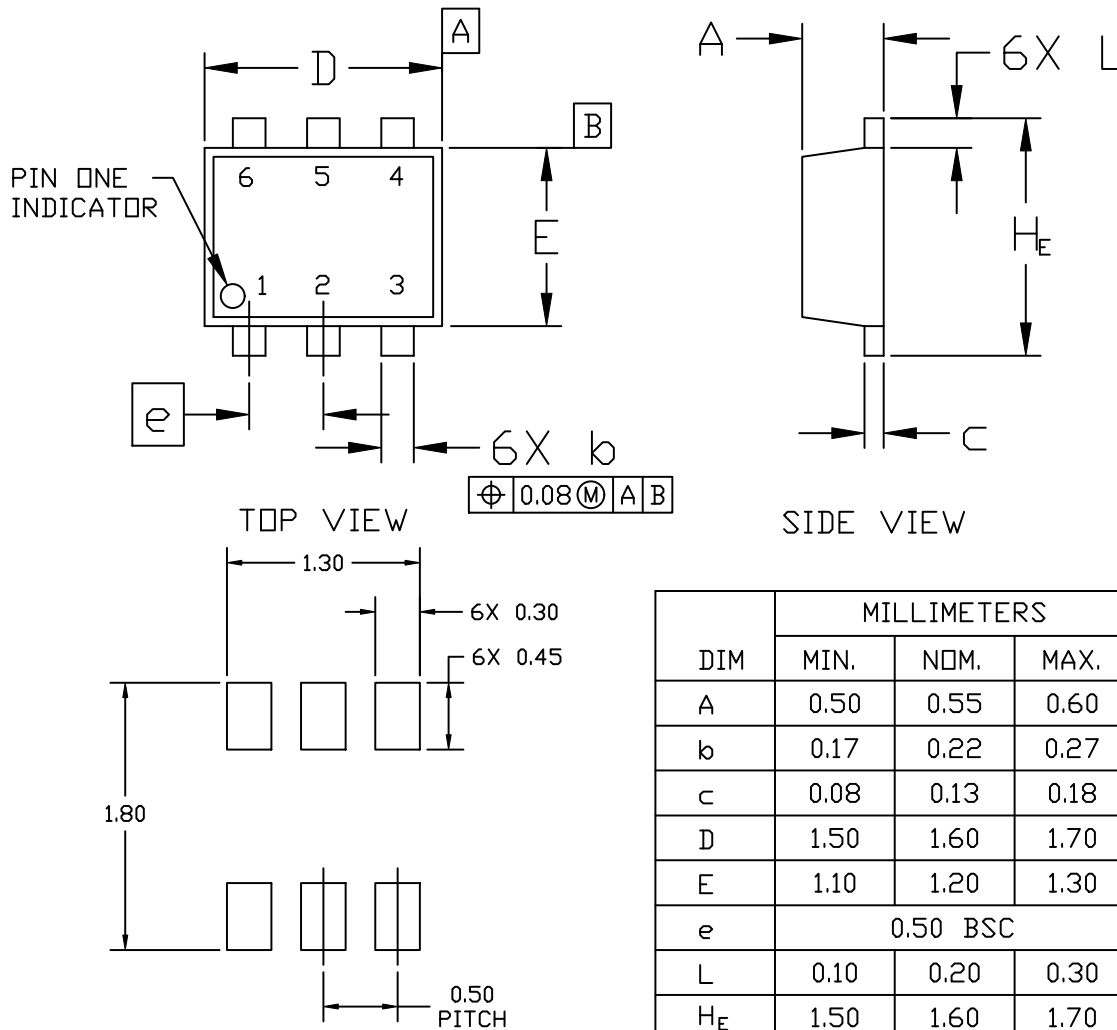| DOCUMENT NUMBER: | 98ASB42985B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| DESCRIPTION: | SC−88/SC70−6/SOT−363 | | PAGE 2 OF 2 |

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6

1

SCALE 4:1

SOT−563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

TOP VIEW

SIDE VIEW

RECOMMENDED MOUNTING FOOTPRINT*
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
L	0.10	0.20	0.30
H_E	1.50	1.60	1.70

DOCUMENT NUMBER:	98AON11126D		
DESCRIPTION:	SOT−563, 6 LEAD		PAGE 1 OF 2

SOT−563, 6 LEAD
CASE 463A
ISSUE H

DATE 26 JAN 2021

STYLE 1:
PIN 1. EMITTER 1
     2. BASE 1
     3. COLLECTOR 2
     4. EMITTER 2
     5. BASE 2
     6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
     2. EMITTER 2
     3. BASE 2
     4. COLLECTOR 2
     5. BASE 1
     6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
     2. CATHODE 1
     3. ANODE/ANODE 2
     4. CATHODE 2
     5. CATHODE 2
     6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
     2. COLLECTOR
     3. BASE
     4. EMITTER
     5. COLLECTOR
     6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
     2. CATHODE
     3. ANODE
     4. ANODE
     5. CATHODE
     6. CATHODE

STYLE 6:
PIN 1. CATHODE
     2. ANODE
     3. CATHODE
     4. CATHODE
     5. CATHODE
     6. CATHODE

STYLE 7:
PIN 1. CATHODE
     2. ANODE
     3. CATHODE
     4. CATHODE
     5. ANODE
     6. CATHODE

STYLE 8:
PIN 1. DRAIN
     2. DRAIN
     3. GATE
     4. SOURCE
     5. DRAIN
     6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
     2. GATE 1
     3. DRAIN 2
     4. SOURCE 2
     5. GATE 2
     6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
     2. N/C
     3. CATHODE 2
     4. ANODE 2
     5. N/C
     6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
     2. BASE 2
     3. COLLECTOR 1
     4. EMITTER 1
     5. BASE 1
     6. COLLECTOR 2

**GENERIC
MARKING DIAGRAM***

XX M▪

1

XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to
 device data sheet for actual part marking.
 Pb−Free indicator, "G" or microdot "▪", may
 or may not be present. Some products may
 not follow the Generic Marking.

SOT–963
CASE 527AD–01
ISSUE E

DATE 09 FEB 2010

SCALE 4:1

TOP VIEW

SIDE VIEW

BOTTOM VIEW

⊕ | 0.08 | X | Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

**GENERIC
MARKING DIAGRAM***

XM

X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot " ▪ ", may or may not be present.

**RECOMMENDED
MOUNTING FOOTPRINT**

DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. EMITTER 1
     2. BASE 1
     3. COLLECTOR 2
     4. EMITTER 2
     5. BASE 2
     6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
     2. EMITTER2
     3. BASE 2
     4. COLLECTOR 2
     5. BASE 1
     6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
     2. CATHODE 1
     3. ANODE/ANODE 2
     4. CATHODE 2
     5. CATHODE 2
     6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
     2. COLLECTOR
     3. BASE
     4. EMITTER
     5. COLLECTOR
     6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
     2. CATHODE
     3. ANODE
     4. ANODE
     5. CATHODE
     6. CATHODE

STYLE 6:
PIN 1. CATHODE
     2. ANODE
     3. CATHODE
     4. CATHODE
     5. CATHODE
     6. CATHODE

STYLE 7:
PIN 1. CATHODE
     2. ANODE
     3. CATHODE
     4. CATHODE
     5. ANODE
     6. CATHODE

STYLE 8:
PIN 1. DRAIN
     2. DRAIN
     3. GATE
     4. SOURCE
     5. DRAIN
     6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
     2. GATE 1
     3. DRAIN 2
     4. SOURCE 2
     5. GATE 2
     6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
     2. N/C
     3. CATHODE 2
     4. ANODE 2
     5. N/C
     6. ANODE 1

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