SBAS327A − JUNE 2004 − REVISED SEPTEMBER 2004

# High-Performance 24-Bit, 216kHz Sampling Four-Channel Audio Analog-to-Digital Converter

## FEATURES

- Four High-Performance Delta-Sigma Analog-to-Digital Converters
  - 24-Bit Linear PCM or 1-Bit Direct Stream Digital (DSD) Output Data
  - Supports PCM Output Sampling Rates up to 216kHz
  - Supports 64$f_S$ and 128$f_S$ DSD Output Data Rates
- Dynamic Performance: PCM Output
  - Dynamic Range: 118dB
  - THD+N: −105dB
- Dynamic Performance: DSD Output
  - Dynamic Range: 115dB
  - THD+N: −103dB
- Audio Serial Port
  - 24-Bit Linear PCM Output Data
  - Master or Slave Mode Operation
  - Supports Left-Justified, Right-Justified, $I^2S$, and TDM Data Formats
- DSD Data Port
  - Supports DSD Output or Input for All Four Channels Simultaneously
  - Input Mode Provides 1-Bit DSD to 24-Bit PCM Data Format Conversion
- Additional PCM Output Features
  - Linear-Phase Digital Decimation Filter
  - Digital High-Pass Filter for DC Removal
  - Clipping Flag Output for Each Channel
- Power Supplies: +5V Analog and +3.3V Digital
- Power Dissipation:
  - $f_S$ = 48kHz: 600mW typical
  - $f_S$ = 96kHz: 640mW typical
  - $f_S$ = 192kHz: 615mW typical
- Power-Down Mode
- Available in a Thermally-Enhanced HTQFP-64 Package

## APPLICATIONS

- Digital Recorders and Mixing Desks
- Digital Audio Effects Processors
- Broadcast Studio Equipment
- Surround Sound Encoders
- High-End A/V Receivers

## DESCRIPTION

The PCM4204 is a high-performance, four-channel analog-to-digital (A/D) converter designed for professional and broadcast audio applications. The PCM4204 architecture utilizes a 1-bit delta-sigma modulator per channel incorporating a novel density modulated dither scheme for improved dynamic performance.

The PCM4204 supports 24-bit linear PCM output data, with sampling frequencies up to 216kHz. The PCM4204 can also be configured to output either 64x or 128x oversampled, 1-bit direct stream digital (DSD) data for each channel. In addition, the PCM4204 supports a DSD input mode, allowing 1-bit DSD to 24-bit PCM data format conversion utilizing the on-chip digital decimation filter. These features make the PCM4204 suitable for a variety of digital audio recording and processing applications.

The PCM4204 includes a flexible audio serial port interface, which supports standard PCM audio data formats, as well as time division multiplexed (TDM) PCM data formats. Multiple format support allows the system designer to choose the interface format that best suits the end application. Audio data format selection, sampling mode configuration, and high-pass filter functions are all programmed using dedicated control pins.

The PCM4204 operates from a +5V analog power supply and a +3.3V digital power supply. The digital I/O pins are compatible with +3.3V logic families. The PCM4204 is available in a thermally-enhanced HTQFP-64 PowerPAD™ package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

| | | PCM4204 | UNIT |
|---|---|---|---|
| Supply voltage | $V_{CC}1$, $V_{CC}2$ | +6.0 | V |
| | $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | +3.6 | V |
| Ground voltage differences | (any AGND to DGND or BGND) | ±0.1 | V |
| Digital input voltage | FMT0, FMT1, FMT2, S/$\overline{M}$, FS0, FS1, FS2, SCKI, $\overline{RST}$, HPFD, SUB, BCK, LRCK, DSDCLK, DSD1, DSD2, DSD3, DSD4, TEST | −0.3 to ($V_{DD}$ + 0.3) | V |
| Analog input voltage | $V_{IN}1-4+$, $V_{IN}1-4-$ | −0.3 to ($V_{CC}$ + 0.3) | V |
| Input current (any pin except supplies) | | ±10mA | V |
| Operating temperature range | | −10 to +70 | °C |
| Storage temperature range, $T_{STG}$ | | −65 to +150 | °C |

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet.

## ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all characteristics specified with $T_A$ = +25°C, $V_{CC}$ = +5V, $V_{DD}$ = +3.3V, system clock (SCKI) is 512$f_S$ for Single Rate Sampling, 256$f_S$ for Dual Rate Sampling, or 128$f_S$ for Quad Rate Sampling. The device is operated in Master mode for all dynamic performance measurements.

| PARAMETER | | TEST CONDITIONS | PCM4204 MIN | PCM4204 TYP | PCM4204 MAX | UNIT |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | 24 | | Bits |
| **DATA FORMAT** | | | | | | |
| Audio Data Formats (PCM) | | | | Left and Right Justified, I²S, TDM | | |
| Audio Data Word Length (PCM) | | | | 24 | | Bits |
| Binary Data Format (PCM) | | | | Two's Complement Binary, MSB First | | |
| DSD Output Format and Word Length | | | | 1-Bit Data | | Bits |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| Input Logic Level | $V_{IH}$ | | 0.7 x $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IL}$ | | 0 | | 0.3 x $V_{DD}$ | |
| Output Logic Level | $V_{OH}$ | $I_{OH}$ = −2mA | 0.8 x $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{OL}$ | $I_{OH}$ = +2mA | 0 | | 0.2 x $V_{DD}$ | |
| Input Leakage Current(1) | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | | +1 | +10 | µA |
| | $I_{IL}$ | $V_{IN}$ = 0V | | −1 | −10 | µA |
| Input Leakage Current(2) | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | | +35 | +100 | µA |
| | $I_{IL}$ | $V_{IN}$ = 0V | | −35 | −100 | µA |
| **CLOCK FREQUENCIES** | | | | | | |
| System Clock Frequency, $f_{SCKI}$ | | Single Rate Sampling Mode | 6.144 | | 38.4 | MHz |
| | | Dual Rate Sampling Mode | 12.8 | | 38.4 | MHz |
| | | Quad Rate Sampling Mode | 12.8 | | 38.4 | MHz |
| Sampling Frequency, $f_S$ | | Single Rate Sampling Mode | 24 | | 54 | kHz |
| | | Dual Rate Sampling Mode | 54 | | 108 | kHz |
| | | Quad Rate Sampling Mode | 108 | | 216 | kHz |
| **ANALOG INPUTS** | | | | | | |
| Full Scale Input Voltage | | Differential Input | | 6.0 | | $V_{PP}$ |
| Average Input Impedance | | | | 3 | | kΩ |
| Common-mode Rejection | | | | 85 | | dB |
| **DC SPECIFICATIONS** | | | | | | |
| $V_{COM}$12, $V_{COM}$34 Output Voltage | | | | +2.5 | | V |
| $V_{COM}$12, $V_{COM}$34 Output Current | | | | 200 | | µA |

(1) Applies to the FMT0, FMT1, FMT2, S/$\overline{M}$, FS0, FS1, FS2, HPFD, BCK, LRCK, SUB, DSDCLK, DSD1, DSD2, DSD3, DSD4, and SCKI pins.
(2) Applies to the TEST and $\overline{RST}$ pins.
(3) Typical performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with either a 20kHz low-pass filter for $f_S$ = 48kHz or a 40kHz low-pass filter for $f_S$ = 96kHz and 192kHz. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filters already mentioned. The measurements are made with the RMS detector selected.
(4) A 256$f_S$ system clock is used at final production test for $f_S$ = 48kHz measurements.
(5) Typical DSD performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with a 20kHz low-pass filter. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filter already mentioned. The measurements are made with the RMS detector selected. The 1-bit DSD data is converted to 24-bit linear PCM data for measurement using a PCM4204 configured for DSD input mode.

## ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, all characteristics specified with $T_A$ = +25°C, $V_{CC}$ = +5V, $V_{DD}$ = +3.3V, system clock (SCKI) is 512$f_S$ for Single Rate Sampling, 256$f_S$ for Dual Rate Sampling, or 128$f_S$ for Quad Rate Sampling. The device is operated in Master mode for all dynamic performance measurements.

| PARAMETER | TEST CONDITIONS | PCM4204 MIN | PCM4204 TYP | PCM4204 MAX | UNIT |
|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE (PCM Output)(3)** | | | | | |
| $f_S$ = 48kHz(4) | | | | | |
| THD+N | $V_{IN}$ = −0.5dBFS, $f_{IN}$ = 1kHz | | −105 | −96 | dB |
| | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz | | −56 | | dB |
| Dynamic Range | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz, A-weighted | 112 | 118 | | dB |
| Channel Separation | | 105 | 120 | | dB |
| $f_S$ = 96kHz | | | | | |
| THD+N | $V_{IN}$ = −0.5dBFS, $f_{IN}$ = 1kHz, BW = 20Hz to 40kHz | | −103 | | dB |
| | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz, BW = 20Hz to 40kHz | | −52 | | dB |
| Dynamic Range | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz, A-weighted | | 118 | | dB |
| Channel Separation | | | 120 | | dB |
| $f_S$ = 192kHz | | | | | |
| THD+N | $V_{IN}$ = −0.5dBFS, $f_{IN}$ = 1kHz, BW = 20Hz to 40kHz | | −103 | | dB |
| Dynamic Range | $V_{IN}$ = 0V, Unweighted, BW = 20Hz to 40kHz | | 108 | | dB |
| | $V_{IN}$ = 0V, A-weighted | | 117 | | dB |
| Channel Separation | | | 120 | | dB |
| **DYNAMIC PERFORMANCE (DSD Output)(5)** | | | | | |
| 64$f_S$ Output Rate | DSDBCK = 2.8224MHz, BW = 20Hz to 20kHz | | | | |
| THD+N | $V_{IN}$ = −0.5dBFS, $f_{IN}$ = 1kHz | | −103 | | dB |
| | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz | | −52 | | dB |
| Dynamic Range | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz, A-weighted | | 115 | | dB |
| 128$f_S$ Output Rate | DSDBCK = 5.6448MHz, BW = 20Hz to 20kHz | | | | |
| THD+N | $V_{IN}$ = −0.5dBFS, $f_{IN}$ = 1kHz | | −105 | | dB |
| | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz | | −56 | | dB |
| Dynamic Range | $V_{IN}$ = −60dBFS, $f_{IN}$ = 1kHz, A-weighted | | 118 | | dB |
| **DIGITAL DECIMATION FILTER** | | | | | |
| Single and Dual Rate Sampling Modes | | | | | |
| Passband Edge | −0.005dB | | | 0.453$f_S$ | Hz |
| Passband Ripple | | | | ±0.005 | dB |
| Stop Band Edge | | 0.547$f_S$ | | | Hz |
| Stop Band Attenuation | | −100 | | | dB |
| Group Delay | | | 37/$f_S$ | | sec |

(1) Applies to the FMT0, FMT1, FMT2, S/$\overline{M}$, FS0, FS1, FS2, HPFD, BCK, LRCK, SUB, DSDCLK, DSD1, DSD2, DSD3, DSD4, and SCKI pins.
(2) Applies to the TEST and $\overline{RST}$ pins.
(3) Typical performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with either a 20kHz low-pass filter for $f_S$ = 48kHz or a 40kHz low-pass filter for $f_S$ = 96kHz and 192kHz. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filters already mentioned. The measurements are made with the RMS detector selected.
(4) A 256$f_S$ system clock is used at final production test for $f_S$ = 48kHz measurements.
(5) Typical DSD performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with a 20kHz low-pass filter. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filter already mentioned. The measurements are made with the RMS detector selected. The 1-bit DSD data is converted to 24-bit linear PCM data for measurement using a PCM4204 configured for DSD input mode.

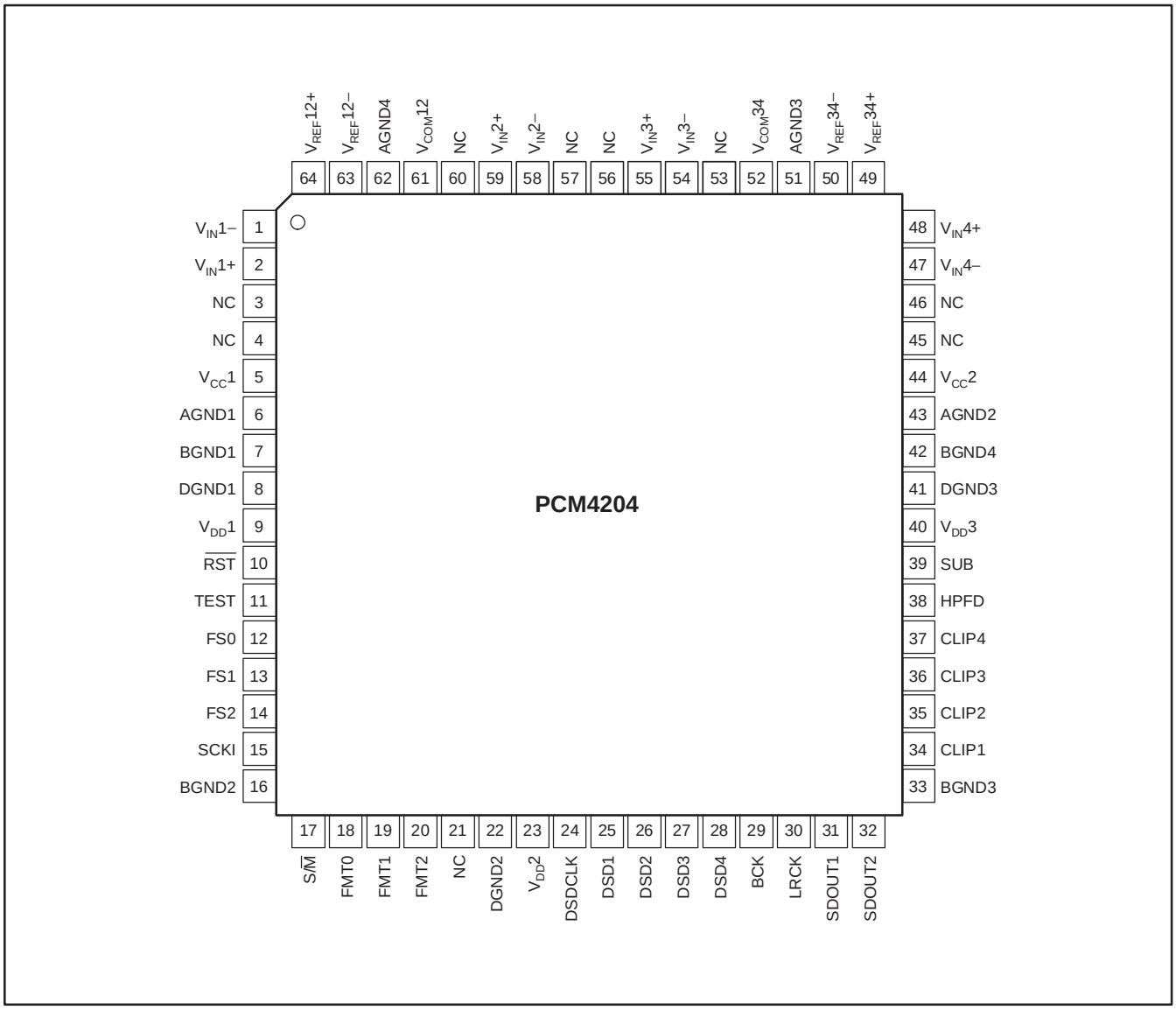
## ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, all characteristics specified with $T_A$ = +25°C, $V_{CC}$ = +5V, $V_{DD}$ = +3.3V, system clock (SCKI) is 512$f_S$ for Single Rate Sampling, 256$f_S$ for Dual Rate Sampling, or 128$f_S$ for Quad Rate Sampling. The device is operated in Master mode for all dynamic performance measurements.

| PARAMETER | TEST CONDITIONS | PCM4204 MIN | PCM4204 TYP | PCM4204 MAX | UNIT |
|---|---|---|---|---|---|
| **DIGITAL DECIMATION FILTER (continued)** | | | | | |
| Quad Rate Sampling Mode | | | | | |
| Passband Edge | −0.005dB | | | 0.375$f_S$ | Hz |
| | −3dB | | | 0.490$f_S$ | Hz |
| Passband Ripple | | | | ±0.005 | dB |
| Stop Band Edge | | 0.770$f_S$ | | | Hz |
| Stop Band Attenuation | | −135 | | | dB |
| Group Delay | | | 9.5/$f_S$ | | sec |
| **DIGITAL HIGH PASS FILTER** | | | | | |
| Frequency Response (−3dB) | | | $f_S$/48000 | | Hz |
| **POWER SUPPLY** | | | | | |
| Voltage Range | | | | | |
| $V_{CC}1$, $V_{CC}2$ | | +4.75 | +5.0 | +5.25 | VDC |
| $V_{DD}1$, $V_{DD}2$, $V_{DD}3$ | | +3.0 | +3.3 | +3.6 | VDC |
| Power Down Supply Current | $V_{CC}$ = +5V, $V_{DD}$ = +3.3V, $\overline{RST}$ = Low | | | | |
| $I_{CC}1 + I_{CC}2$ | | | | 10 | mA |
| $I_{DD}1 + I_{DD}2 + I_{DD}3$ | | | | 2 | mA |
| Quiescent Current $I_{CC}1 + I_{CC}2$ | $V_{CC}$ = +5.0V | | | | |
| | $f_S$ = 48kHz(4) | | 108 | 130 | mA |
| | $f_S$ = 96kHz | | 108 | 130 | mA |
| | $f_S$ = 192kHz | | 108 | 130 | mA |
| $I_{DD}1 + I_{DD}2 + I_{DD}3$ | $V_{DD}$ = +3.3V | | | | |
| | $f_S$ = 48kHz(4) | | 18 | 23 | mA |
| | $f_S$ = 96kHz | | 30 | 44 | mA |
| | $f_S$ = 192kHz | | 23 | 26 | mA |
| Total Power Dissipation | $V_{CC}$ = +5V, $V_{DD}$ = +3.3V | | | | |
| | $f_S$ = 48kHz(4) | | 600 | 726 | mW |
| | $f_S$ = 96kHz | | 640 | 795 | mW |
| | $f_S$ = 192kHz | | 615 | 736 | mW |

(1) Applies to the FMT0, FMT1, FMT2, S/$\overline{M}$, FS0, FS1, FS2, HPFD, BCK, LRCK, SUB, DSDCLK, DSD1, DSD2, DSD3, DSD4, and SCKI pins.
(2) Applies to the TEST and $\overline{RST}$ pins.
(3) Typical performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with either a 20kHz low-pass filter for $f_S$ = 48kHz or a 40kHz low-pass filter for $f_S$ = 96kHz and 192kHz. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filters already mentioned. The measurements are made with the RMS detector selected.
(4) A 256$f_S$ system clock is used at final production test for $f_S$ = 48kHz measurements.
(5) Typical DSD performance is measured using an Audio Precision System Two Cascade or Cascade Plus test system. The measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter in combination with a 20kHz low-pass filter. All A-weighted measurements are performed using the A-weighting filter in combination with the band limiting filter already mentioned. The measurements are made with the RMS detector selected. The 1-bit DSD data is converted to 24-bit linear PCM data for measurement using a PCM4204 configured for DSD input mode.

## PIN ASSIGNMENT



## Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| PIN NO. | NAME | | |
| 1 | $V_{IN}1-$ | Input | Channel 1 Analog Input, Inverting |
| 2 | $V_{IN}1+$ | Input | Channel 1 Analog Input, Non-inverting |
| 3 | NC | — | No Internal Connection |
| 4 | NC | — | No Internal Connection |
| 5 | $V_{CC}1$ | Power | Analog Supply, +5V Nominal |
| 6 | AGND1 | Ground | Analog Ground |
| 7 | BGND1 | Ground | Substrate Ground |
| 8 | DGND1 | Ground | Digital Ground |
| 9 | $V_{DD}1$ | Power | Digital Supply, +3.3V Nominal |
| 10 | $\overline{RST}$ | Input | Reset/Power Down (Active Low with internal pull-up to $V_{DD}1$) |
| 11 | TEST | Input | Test Pin (Active High with internal pull-down to DGND) |
| 12 | FS0 | Input | Sampling Mode |
| 13 | FS1 | Input | Sampling Mode |
| 14 | FS2 | Input | Sampling Mode |
| 15 | SCKI | Input | System Clock |
| 16 | BGND2 | Ground | Substrate Ground |
| 17 | S/$\overline{M}$ | Input | Audio Serial Port Slave/Master Mode (0 = Master, 1 = Slave) |
| 18 | FMT0 | Input | Audio Data Format |
| 19 | FMT1 | Input | Audio Data Format |
| 20 | FMT2 | Input | Audio Data Format |
| 21 | NC | — | No Internal Connection |
| 22 | DGND2 | Ground | Digital Ground |
| 23 | $V_{DD}2$ | Power | Digital Supply, +3.3V Nominal |
| 24 | DSDCLK | I/O | DSD Data Clock |
| 25 | DSD1 | I/O | Channel 1 DSD Data |
| 26 | DSD2 | I/O | Channel 2 DSD Data |
| 27 | DSD3 | I/O | Channel 3 DSD Data |
| 28 | DSD4 | I/O | Channel 4 DSD Data |
| 29 | BCK | I/O | Audio Serial Port Bit Clock |
| 30 | LRCK | I/O | Audio Serial Port Left/Right (or Word) Clock |
| 31 | SDOUT1 | Output | PCM Data for Channels 1 and 2(1) |
| 32 | SDOUT2 | Output | PCM Data for Channels 3 and 4(1) |
| 33 | BGND3 | Ground | Substrate Ground |
| 34 | CLIP1 | Output | Channel 1 Clipping Flag (Active High) |
| 35 | CLIP2 | Output | Channel 2 Clipping Flag (Active High) |
| 36 | CLIP3 | Output | Channel 3 Clipping Flag (Active High) |
| 37 | CLIP4 | Output | Channel 4 Clipping Flag (Active High) |
| 38 | HPFD | Input | High-Pass Filter Disable (Active High) |
| 39 | SUB | Input | TDM Sub-Frame Assignment (0 = SF 0, 1 = SF 1) |
| 40 | $V_{DD}3$ | Power | Digital Supply, +3.3V Nominal |

(1) For TDM formats, SDOUT1 carries data for all four channels, while SDOUT2 is driven low.

## Terminal Functions (continued)

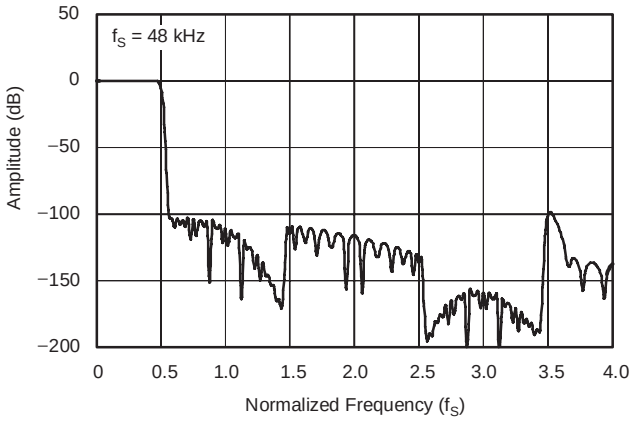
| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| PIN NO. | NAME | | |
| 41 | DGND3 | Ground | Digital Ground |
| 42 | BGND4 | Ground | Substrate Ground |
| 43 | AGND2 | Ground | Analog Ground |
| 44 | $V_{CC}2$ | Power | Analog Supply, +5V Nominal |
| 45 | NC | — | No Internal Connection |
| 46 | NC | — | No Internal Connection |
| 47 | $V_{IN}4-$ | Input | Channel 4 Analog Input, Inverting |
| 48 | $V_{IN}4+$ | Input | Channel 4 Analog Input, Non-inverting |
| 49 | $V_{REF}34+$ | Output | Voltage Reference De-Coupling for Channels 3 and 4 |
| 50 | $V_{REF}34-$ | Output | Reference Ground for Channels 3 and 4, connect to AGND |
| 51 | AGND3 | Output | Analog Ground |
| 52 | $V_{COM}34$ | Output | Common-mode Voltage for Channels 3 and 4, +2.5V Nominal |
| 53 | NC | — | No Internal Connection |
| 54 | $V_{IN}3-$ | Input | Channel 3 Analog Input, Inverting |
| 55 | $V_{IN}3+$ | Input | Channel 3 Analog Input, Non-inverting |
| 56 | NC | — | No Internal Connection |
| 57 | NC | — | No Internal Connection |
| 58 | $V_{IN}2-$ | Input | Channel 2 Analog Input, Inverting |
| 59 | $V_{IN}2+$ | Input | Channel 2 analog Input, Non-inverting |
| 60 | NC | — | No Internal Connection |
| 61 | $V_{COM}12$ | Output | Common-mode Voltage for Channels 1 and 2, +2.5V Nominal |
| 62 | AGND4 | Ground | Analog Ground |
| 63 | $V_{REF}12-$ | Output | Reference Ground for Channels 1 and 2, connect to AGND |
| 64 | $V_{REF}12+$ | Output | Voltage Reference De-Coupling for Channels 1 and 2 |

(1) For TDM formats, SDOUT1 carries data for all four channels, while SDOUT2 is driven low.

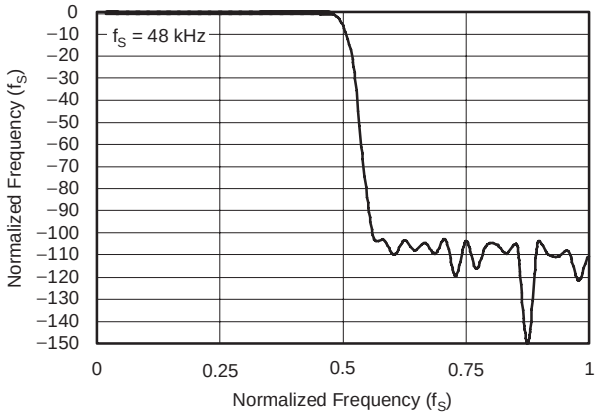
## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C with $V_{CC}$ = +5V, VDD = +3.3V, and a measurement bandwidth from 20Hz to 20kHz, unless otherwise noted.

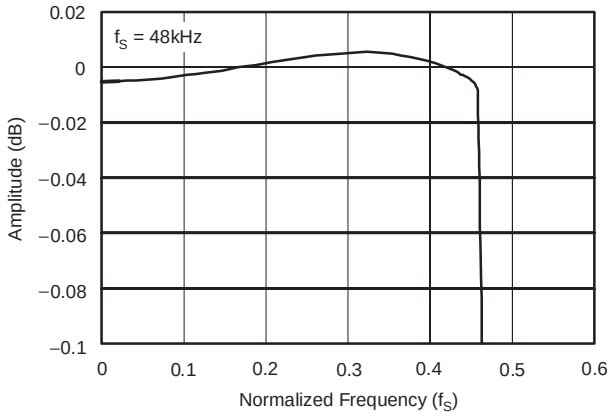
OVERALL CHARACTERISTICS
SINGLE RATE FILTER



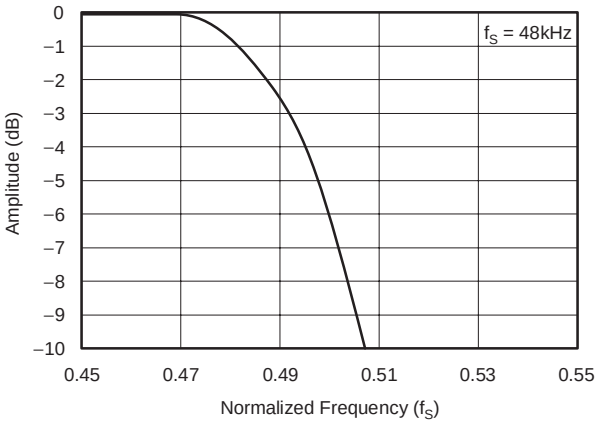

STOP BAND ATTENUATION CHARACTERISTICS
SINGLE RATE FILTER



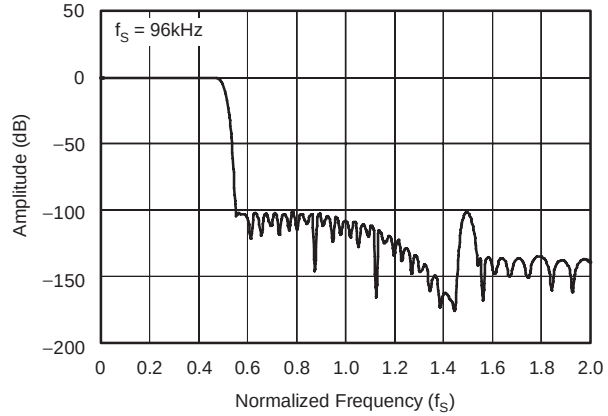

PASSBAND RIPPLE CHARACTERISTICS
SINGLE RATE FILTER



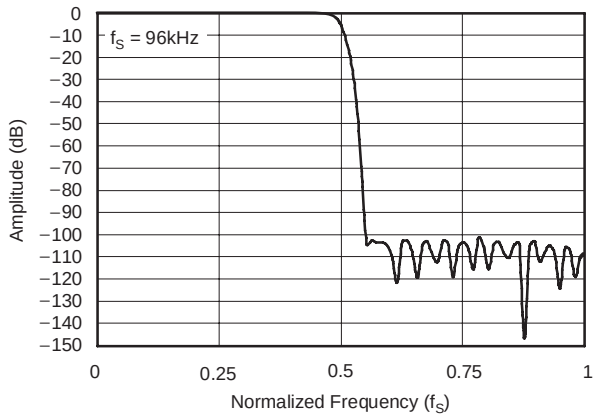

TRANSIENT BAND CHARACTERISTICS
SINGLE RATE FILTER




OVERALL CHARACTERISTICS
DUAL RATE FILTER



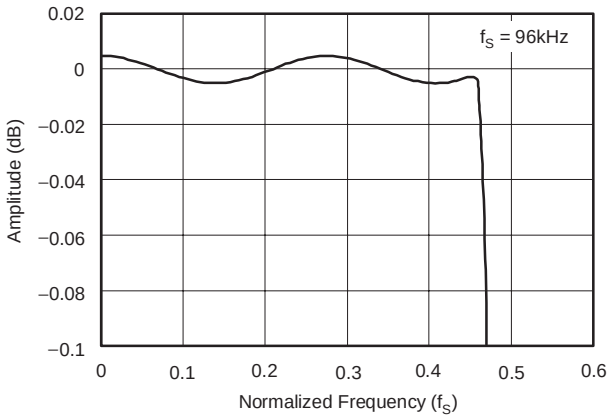

STOP BAND ATTENUATION CHARACTERISTICS
DUAL RATE FILTER



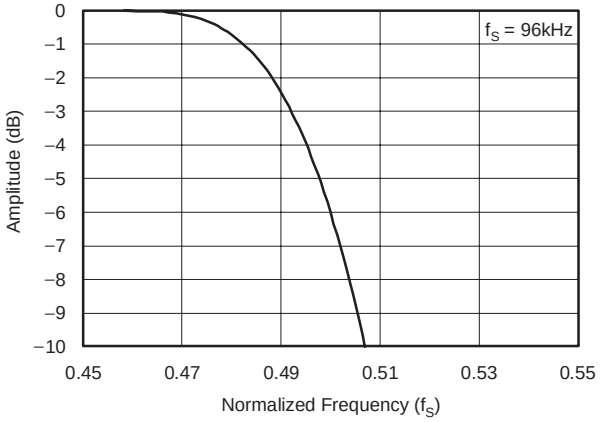
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C with $V_{CC}$ = +5V, VDD = +3.3V, and a measurement bandwidth from 20Hz to 20kHz, unless otherwise noted.

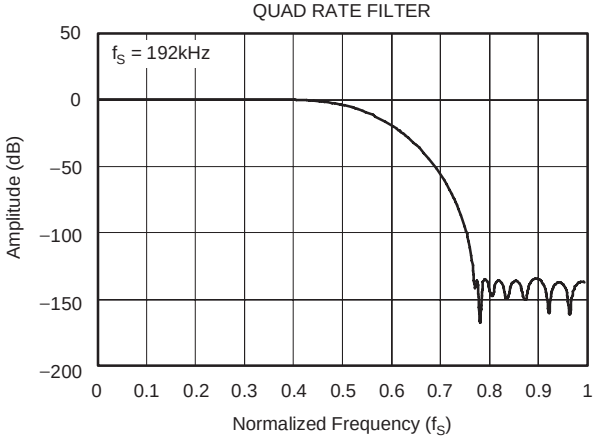
PASSBAND RIPPLE CHARACTERISTICS
DUAL RATE FILTER



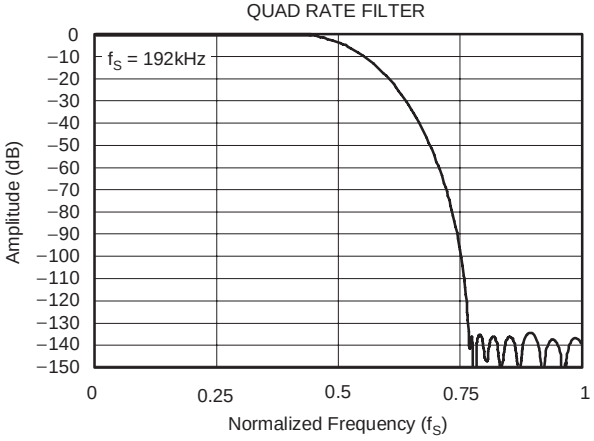

TRANSIENT BAND CHARACTERISTICS
DUAL RATE FILTER



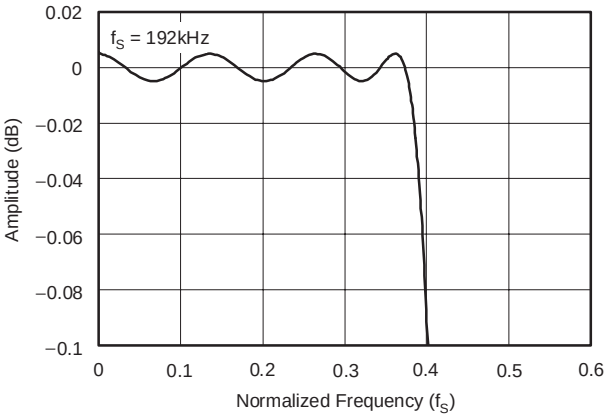

OVERALL CHARACTERISTICS
QUAD RATE FILTER



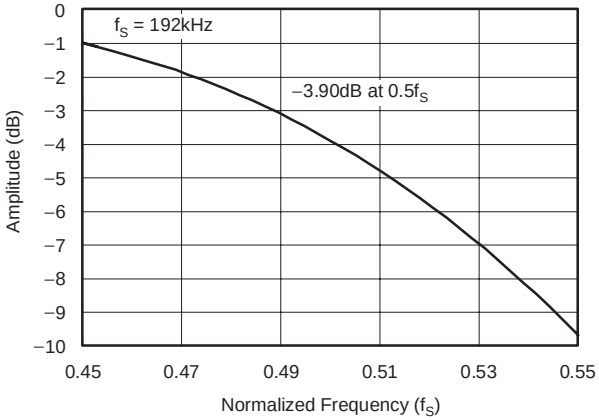

STOP BAND ATTENUATION CHARACTERISTICS
QUAD RATE FILTER




PASSBAND RIPPLE CHARACTERISTICS
QUAD RATE FILTER



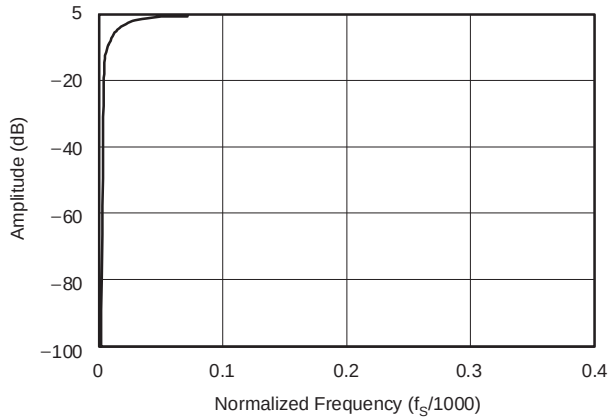

TRANSIENT BAND CHARACTERISTICS
QUAD RATE FILTER



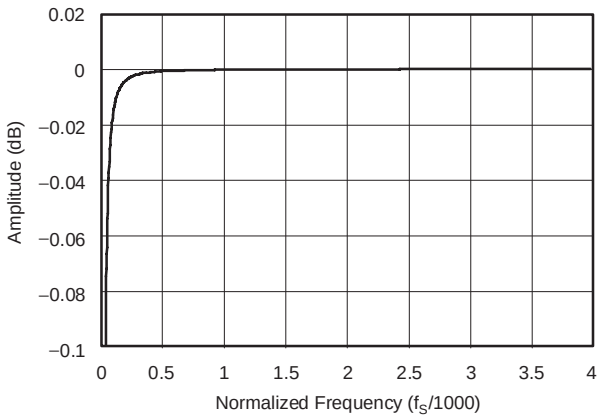
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C with $V_{CC}$ = +5V, VDD = +3.3V, and a measurement bandwidth from 20Hz to 20kHz, unless otherwise noted.

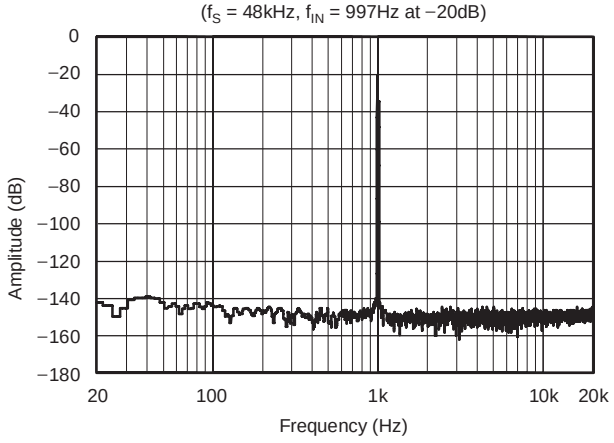
HIGH PASS FILTER
STOP BAND CHARACTERISTICS



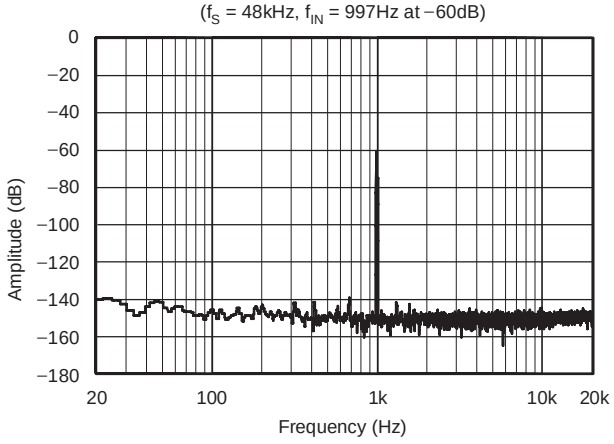

HIGH PASS FILTER
PASSBAND CHARACTERISTICS



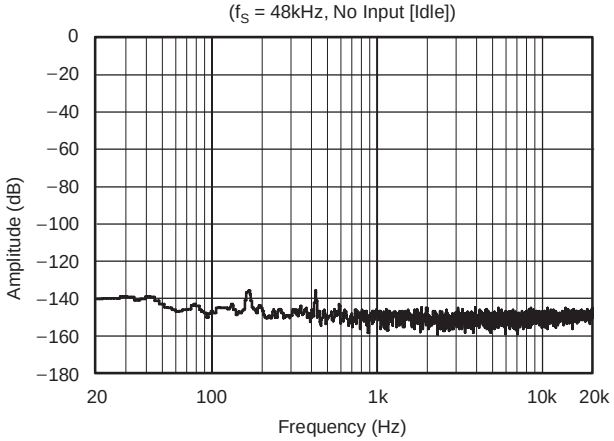

FFT PLOT
($f_S$ = 48kHz, $f_{IN}$ = 997Hz at −20dB)



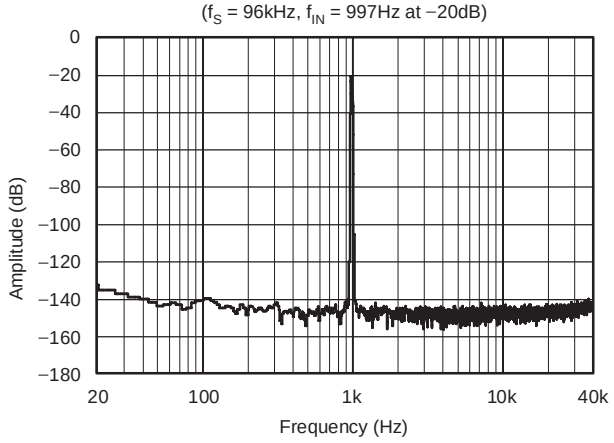

FFT PLOT
($f_S$ = 48kHz, $f_{IN}$ = 997Hz at −60dB)




FFT PLOT
($f_S$ = 48kHz, No Input [Idle])



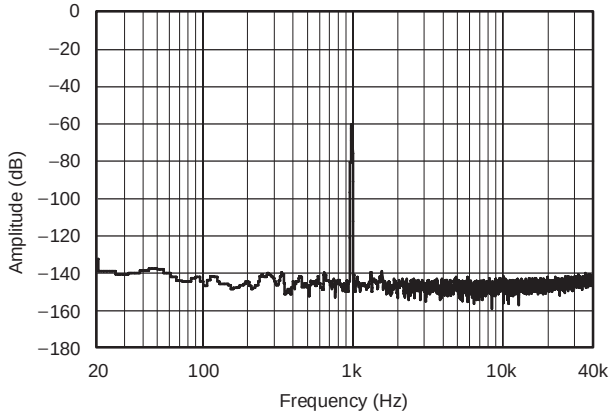

FFT PLOT
($f_S$ = 96kHz, $f_{IN}$ = 997Hz at −20dB)



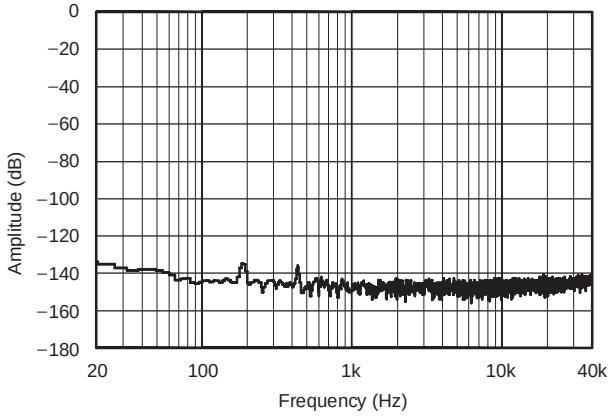
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C with $V_{CC}$ = +5V, VDD = +3.3V, and a measurement bandwidth from 20Hz to 20kHz, unless otherwise noted.

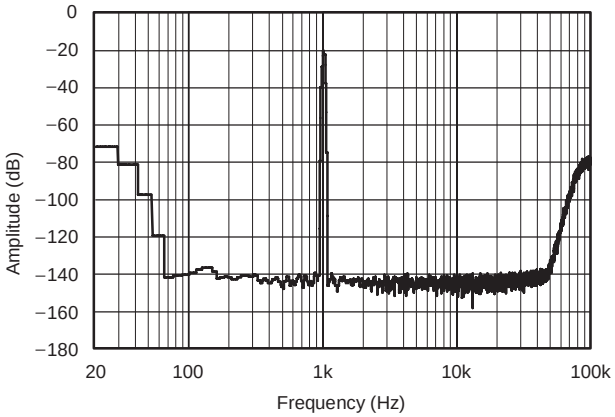
FFT PLOT
($f_S$ = 96kHz, $f_{IN}$ = 997Hz at −60dB)



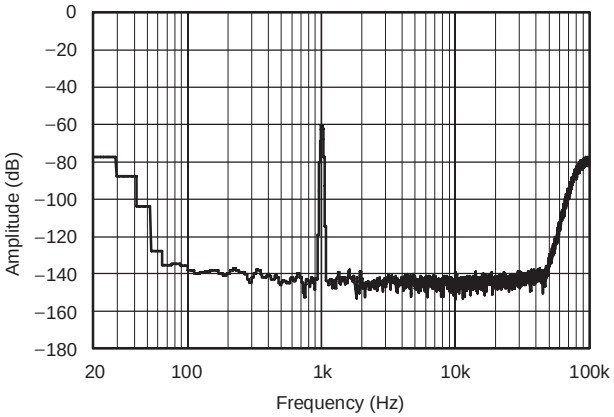

FFT PLOT
($f_S$ = 96kHz, No Input [Idle])



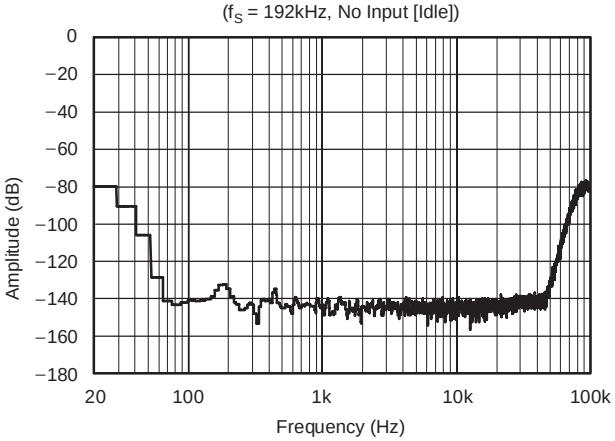

FFT PLOT
($f_S$ = 192kHz, $f_{IN}$ = 997Hz at −20dB)



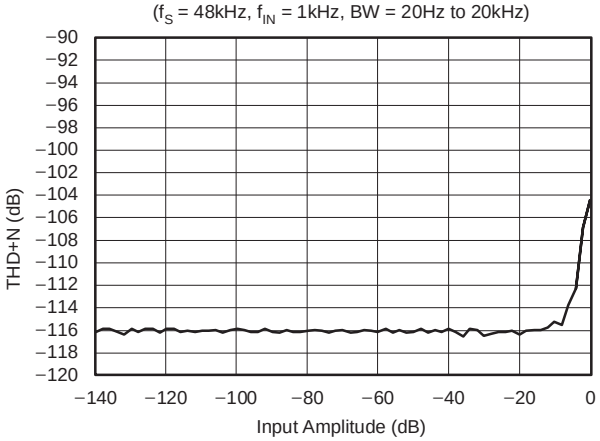

FFT PLOT
($f_S$ = 192kHz, $f_{IN}$ = 997Hz at −60dB)




FFT PLOT
($f_S$ = 192kHz, No Input [Idle])



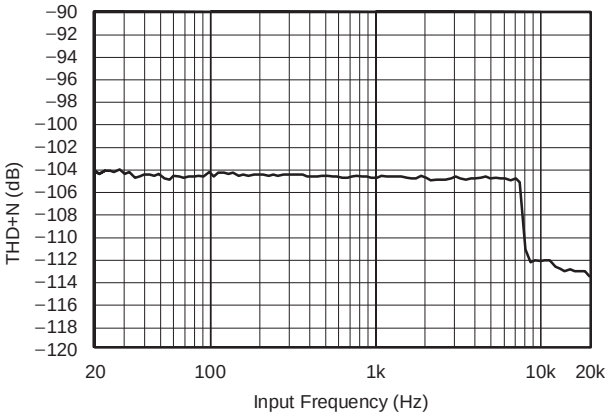

THD+N vs AMPLITUDE
($f_S$ = 48kHz, $f_{IN}$ = 1kHz, BW = 20Hz to 20kHz)



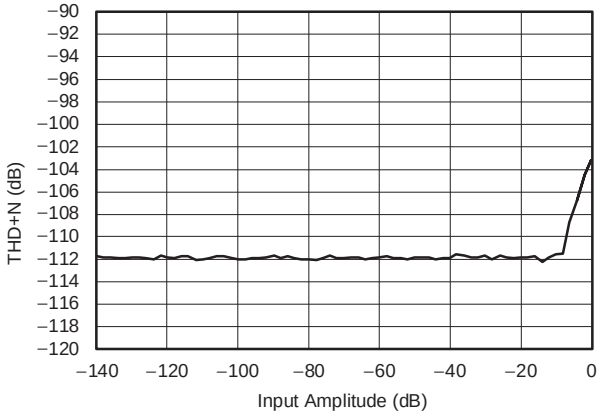
## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C with $V_{CC}$ = +5V, VDD = +3.3V, and a measurement bandwidth from 20Hz to 20kHz, unless otherwise noted.

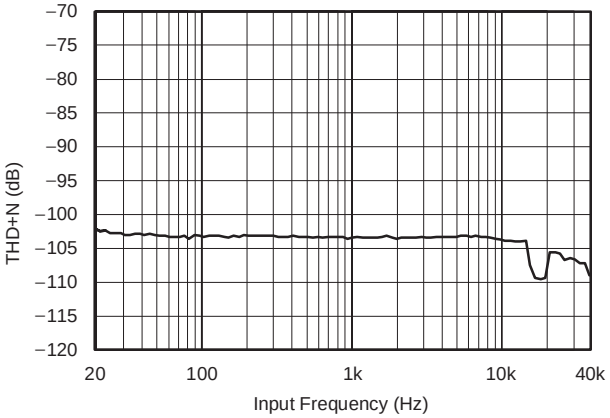
THD+N vs FREQUENCY
($f_S$ = 48kHz, Input Amplitude = −1dB,
BW = 20Hz to 20kHz)



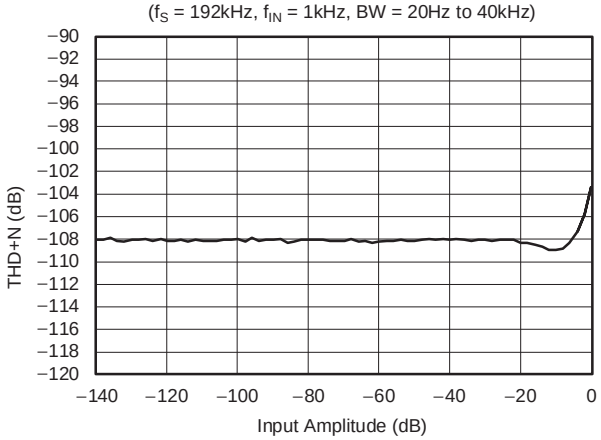

THD+N vs AMPLITUDE
($f_S$ = 96kHz, $f_{IN}$ = 1kHz, BW = 20Hz to 40kHz)



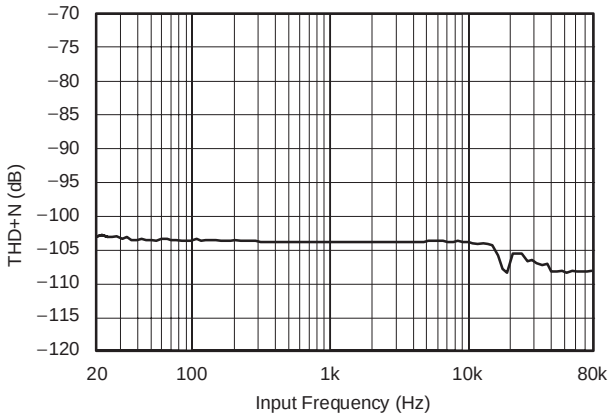

THD+N vs FREQUENCY
($f_S$ = 96kHz, Input Amplitude = −1dB,
BW = 20Hz to 40kHz)




THD+N vs AMPLITUDE
($f_S$ = 192kHz, $f_{IN}$ = 1kHz, BW = 20Hz to 40kHz)




THD+N vs FREQUENCY
($f_S$ = 192kHz, Input Amplitude = −1dB,
BW = 20Hz to 40kHz)



## PRODUCT OVERVIEW

The PCM4204 is a high-performance, four-channel audio analog-to-digital (A/D) converter designed for use in professional and broadcast audio applications. The PCM4204 features 24-bit linear PCM data outputs, as well as 1-bit Direct Stream Digital (DSD) data output and input capability for all four channels. Sampling rates up to 216kHz are supported for PCM output formats, while 64x or 128x oversampled 1-bit data is supported for DSD modes. Native support for both PCM and DSD data formats makes the PCM4204 ideal for use in a wide variety of audio recording and processing applications.

The PCM4204 features 1-bit delta sigma modulators employing density modulated dither for improved dynamic performance. Differential voltage inputs are utilized for the modulators, providing excellent common-mode rejection. On-chip voltage references are provided for the modulators, in addition to generating DC common-mode bias voltage outputs for use with external input circuitry. Linear phase digital decimation filtering is provided for the 24-bit PCM output, with a minimum stop band attenuation of −100dB for all sampling modes.

The PCM output mode features clipping flag outputs for each of the four channels, as well as a digital high-pass filter for DC removal. The PCM4204 may be configured using dedicated input pins for sampling mode and audio data format selection, high-pass filter enable/disable, and reset/power-down operation.

A +5V power supply is required for the analog section of the device, while a +3.3V power supply is required for the digital circuitry. Figure 1 shows the functional block diagram for the PCM4204.

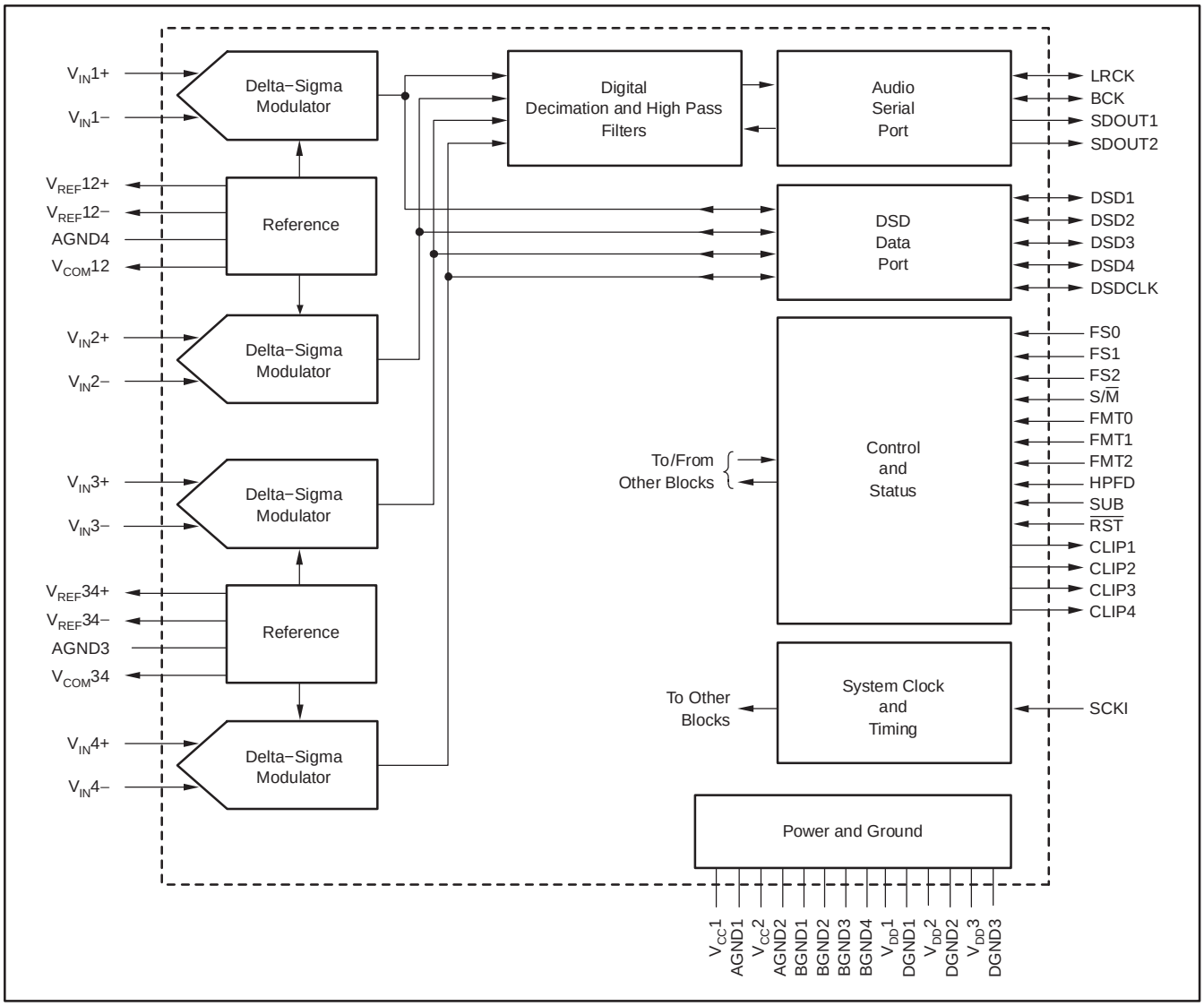



**Figure 1. PCM4204 Functional Block Diagram**

## ANALOG INPUTS

The PCM4204 includes four channels of A/D conversion, each with its own pair of differential voltage input pins. The $V_{IN}1-$ (pin 1) and $V_{IN}1+$ (pin 2) analog inputs correspond to Channel 1. The $V_{IN}2-$ (pin 58) and $V_{IN}2+$ (pin 59) analog inputs correspond to Channel 2. The $V_{IN}3-$ (pin 54) and $V_{IN}3+$ (pin 55) analog inputs correspond to Channel 3. The $V_{IN}4-$ (pin 47) and $V_{IN}4+$ (pin 48) analog inputs correspond to Channel 4. The average input impedance of each input pin is 3.0kΩ.

Each analog input pair accepts a full-scale input voltage of approximately $6.0V_{PP}$ differential. The analog input should not swing below analog ground or above the $V_{CC}1$ (pin 5) or $V_{CC}2$ (pin 44) power supplies by more than 300mV. Schottky diodes may be used to clamp these pins to a safe input range, or the input buffer circuitry may be designed in a manner to ensure that the input swing does not exceed the absolute maximum ratings of the PCM4204. Refer to the ***Applications Information*** section of this datasheet for an example input buffer circuit.

## VOLTAGE REFERENCES AND COMMON MODE BIAS VOLTAGE OUTPUTS

The PCM4204 includes two on-chip voltage references, one for Channels 1 and 2 and another for Channels 3 and 4. The $V_{REF}12-$ (pin 63) and $V_{REF}12+$ (pin 64) outputs correspond to low and high reference outputs for Channels 1 and 2. The $V_{REF}34-$ (pin 50) and $V_{REF}34+$ (pin 49) outputs correspond to low and high reference outputs for Channels 3 and 4. De-coupling capacitors are connected between the high and low reference pins, and the low reference pin is then connected to an analog ground. It is recommended to have at least a 0.1μF X7R ceramic chip capacitor connected in parallel with a 33μF low ESR capacitor (tantalum, multilayer ceramic, or aluminum electrolytic) for de-coupling purposes.

Refer to the ***Applications Information*** section of this datasheet for the recommended voltage reference pin connections.

The $V_{REF}12+$ and $V_{REF}34+$ outputs should not be utilized to bias external circuitry, as they are not buffered. Use the $V_{COM}12$ (pin 16) and $V_{COM}34$ (pin 52) outputs to bias external circuitry. Although the $V_{COM}L$ and $V_{COM}R$ outputs are internally buffered, the output current is limited to a few hundred μA. It is recommended to connect these pins to external nodes with greater than 1MΩ impedance, or to buffer the outputs with a voltage follower circuit when driving multiple external nodes.

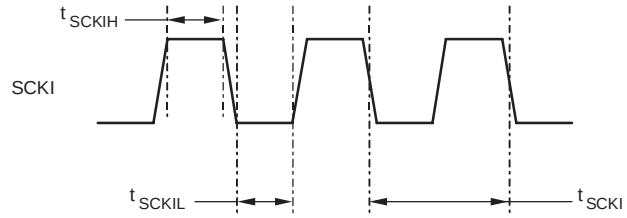
Refer to the ***Applications Information*** section of this datasheet for an example input buffer circuit that utilizes the common-mode bias voltage outputs.

## SYSTEM CLOCK INPUT

The PCM4204 requires a system clock, from which the modulator oversampling and digital sub-system clocks are derived. The system clock is applied at the SCKI input (pin 15). The frequency of the system clock is dependent upon the desired PCM output sampling frequency or DSD data rate, along with the sampling mode selection. Table 1 shows the corresponding system clock frequencies for common output sampling and data rates, along with the corresponding sampling modes. Timing requirements for the system clock are shown in Figure 2.

**Table 1. System Clock Frequencies for Common Output Sampling and Data Rates**

| SAMPLING MODE | SAMPLING FREQUENCY, $f_S$ (kHz) | SYSTEM CLOCK FREQUENCY (MHz) | | | | | |
|---|---|---|---|---|---|---|---|
| | | $128f_S$ | $192f_S$ | $256f_S$ | $384f_S$ | $512f_S$ | $768f_S$ |
| Single Rate | 32 | n/a | n/a | 8.192 | 12.288 | 16.384 | 24.576 |
| Single Rate | 44.1 | n/a | n/a | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| Single Rate | 48 | n/a | n/a | 12.288 | 18.432 | 24.576 | 36.864 |
| Dual Rate | 88.2 | n/a | n/a | 22.5792 | 33.8688 | n/a | n/a |
| Dual Rate | 96 | n/a | n/a | 24.576 | 36.864 | n/a | n/a |
| Quad Rate | 176.4 | 22.5792 | 33.8688 | n/a | n/a | n/a | n/a |
| Quad Rate | 192 | 24.576 | 36.864 | n/a | n/a | n/a | n/a |
| DSD Input/Output | $128f_S$ Data (Single Rate) | n/a | n/a | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| DSD Input/Output | $64f_S$ Data (Dual Rate) | n/a | n/a | 11.2896 | 16.9344 | n/a | n/a |




| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{SCKI}$ | System Clock Period | 26 | | ns |
| $t_{SCKIH}$ | System Clock High Pulse Time | 12 | | ns |
| $t_{SCKIL}$ | System Clock Low Pulse Time | 12 | | ns |

**Figure 2. System Clock Timing Requirements**

## SAMPLING MODES

The PCM4204 may be operated in one of three PCM sampling modes, or at one of two DSD output data rates. The PCM sampling modes are referred to as Single Rate, Dual Rate, and Quad Rate.

Single Rate mode is utilized for sampling rates up to 54kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 128 times the desired output sampling rate.

Dual Rate mode is utilized for sampling rates higher than 54kHz and up to 108kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 64 times the desired output sampling rate.

Quad Rate mode is utilized for sampling frequencies higher than 108kHz and up to 216kHz. The delta-sigma modulator oversamples the analog input signal by a rate equal to 32 times the desired output sampling rate.

For DSD output data, the user may select either $64f_S$ or $128f_S$ oversampled data rates, where $f_S$ is the base sampling rate, which is 44.1kHz for Super Audio CD (SACD) applications. The $64f_S$ data rate is analogous to the Dual Rate PCM sampling mode, where the analog input signal is oversampled by a rate equal to 64 times the base sampling rate. The $128f_S$ data rate corresponds to the Single Rate PCM sampling mode, where the analog input signal is oversampled by a rate equal to 128 times the base sampling rate. For DSD input data, the rate of the data must be known in order to configure the digital decimation filter for either 1/64 or 1/128 operation.

Table 1 indicates the sampling mode utilized for common system clock and sampling rate combinations. The FS0 (pin 12), FS1 (pin 13), and FS2 (pin 14) inputs are utilized to select the sampling mode for the PCM4204. If the state of the sampling mode pins is changed any time after power-up reset initialization, the user should issue an external forced reset to re-initialize the PCM4204. Table 2, Table 3, Table 4, and Table 5 indicate the sampling mode selections for PCM Master and Slave mode operation, as well as the DSD Output and Input mode operation.

**Table 2. Sampling Mode Selection for PCM Master Mode Operation**

| FS2 | FS1 | FS0 | SAMPLING MODE WITH SYSTEM CLOCK RATE |
|---|---|---|---|
| 0 | 0 | 0 | Single Rate with $f_{SCKI} = 768f_S$ |
| 0 | 0 | 1 | Single Rate with $f_{SCKI} = 512f_S$ |
| 0 | 1 | 0 | Single Rate with $f_{SCKI} = 384f_S$ |
| 0 | 1 | 1 | Single Rate with $f_{SCKI} = 256f_S$ |
| 1 | 0 | 0 | Dual Rate with $f_{SCKI} = 384f_S$ |
| 1 | 0 | 1 | Dual Rate with $f_{SCKI} = 256f_S$ |
| 1 | 1 | 0 | Quad Rate with $f_{SCKI} = 192f_S$ |
| 1 | 1 | 1 | Quad Rate with $f_{SCKI} = 128f_S$ |

**Table 3. Sampling Mode Selection for PCM Slave Mode Operation**

| FS2 | FS1 | FS0 | SAMPLING MODE |
|---|---|---|---|
| 0 | 0 | 0 | Single Rate with Clock Auto-Detection |
| 0 | 0 | 1 | Dual Rate with Clock Auto-Detection |
| 0 | 1 | 0 | Quad Rate with Clock Auto-Detection |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Table 4. Sampling Mode Selection for DSD Output Mode Operation**

| FS2 | FS1 | FS0 | SAMPLING MODE |
|---|---|---|---|
| 0 | 0 | 0 | $128f_S$ DSD Output Rate with $f_{SCKI} = 768f_S$ |
| 0 | 0 | 1 | $128f_S$ DSD Output Rate with $f_{SCKI} = 512f_S$ |
| 0 | 1 | 0 | $128f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$ |
| 0 | 1 | 1 | $128f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$ |
| 1 | 0 | 0 | $64f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$ |
| 1 | 0 | 1 | $64f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$ |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Table 5. Sampling Mode Selection for DSD Input Mode Operation**

| FS2 | FS1 | FS0 | SAMPLING MODE |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | $128f_S$ DSD Output Rate with $f_{SCKI} = 512f_S$ |
| 0 | 1 | 0 | $128f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$ |
| 0 | 1 | 1 | $128f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$ |
| 1 | 0 | 0 | $64f_S$ DSD Output Rate with $f_{SCKI} = 384f_S$ |
| 1 | 0 | 1 | $64f_S$ DSD Output Rate with $f_{SCKI} = 256f_S$ |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

## AUDIO DATA FORMATS

As mentioned previously, the PCM4204 supports 24-bit linear PCM output data, as well as 1-bit DSD output data. The available data formats are dependent upon whether the PCM4204 is configured in Slave or Master mode. The S/$\overline{M}$ (pin 17), FMT0 (pin 18), FMT1 (pin 19), and FMT2 (pin 20) inputs are utilized to select either Slave or Master mode and the corresponding audio data format.

In Slave mode, the PCM bit and left/right word clocks (BCK and LRCK) are configured as input pins. DSD data formats are not supported in Slave mode. Slave mode supports commonly used PCM audio data formats, including Left-Justified, Right-Justified, and Philips $I^2S$. Time division multiplexed (TDM) data formats are also supported, allowing up to two PCM4204 devices to be cascaded on a single audio serial bus. Table 6 summarizes the corresponding Slave mode data format selections.

In Master mode, the PCM bit and left/right clocks (BCK and LRCK respectively) are configured as output pins, and are derived from the system clock input (SCKI). For the DSD data and clock pins (DSD1, DSD2, DSD3, DSD4, and DSDCLK), they may be configured as either inputs or outputs, depending upon the DSD format selection. Table 7 summarizes the corresponding Master mode data format selections.

Figure 3, Figure 4, and Figure 5 illustrate the PCM and DSD data formats supported by the PCM4204.

**Table 6. Slave Mode Audio Data Format Selection**

| S/$\overline{M}$ | FMT2 | FMT1 | FMT0 | AUDIO DATA FORMAT |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 24-bit Left-Justified |
| 1 | 0 | 0 | 1 | 24-bit $I^2S$ |
| 1 | 0 | 1 | 0 | 24-bit Right-Justified |
| 1 | 0 | 1 | 1 | TDM with No BCK Delay for Start of Frame |
| 1 | 1 | 0 | 0 | TDM with One BCK Delay for Start of Frame |
| 1 | 1 | 0 | 1 | Reserved |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

**Table 7. Master Mode Audio Data Format Selection**

| S/$\overline{M}$ | FMT2 | FMT1 | FMT0 | AUDIO DATA FORMAT |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 24-bit Left-Justified |
| 0 | 0 | 0 | 1 | 24-bit $I^2S$ |
| 0 | 0 | 1 | 0 | 24-bit Right-Justified |
| 0 | 0 | 1 | 1 | DSD Output with PCM Output Disabled |
| 0 | 1 | 0 | 0 | DSD Input with 24−Bit Right-Justified PCM Output |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |

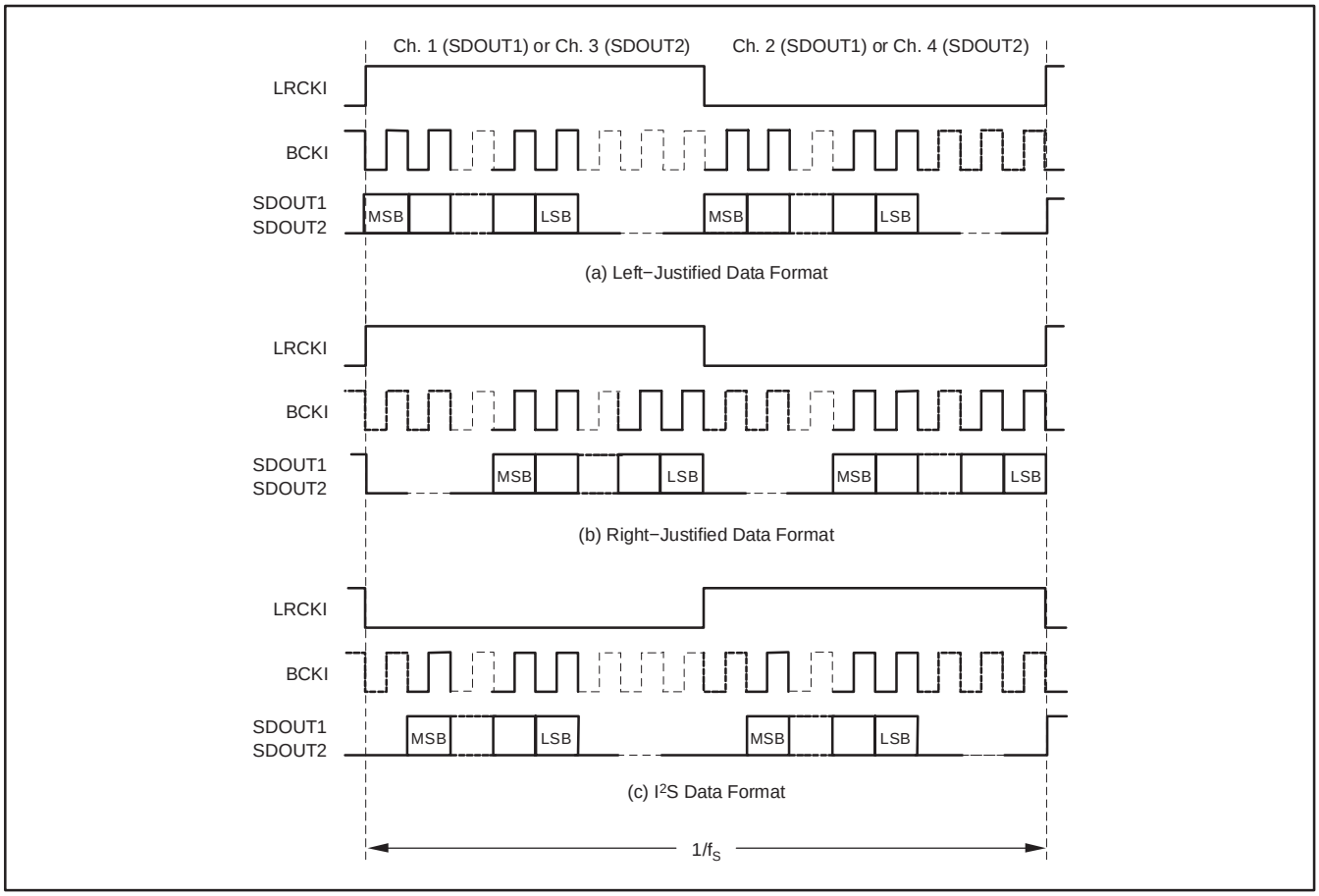



**Figure 3. PCM Data Formats: Left-Justified, Right-Justified, and Philips I²S**

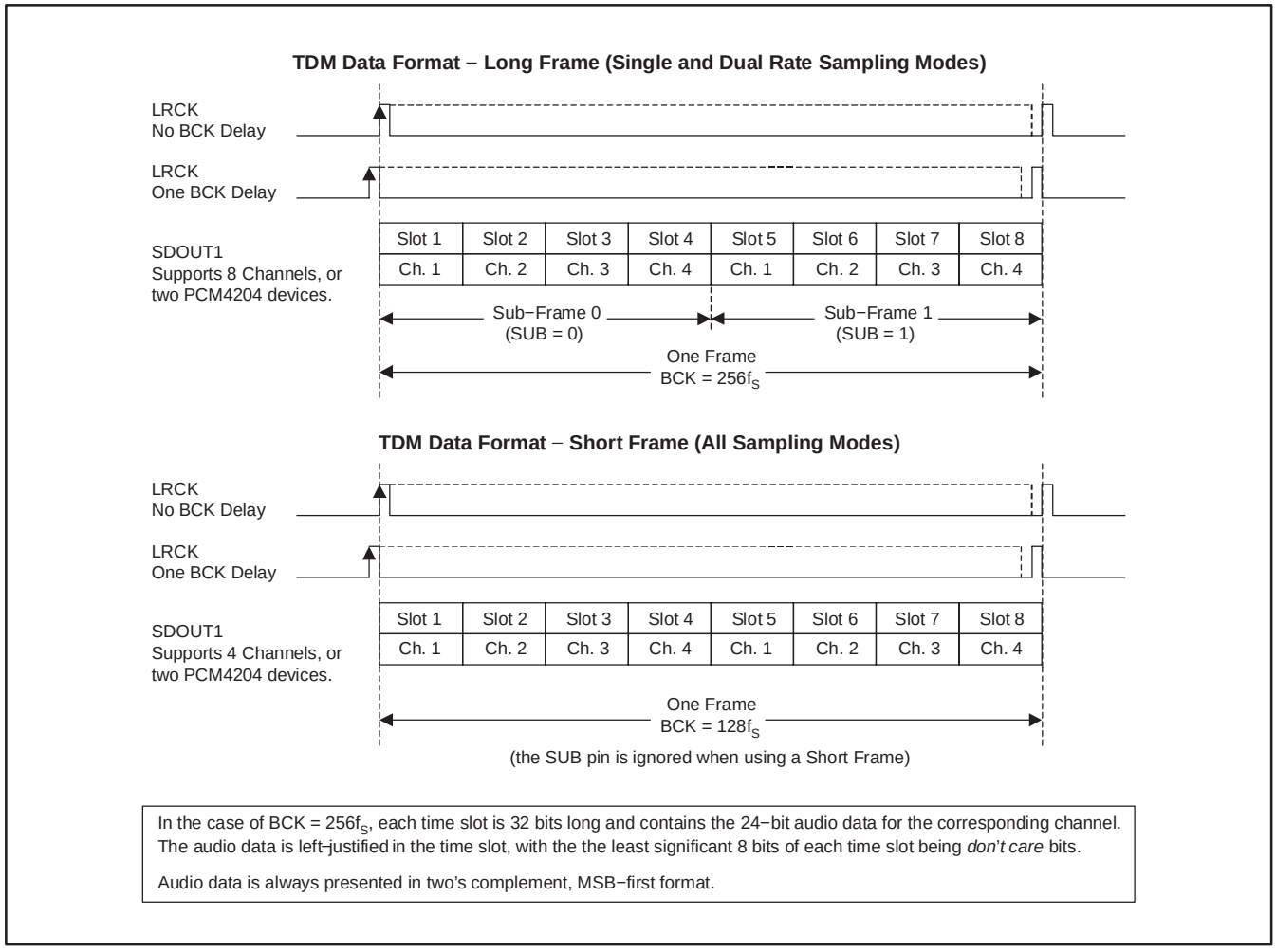



**Figure 4. PCM Data Formats: Time Division Multiplexed (TDM)**

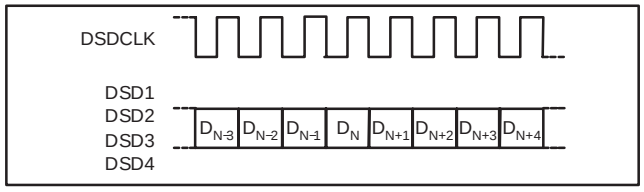



**Figure 5. DSD Input and Output Data Format**

## AUDIO SERIAL PORT OPERATION

This section provides additional details regarding the PCM4204 audio serial port, utilized for 24-bit linear PCM output data. The serial port is comprised of four signals: BCK (pin 29), LRCK (pin 30), SDOUT1 (pin 31), and SDOUT2 (pin 32). The BCK signal functions as the data (or bit) clock for the serial audio data. The LRCK is the left/right word or TDM frame synchronization clock for the audio serial port. The LRCK and BCK clocks must be synchronous. The SDOUT1 and SDOUT2 signals are the serial audio data outputs, with data being clocked out on the falling edge of the BCK clock. SDOUT1 carries data for Channels 1 and 2 when using Left-Justified, Right-Justified, or $I^2S$ data formats. SDOUT1 carries data for all four channels when using TDM data formats. SDOUT2 carries data for Channels 3 and 4 when using Left-Justified, Right-Justified, or $I^2S$ data formats. SDOUT2 is forced low when using TDM data formats.

As mentioned in the Audio Data Format section of this datasheet, the audio serial port can operate in Master or Slave mode. In Master mode, the BCK and LRCK clock signals are outputs, derived from the system clock input, SCKI. The BCK clock is fixed at $128f_S$ for Single Rate sampling mode, and at $64f_S$ for Dual or Quad Rate sampling modes. The LRCK clock operates at $f_S$, the output sampling rate (that is, 48kHz, 96kHz, etc.).

In Slave mode, the BCK and LRCK signals are inputs, with the clocks being generated by a master timing source, such as a DSP serial port, PLL clock synthesizer, or a crystal oscillator/divider circuit. For Left Justified, Right Justified, and $I^2S$ data formats, the BCK rate is typically $128f_S$ in Single Rate sampling mode, and $64f_S$ in Dual or Quad Rate sampling modes. Although other BCK clock rates are possible, they are not recommended due to the potential for clock phase sensitivity issues, which may degrade the dynamic performance of the PCM4204. The LRCK clock operates at $f_S$, the output sampling rate.

Figure 6 illustrates the typical audio serial port connections between a PCM4204 and an audio signal processor when using Left-Justified, Right-Justified, and $I^2S$ data formats in either Slave or Master modes.

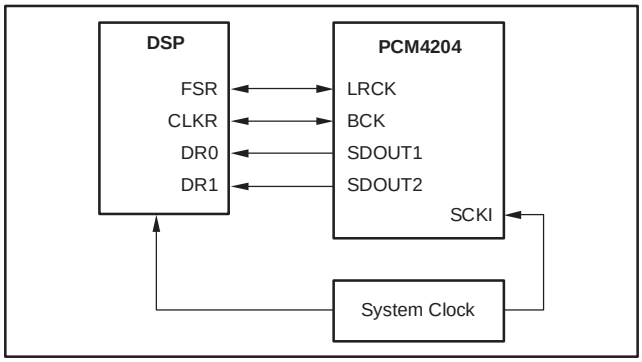



**Figure 6. Typical Audio Serial Port Connections for Left-Justified, Right-Justified, and Philips $I^2S$ Data Formats**

In Slave mode, the TDM data formats support a BCK clock rate of $256f_S$ for Long Frame operation, and $128f_S$ for Short Frame operation. The length and rate of the TDM frame is auto−detected by the audio serial port. Long Frame operation is supported for Single and Dual rate sampling modes only. Short Frame operation is supported for all sampling modes.

For the TDM data formats, the maximum BCK rate is 27.648MHz for either Long or Short Frame operation. The LRCK clock operates at $f_S$, the output sampling rate. The minimum clock high time for the LRCK clock is one BCK clock period. The start of frame is referenced to the rising edge of the LRCK signal.

Sub-frame selection for Long Frame TDM operation is accomplished by using the SUB input (pin 39). When SUB = 0, the PCM4204 is assigned to sub-frame 0. The SDOUT1 pin will be driven during sub-frame 0 and tri-stated during sub-frame 1. When SUB = 1, the PCM4204 is assigned to sub-frame 1. The SDOUT1 pin will be driven during sub-frame 1 and tri-stated during sub-frame 0. For Short Frame TDM operation, the SUB pin is ignored, although driving or hardwiring the SUB pin low is an acceptable practice. Figure 7 shows two PCM4204 devices and an audio DSP in a typical TDM format application.

Figure 8 and Figure 9 illustrate the PCM4204 audio serial port timing for both Master and Slave mode operation.

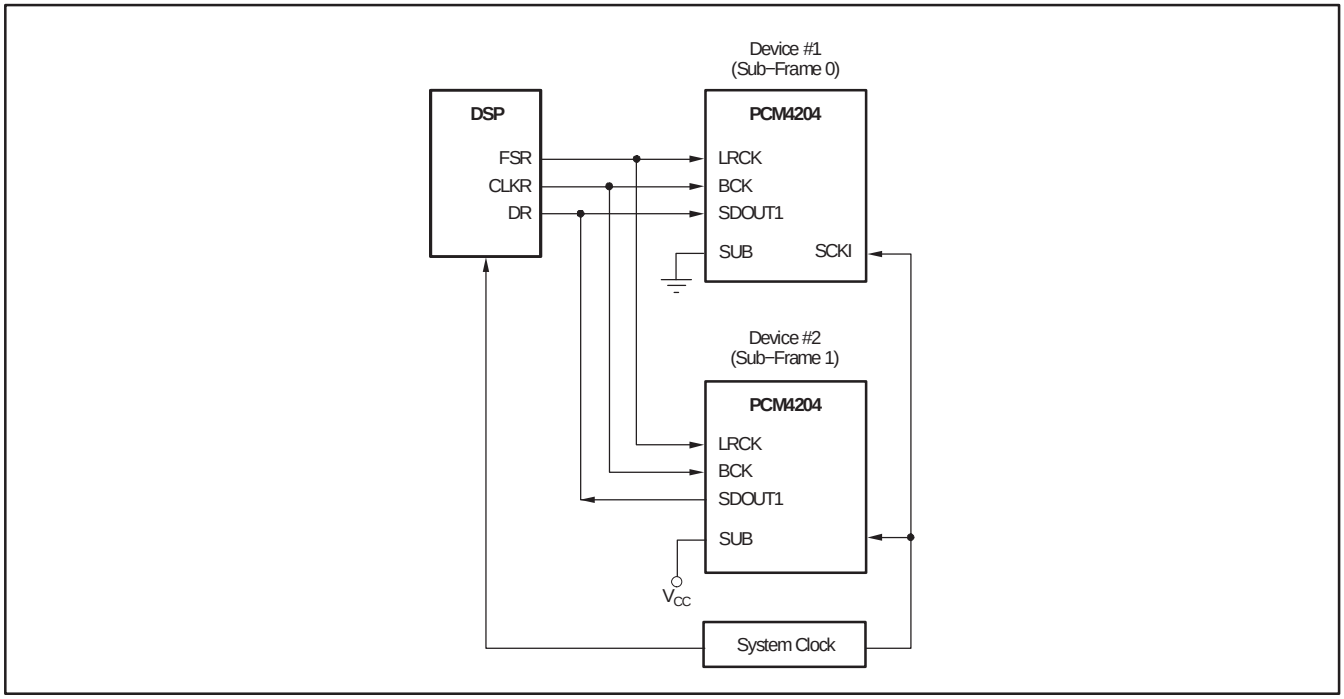
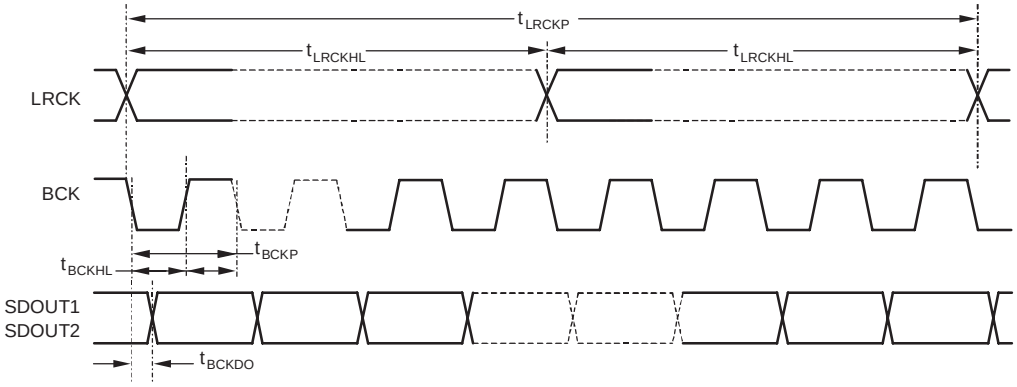
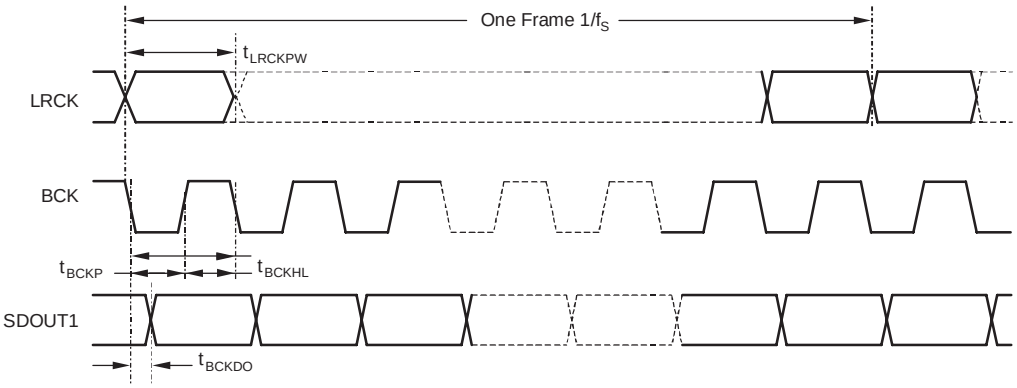



**Figure 7. TDM Connections for Two PCM4204 Devices and an Audio DSP**




| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{LRCKP}$ | LRCK Period | 5 | | µs |
| $t_{LRCKHL}$ | LRCK High/Low Time | 2.25 | | µs |
| $t_{BCKP}$ | BCK Period | 78 | | ns |
| $t_{BCKHL}$ | BCK High/Low Time | 35 | | ns |
| $t_{BCKDO}$ | SDOUT Data Output Delay from BCK Falling Edge | | 10 | ns |

**Figure 8. Master and Slave Mode Audio Serial Port Timing: Left-Justified, Right-Justified, and Philips I²S**




| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{LRCKPW}$ | LRCK Period Width | $t_{BCKP}$ | $1/f_S - t_{BCKP}$ | µs |
| $t_{BCKP}$ | BCK Period | 39 | | ns |
| $t_{BCKHL}$ | BCK High/Low Time | 17.5 | | ns |
| $t_{BCKDO}$ | SDOUT Data Output Delay from BCK Falling Edge | | 10 | ns |

**Figure 9. Slave Mode Audio Serial Port Timing: Time Division Multiplexed (TDM) Formats**

## DSD DATA PORT OPERATION

The DSD data port consists of a single DSD data clock signal, DSDCLK (pin 24), along with four synchronous DSD data lines, DSD1 (pin 25), DSD2 (pin 26), DSD3 (pin 27), and DSD4 (pin 28). The data lines correspond to Channels 1 through 4, respectively. The DSD output or input data rate is determined by the sampling mode settings for the device, discussed in the ***Sampling Modes*** section of this datasheet.

For DSD output data, the serial port is configured in Master mode, with the DSDCLK derived from the system clock input, SCKI. The DSDCLK is equivalent to the oversampling clock supplied to the delta-sigma modulators. The DSD data outputs, DSD1 through DSD4, are synchronous to the DSDCLK. The clock and data lines are then connected to a data capture device for storage and processing.

The DSD input mode, the data port is configured as an input port, with DSD clock and data lines driven from an external data source. The Audio Serial Port is configured in Master mode, with the LRCK and BCK clocks derived from the system clock input, SCKI. The PCM data format is set to 24-bit Right-Justified. The input data is processed by the digital decimation filter and output as PCM data at the audio serial port.

Figure 10 illustrates the DSD port timing for both the DSD output and input modes.

## HIGH-PASS FILTER

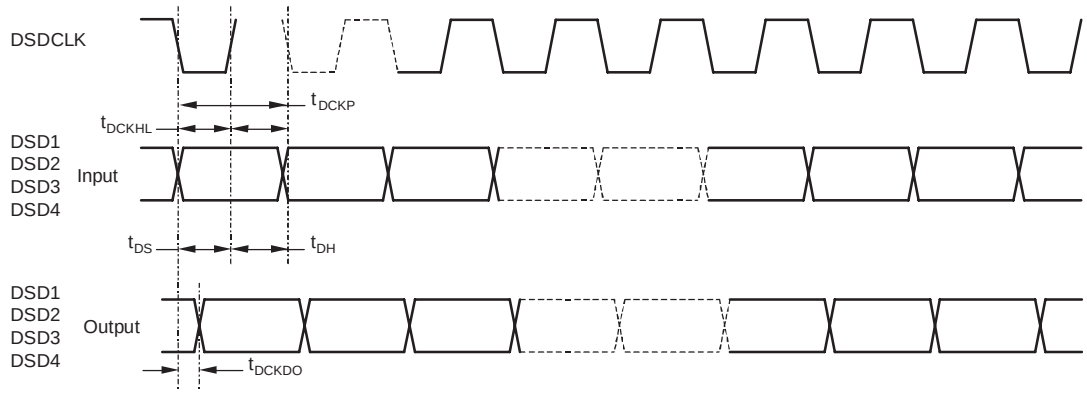
A digital high-pass filter is available for removing the DC component of the digitized input signal. The filter is located at the output of the digital decimation filter, and is available only when using PCM output data formats. The high-pass filter can be enabled or disabled for all four channels using the HPFD input (pin 38). Driving the HPFD input low enables the high-pass filter. Driving the HPFD input high disables the high-pass filter.

The −3dB corner frequency for the high-pass filter scales with the output sampling rate, where $f_{-3dB} = f_S/48000$, where $f_S$ is the output sampling rate.

## CLIPPING FLAGS

The PCM4204 includes a clipping flag output for each channel. The outputs are designated CLIP1 (pin 34), CLIP2 (pin 35), CLIP3 (pin 36), and CLIP4 (pin 37), corresponding to Channels 1 through 4, respectively.

A clipping flag is forced high as soon as the digital output of the decimation filter exceeds the full-scale range for the corresponding channel. The clipping flag output is held high for a maximum of (256 x N) / $f_S$ seconds, where N = 128 for Single Rate sampling mode, 256 for Dual Rate sampling mode, and 512 for Quad Rate sampling mode. If the decimation filter output does not exceed the full-scale range during the initial hold period, the output returns to a low state upon termination of the hold period.




| PARAMETER | DESCRIPTION | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{DCKP}$ | DSDCLK Cycle Time | 156 | | ns |
| $t_{DCKHL}$ | DSDCLK High/Low Time | 70 | | ns |
| $t_{DS}$ | Data Setup Time | 10 | 10 | ns |
| $t_{DH}$ | Data Hold Time | 10 | 10 | ns |
| $t_{DCKDO}$ | DSD Data Output Delay from DSDCLK Falling | | 10 | ns |

**Figure 10. DSD Data Port Timing**

## RESET OPERATION

The PCM4204 includes two reset functions: power-on and externally controlled. This section describes the operation of each of these functions.

On power-up, the internal reset signal is forced low, forcing the PCM4204 into a reset state. The power-on reset circuit monitors the $V_{DD}1$, $V_{DD}2$, $V_{DD}3$, $V_{CC}1$, and $V_{CC}2$ power supply. When the $V_{DD}$ supply exceeds +2.0V (±400mV) and $V_{DD}1$ and $V_{DD}2$ supply exceeds +4.0V (±400mV), the internal reset signal is forced high. The PCM4204 then waits for the system clock input (SCKI) to become active. Once the system clock has been detected, the initialization sequence begins. The initialization sequence requires 1024 system clock periods for completion. During the initialization sequence, the ADC output data pins are forced low. Once the initialization sequence is completed, the PCM4204 output is enabled. Figure 11 shows the power-on reset sequence timing.

The user may force a reset initialization sequence at any time while the system clock input is active by utilizing the $\overline{RST}$ input (pin 10). The $\overline{RST}$ input is active low, and requires a minimum low pulse width of 40ns. The low-to-high transition of the applied reset signal forces an initialization sequence to begin. As in the case of the power-on reset, the initialization sequence requires 1024 system clock periods for completion. Figure 12 illustrates the reset sequence initiated when using the $\overline{RST}$ input.

Figure 13 shows the state of the audio data outputs for the PCM4204 before, during and after the reset operations.

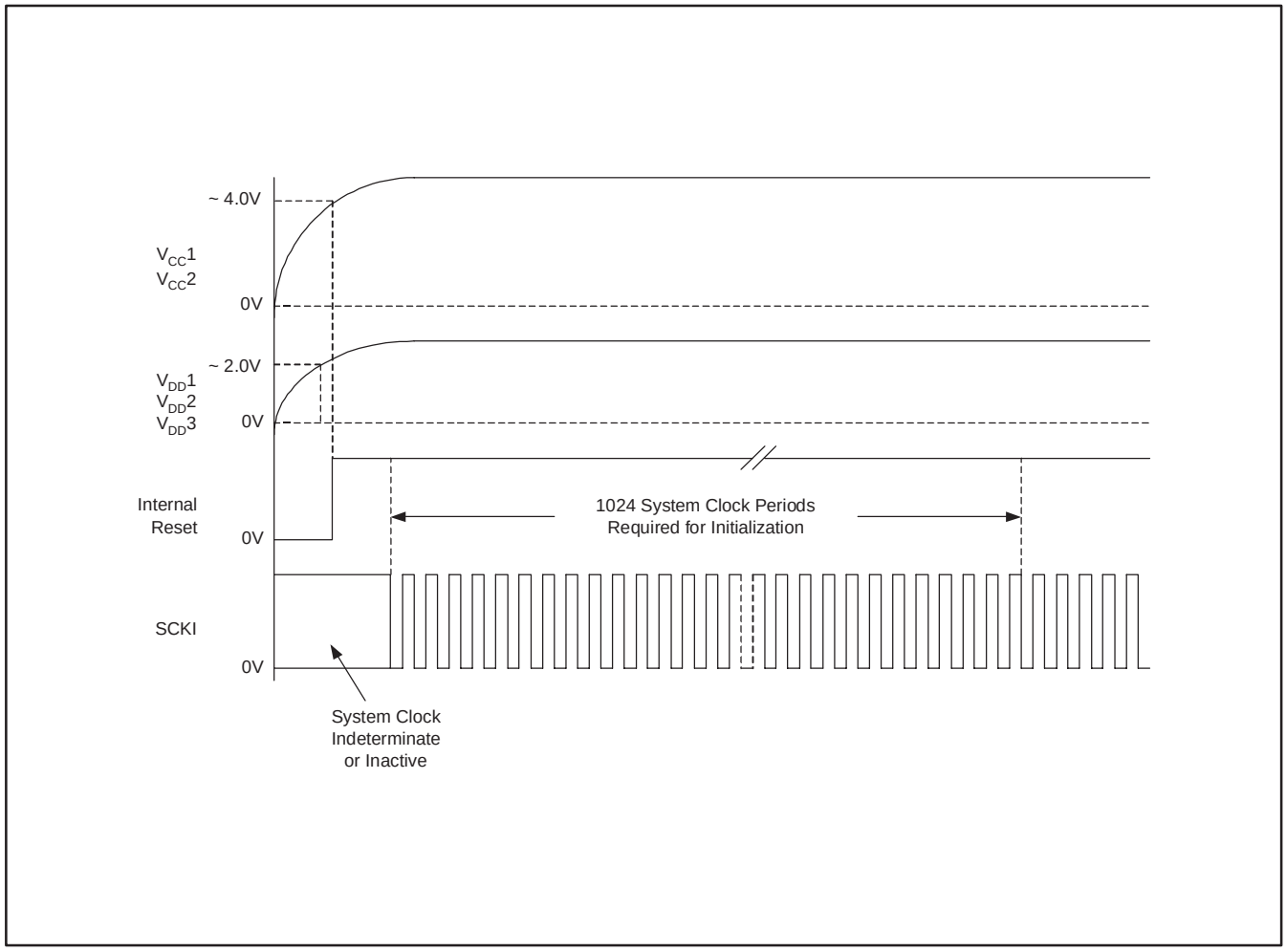



**Figure 11. Power-On Reset Sequence**

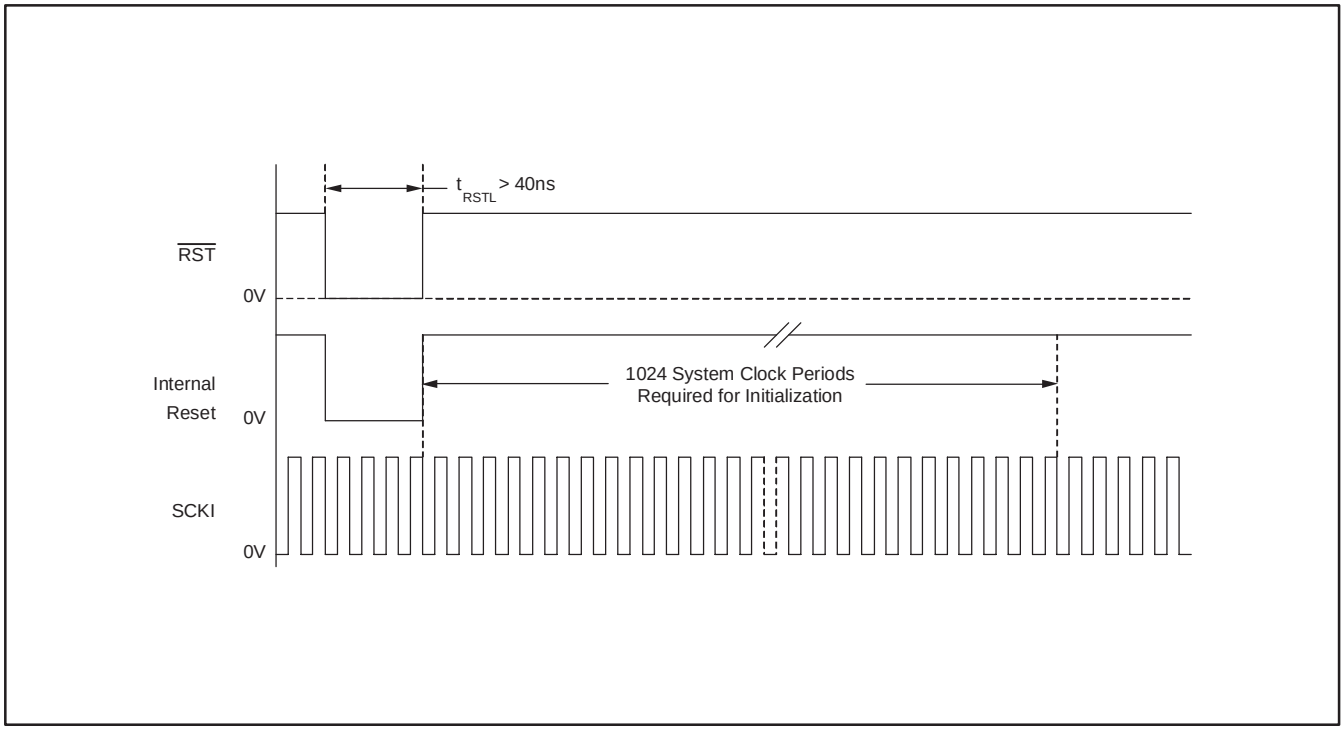



**Figure 12. External Reset Sequence**

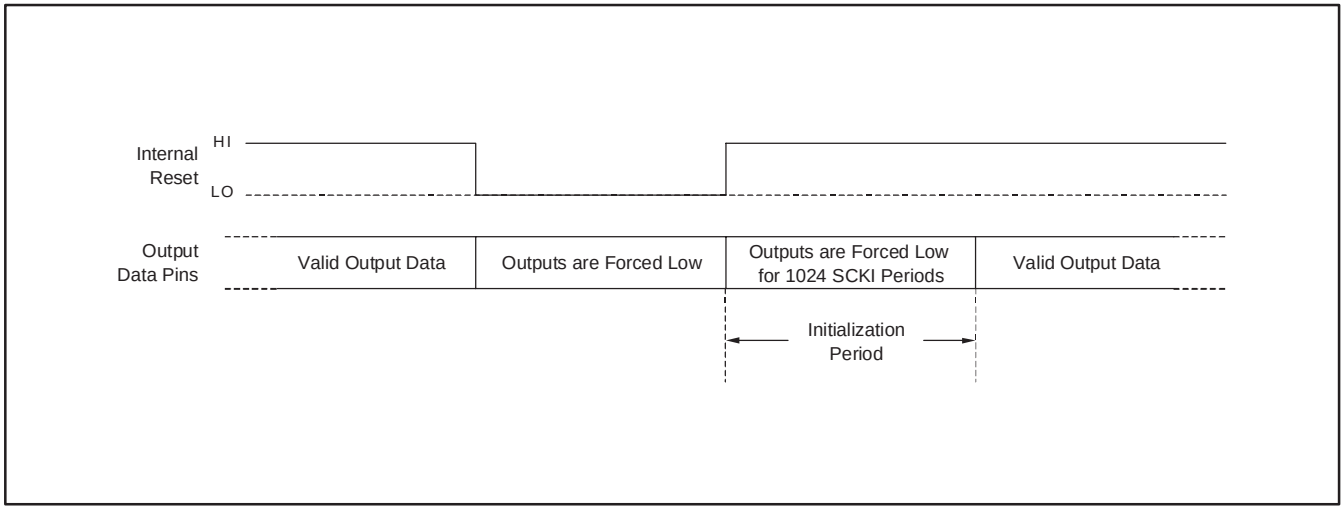



**Figure 13. ADC Digital Output State for Reset Operations**

### POWER-DOWN OPERATION

The PCM4204 can be forced to a power-down state by applying a low level to the $\overline{RST}$ input (pin 10) for a minimum of 65,536 system clock cycles. In power-down mode, all internal clocks are stopped, and output data pins are forced low. The system clock may then be removed to conserve additional power. Before exiting power-down mode, the system and audio clocks should be restarted. Once the clocks are active, the $\overline{RST}$ input may be driven high, which initiates a reset initialization sequence. Figure 14 illustrates the state of the output data pins before, during, and upon exiting the power-down state.

## APPLICATIONS INFORMATION

A typical connection diagram for the PCM4204 is shown in Figure 15. Capacitors for power supply and reference bypassing are shown with recommended values. Bypass capacitors should be located as close as possible to the power supply and reference pins of the PCM4204. Due to its small size, the 0.1µF capacitor can be located on the component (top) side of the board, while the larger 33µF capacitor can be located on the solder (bottom) side of the board.

A single ground plane is utilized for the analog and digital ground connections. This approach ensures a low impedance connection between the analog, digital, and substrate ground pins. The +5V analog and +3.3V digital power connections are provided from separate supplies.

Figure 16 illustrates an example input buffer circuit, designed for balanced differential input signals. This circuit is utilized on the PCM4204EVM evaluation board. The 2.7nF and 100pF capacitors shown at the output of the buffer should be located as close as possible to the analog input pins of the PCM4204. The buffer shown in Figure 16 can be easily made to function as a single ended to differential converter by simply grounding the (−) input terminal of the buffer circuit.

The input impedance for the $V_{COM}$IN pin of the OPA1632 is relatively low and will load down the $V_{COM}$12 or $V_{COM}$34 outputs from the PCM4204. A voltage follower circuit is required to buffer these outputs, with a typical circuit configuration shown in Figure 17. An OPA227 is utilized as the buffer for the PCM4204EVM evaluation board. However, alternative op amps with comparable performance may be substituted.

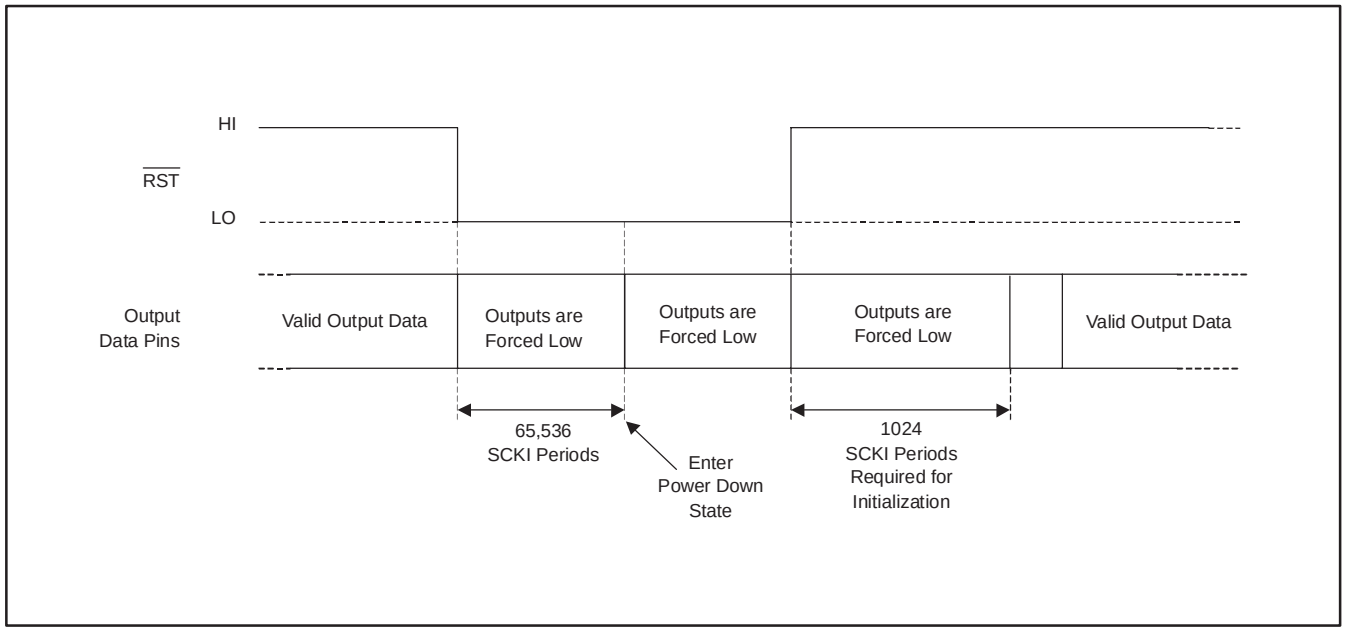



**Figure 14. ADC Digital Output State for Power-Down Operations**

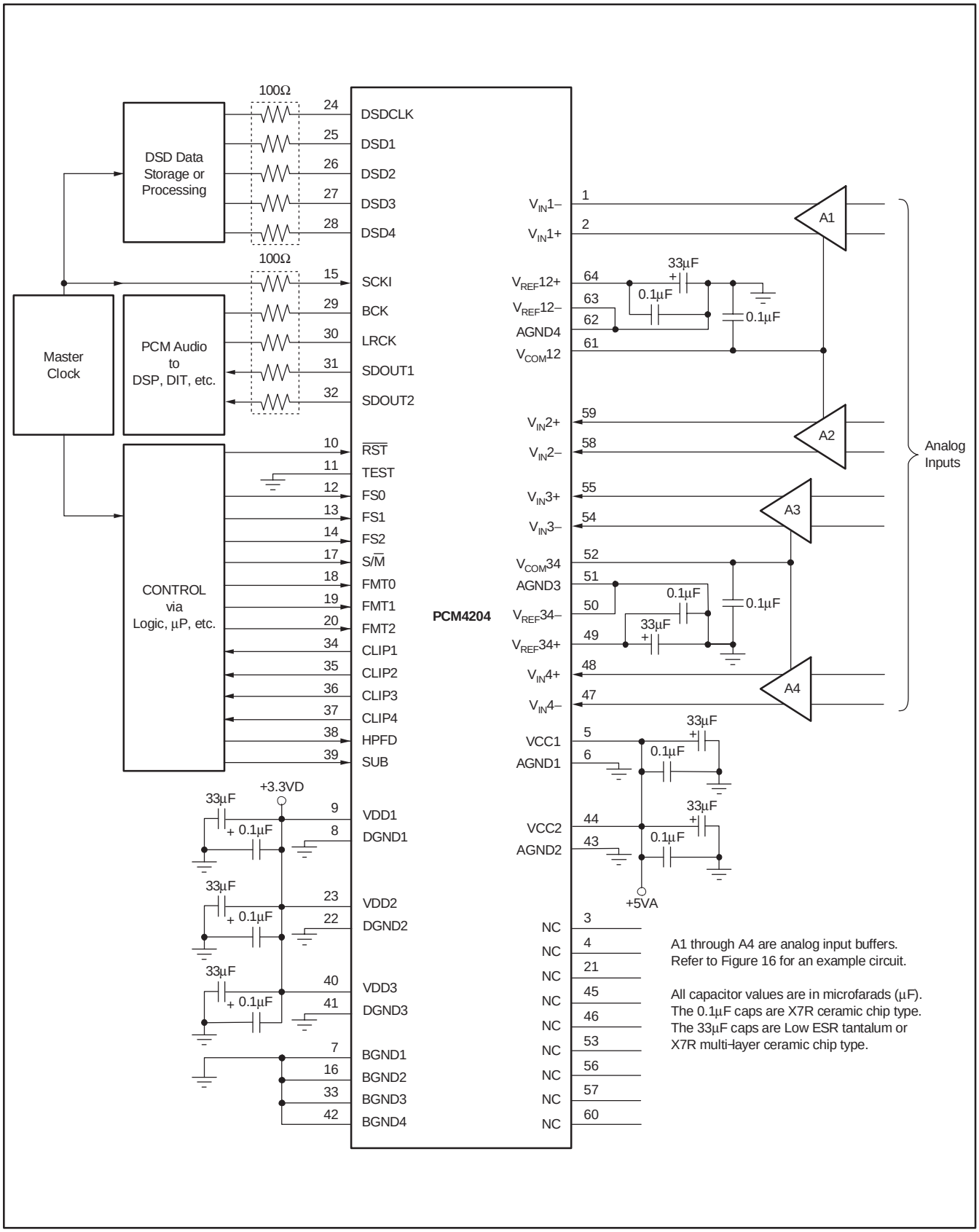



**Figure 15. Typical Connection Diagram**

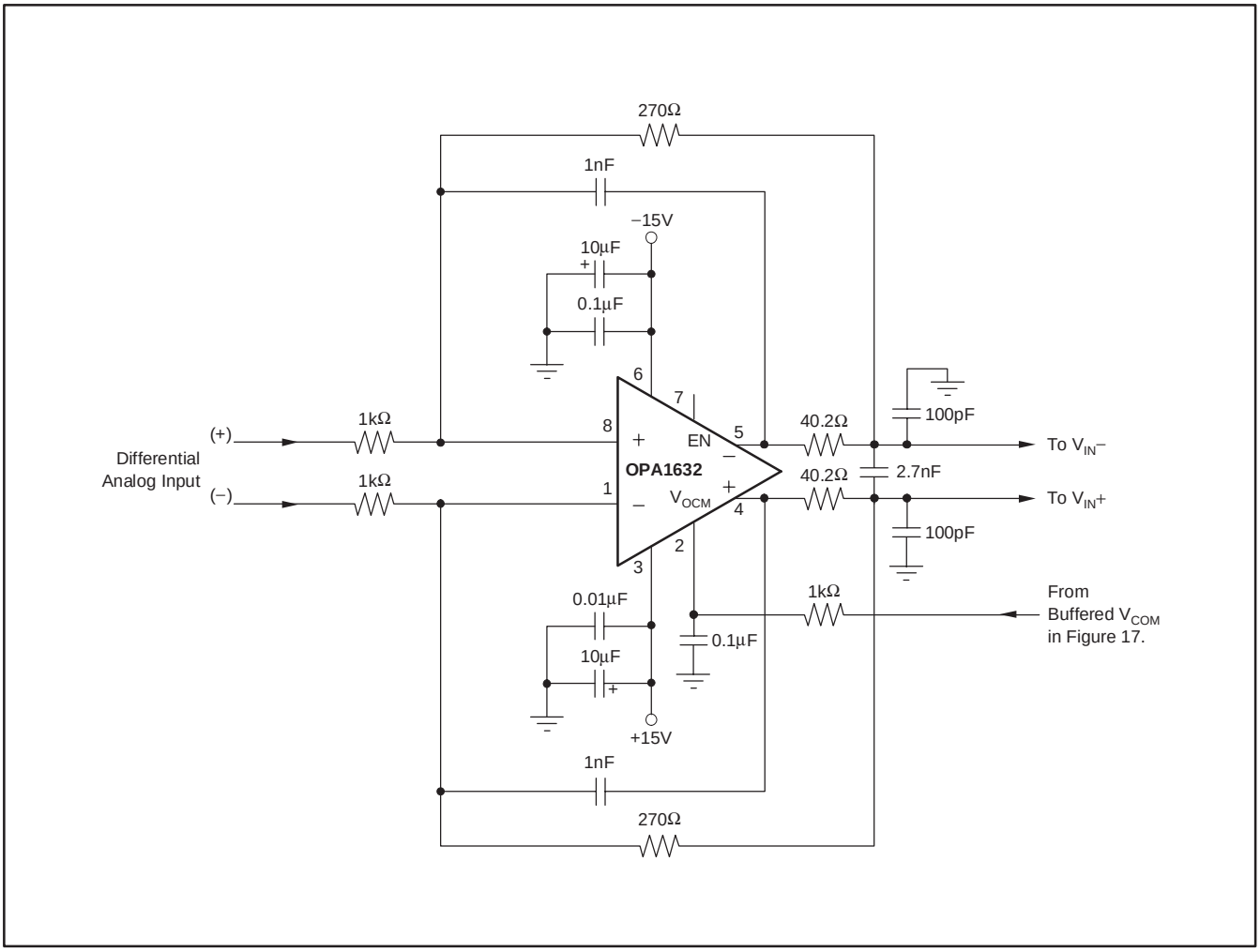



**Figure 16. Example Input Buffer Circuit**

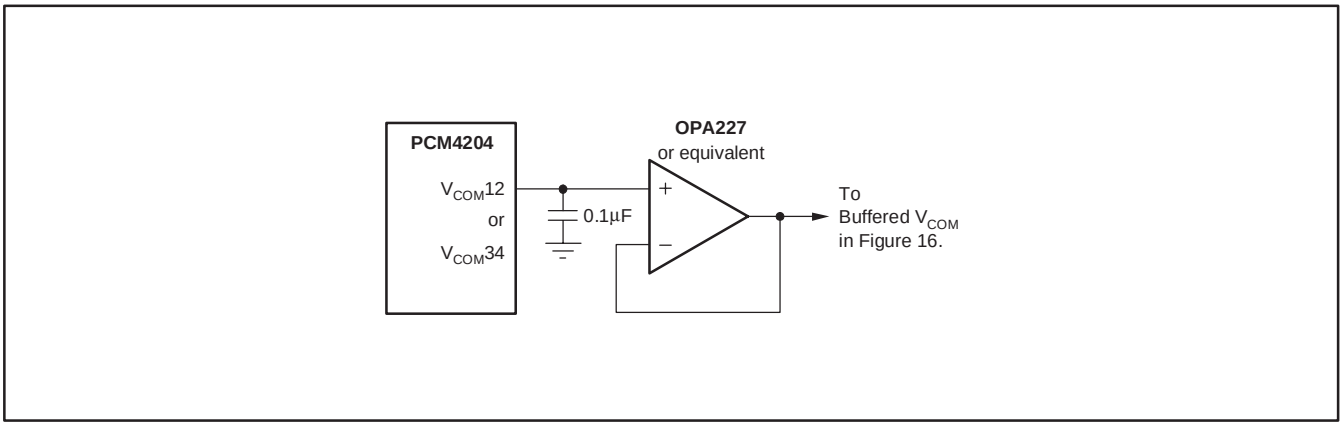



**Figure 17. Example Buffer Circuit for $V_{COM}12$ and $V_{COM}34$**

## PowerPAD THERMALLY ENHANCED PACKAGING

The PowerPAD concept is implemented in standard epoxy resin package material. The integrated circuit is attached to the leadframe die pad using thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance to the path between the IC junction and the exterior case. The external surface of the leadframe die pad is located on the PCB side of the package, allowing the die pad to be attached to the PCB using standard flow soldering techniques. This allows efficient attachment to the PCB and permits the board structure to be utilized as a heat sink for the package. Using a thermal pad identical in size to the die pad and vias connected to the PCB ground plane, the board designer can now implement power packaging without additional thermal hardware (for example, external heat sinks) or the need for specialized assembly instructions.

Figure 18 illustrates a cross-section view of a PowerPAD package.

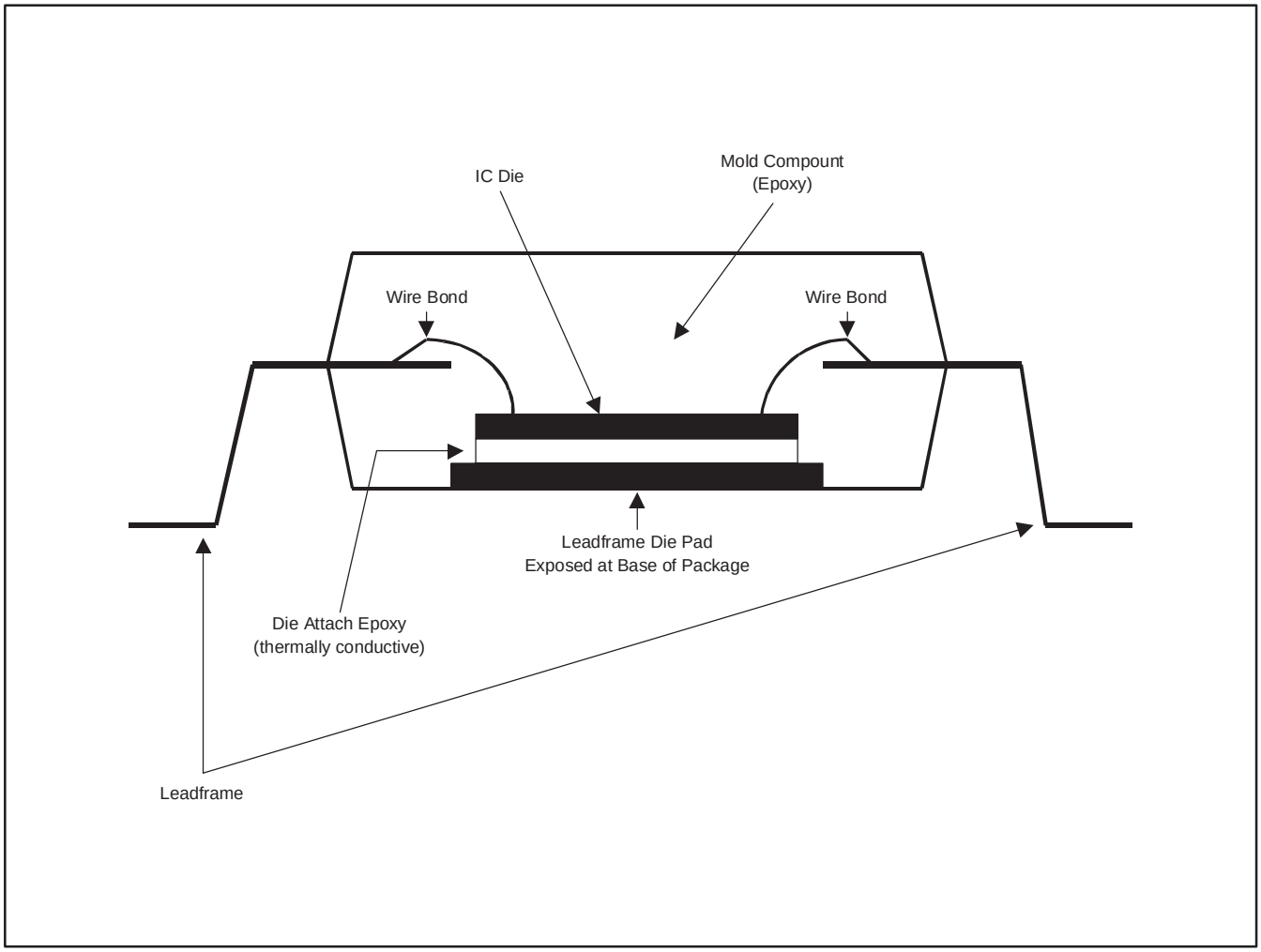



**Figure 18. Cross-Section View of a PowerPAD Thermally-Enhanced Package**

## PowerPAD PCB LAYOUT CONSIDERATIONS FOR THE PCM4204

Figure 19 shows the recommended layer structure for thermal management when using a PowerPad package on a 4-layer printed circuit board design. Note that the thermal pad is placed on both the top and bottom sides of the board. The ground plane is utilized as the heat sink, while the power plane is thermally isolated from the thermal vias.

Figure 20 shows the required thermal pad etch pattern for the 64-lead HTQFP package used for the PCM4204. Nine 13 mil (0.33 mm) thermal vias plated with 1 oz. copper are placed within the thermal pad area for the purpose of connecting the pad to the ground plane layer. The ground plane is utilized as a heatsink in this application. It is very important that the thermal via diameter be no larger than 13mils in order to avoid solder wicking during the reflow process. Solder wicking results in thermal voids that reduce heat dissipation efficiency and hampers heat flow away from the IC die.

The via connections to the thermal pad and internal ground plane should be plated completely around the hole, as opposed to the typical web or spoke thermal relief connection. Plating entirely around the thermal via provides the most efficient thermal connection to the ground plane.

## ADDITIONAL PowerPAD PACKAGE INFORMATION

Texas Instruments publishes the PowerPAD Thermally Enhanced Package Application Report (TI literature number SLMA002), available for download at www.ti.com, which provides a more detailed discussion of PowerPAD design and layout considerations. Before attempting a board layout with the PCM4204, it is recommended that the hardware engineer and/or layout designer be familiar with the information contained in this document.

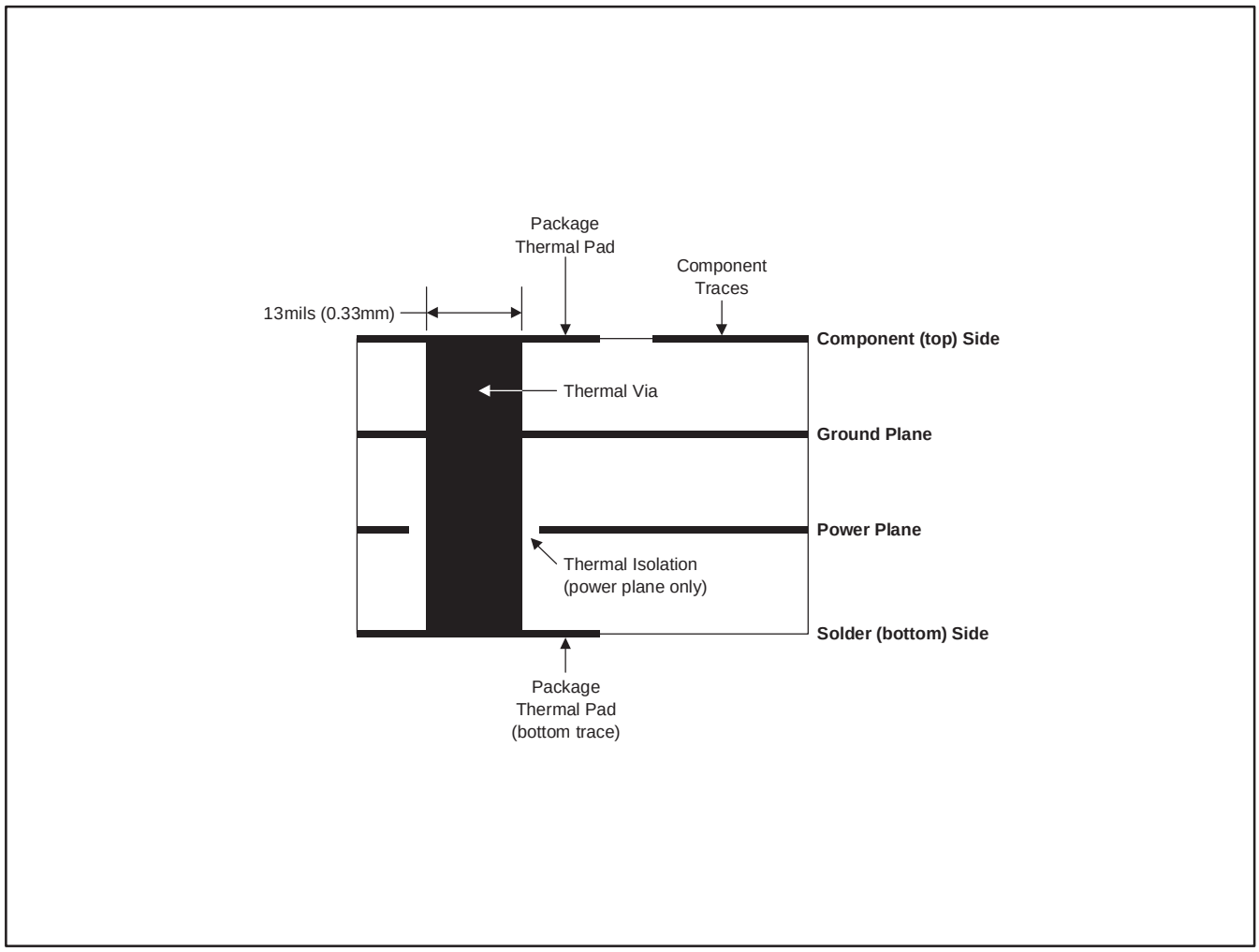



**Figure 19. Recommended PCB Structure for a 4−Layer Board**

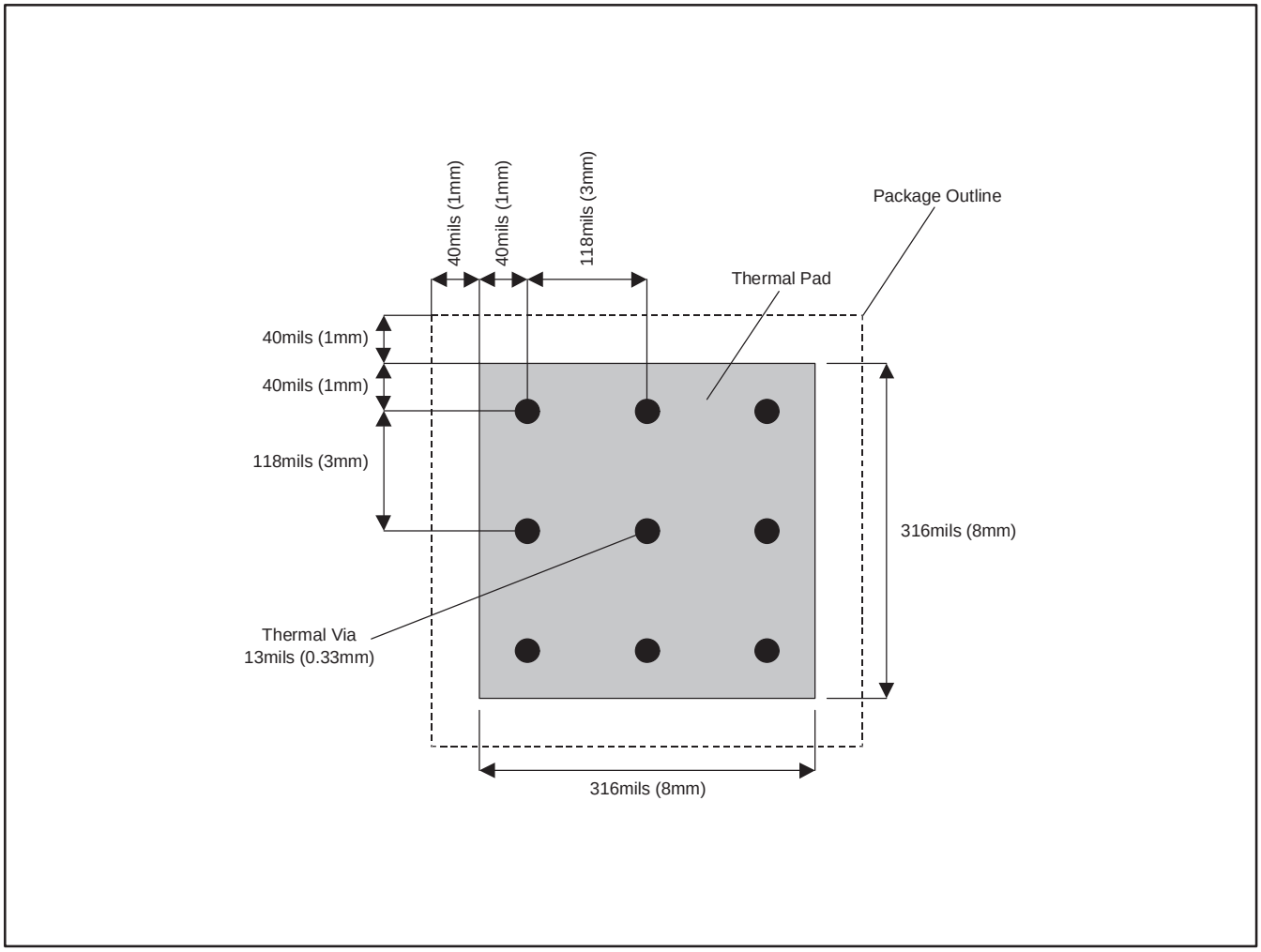



**Figure 20. Thermal Pad Etch and Via Pattern for the 64-Lead HTQFP Package**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM4204PAPR | ACTIVE | HTQFP | PAP | 64 | 1500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 70 | PCM4204 | Samples |
| PCM4204PAPRG4 | ACTIVE | HTQFP | PAP | 64 | 1500 | TBD | Call TI | Call TI | -10 to 70 | | Samples |
| PCM4204PAPT | ACTIVE | HTQFP | PAP | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -10 to 70 | PCM4204 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# GENERIC PACKAGE VIEW

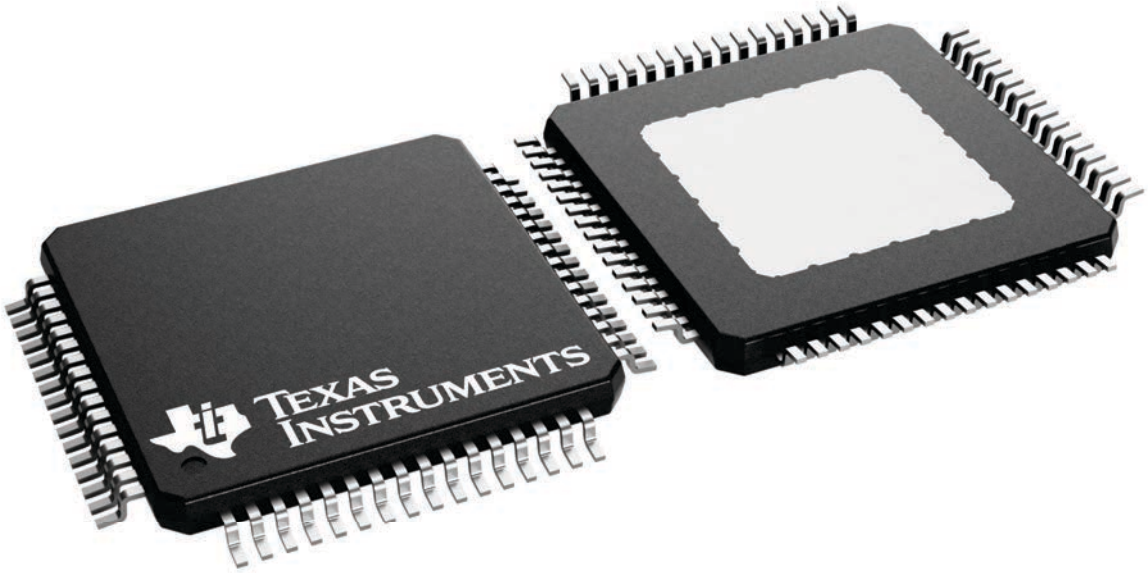
## PAP 64

## HTQFP - 1.2 mm max height

**10 x 10, 0.5 mm pitch**

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



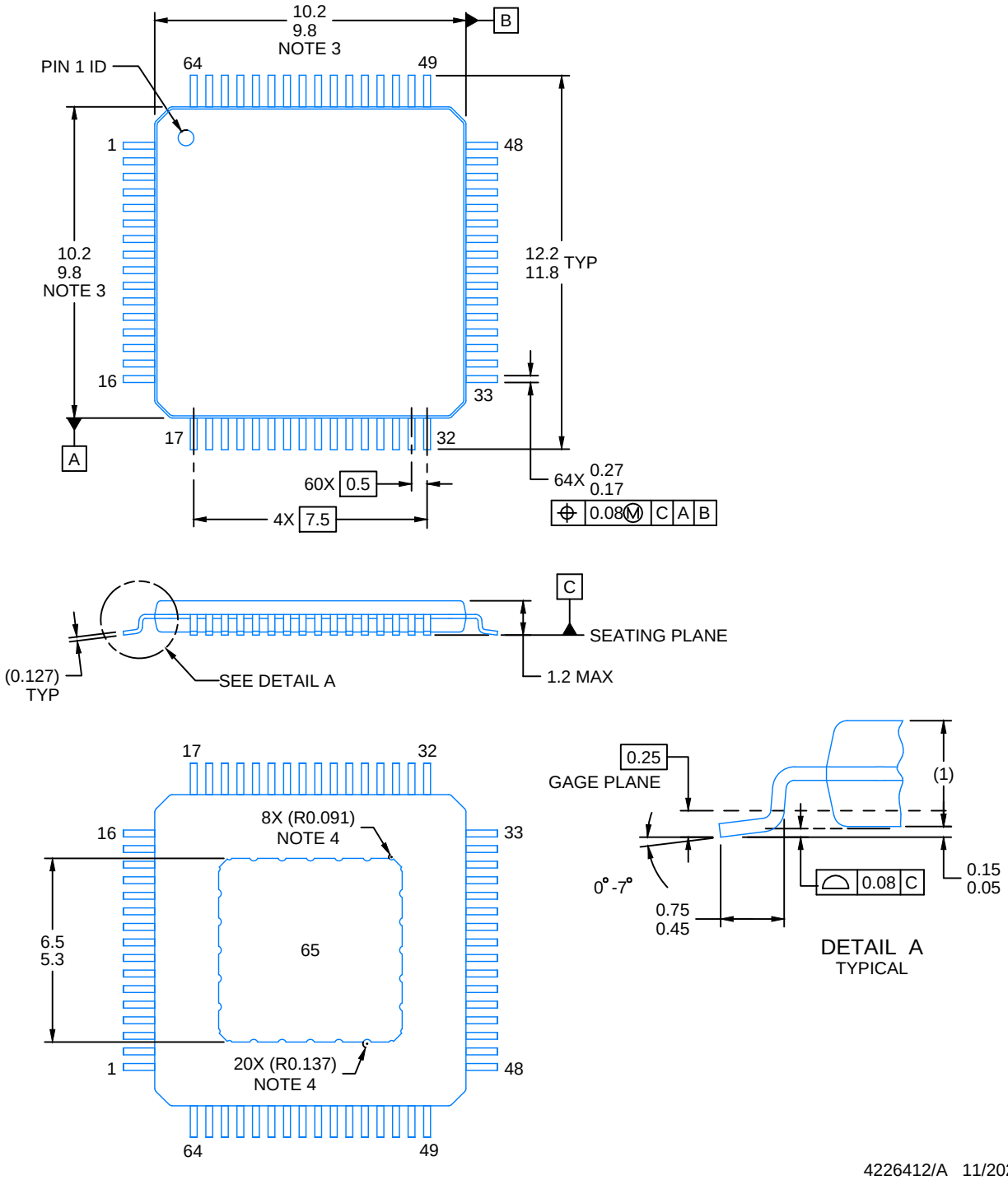

4226442/A

# PACKAGE OUTLINE

## PAP0064F

## PowerPAD™ TQFP - 1.2 mm max height

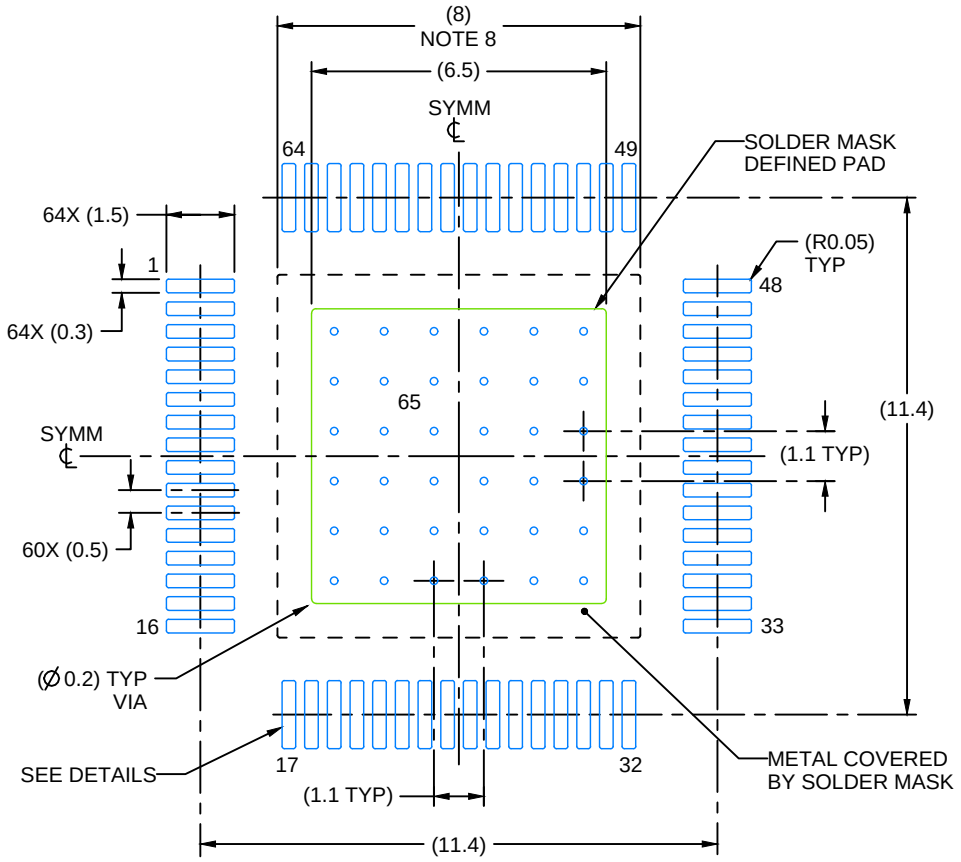
PLASTIC QUAD FLATPACK



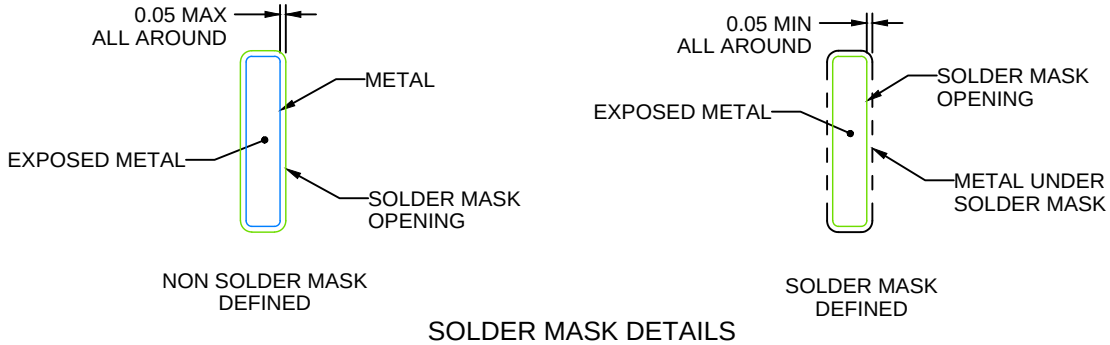

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




NON SOLDER MASK
DEFINED

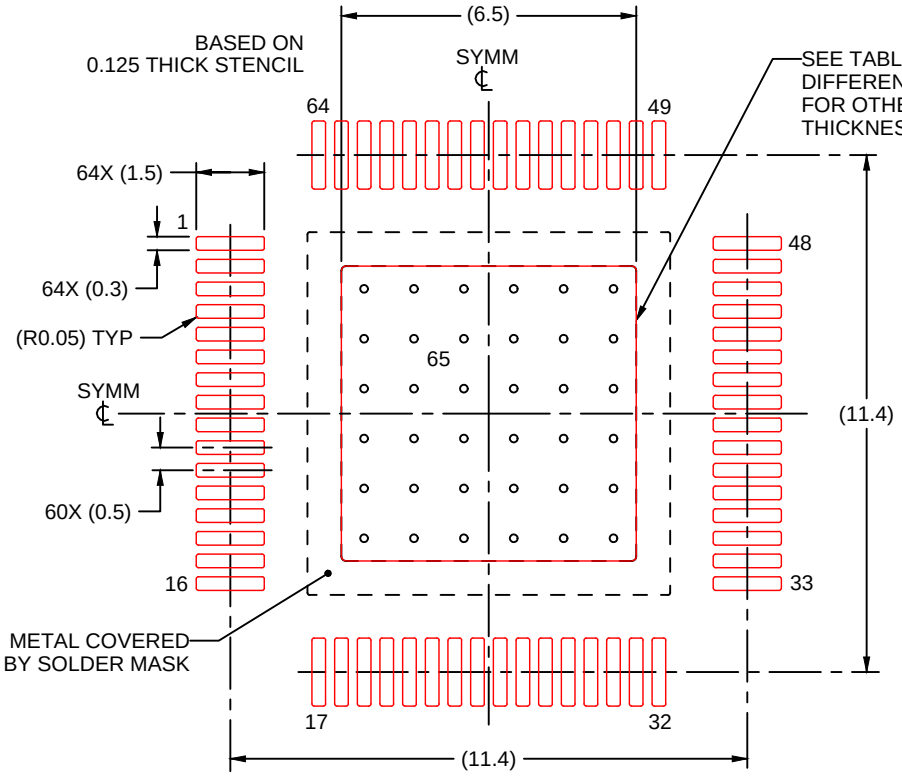
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.




SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 7.27 X 7.27 |
| 0.125 | 6.5 X 6.5 (SHOWN) |
| 0.15 | 5.93 X 5.93 |
| 0.175 | 5.49 X 5.49 |

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265