Three-Phase Power MOSFET Controller

Discontinued Product

This part is no longer in production. The part should not be purchased for new design applications. Samples are no longer available.

Date of status change: June 1, 2016

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to A3938SLDTR-T.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

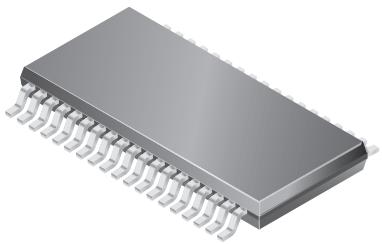
Three-Phase Power MOSFET Controller

Features and Benefits

- Drives wide range of N-channel MOSFETs
- Synchronous rectification
- Power MOSFET protection
- Adjustable dead time for cross-conduction protection
- 100% duty cycle operation
- Selectable fast or slow current-decay modes
- Internal PWM peak current control
- High-current gate drive
- Motor lead short-to-ground protection
- Internal 5 V regulator
- Brake input
- PWM torque-control input
- Fault-diagnostic output
- Tachometer output
- Thermal shutdown
- Undervoltage protection

Packages

38-pin TSSOP (suffix LD)



Not to scale

Description

The A3932 is a three-phase MOSFET controller for use with bipolar brushless DC motors. Its high gate-current drive capability allows driving a wide range of N-channel power MOSFETs and can support motor supply voltages to 50 V. Bootstrapped high-side drive blocks provide the floating positive supplies for the gate drive and minimize the component count normally required. The high-side circuitry also employs a unique FET monitoring circuit that ensures the gate voltages are at the proper levels before turn-on and during the ON cycle.

Internal fixed off-time PWM current-control circuitry can be used to regulate the maximum load current to a desired value. The peak load-current limit is set by the user's selection of an input reference voltage and external sensing resistor. The fixed off-time pulse duration is set by a user-selected external RC timing network. For added flexibility, the PWM input can be used to provide speed/torque control, allowing the internal current control circuit to set the maximum current limit.

Optional synchronous rectification is included. This feature will short out the current path through the power MOSFET reverse body diodes during the PWM off-cycle current decay. This can minimize power dissipation in the power MOSFET, eliminate the need for external power clamp diodes, and potentially allow more economical choices for the MOSFET application.

The A3932 includes the commutation logic for Hall sensors configured for 120 degree spacing. Power MOSFET protection features include bootstrap capacitor charging current monitor, undervoltage monitor, motor-lead short-to-ground, and thermal shutdown.

The '–S–' part-number suffix indicates an operating temperature range of -20°C to +85°C. The '–LD–' suffix indicates a 38-lead TSSOP package. The initial '–TR–' variant suffix indicates tape and reel packing. The '–T' final variant suffix indicates lead (Pb) free composition, with 100% matte tin leadframe plating.

Selection Guide

Part Number	Packing
A3932SLDTR-T	4000 pieces per reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{BB}		50	V
Peak Regulator Voltage	V_{REG}		15	V
Logic Input Voltage Range	V_{IN}		–0.3 to V_{LCAP} + 0.3	V
Sense Voltage Range	V_{SENSE}		–5 to 1.5	V
Output Voltage Range				V
SA, SB, SC Pins			–5 to 50	V
GHA, GHB, GHC Pins			–5 to V_{BB} + 17	V
CA, CB, CC Pins			V_{Sx} + 17	V
Operating Ambient Temperature	T_A	Range S	–20 to 85	ºC
Junction Temperature	T_J		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

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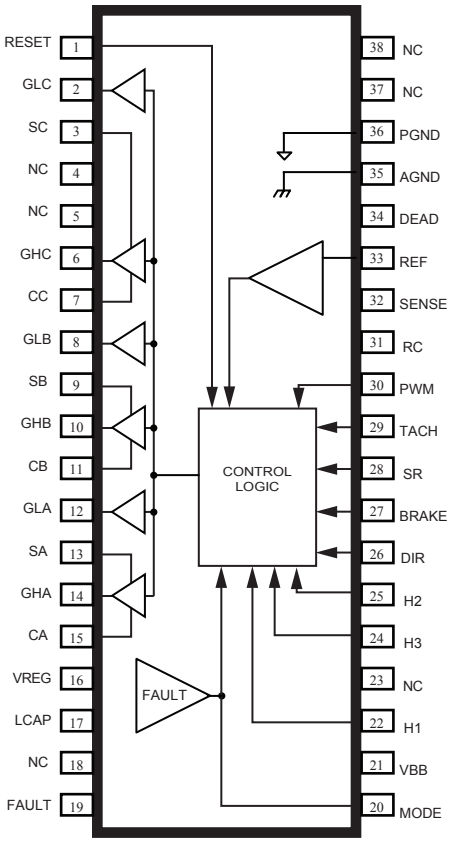
Pin-Out Diagram

38-pin TSSOP (suffix LD)



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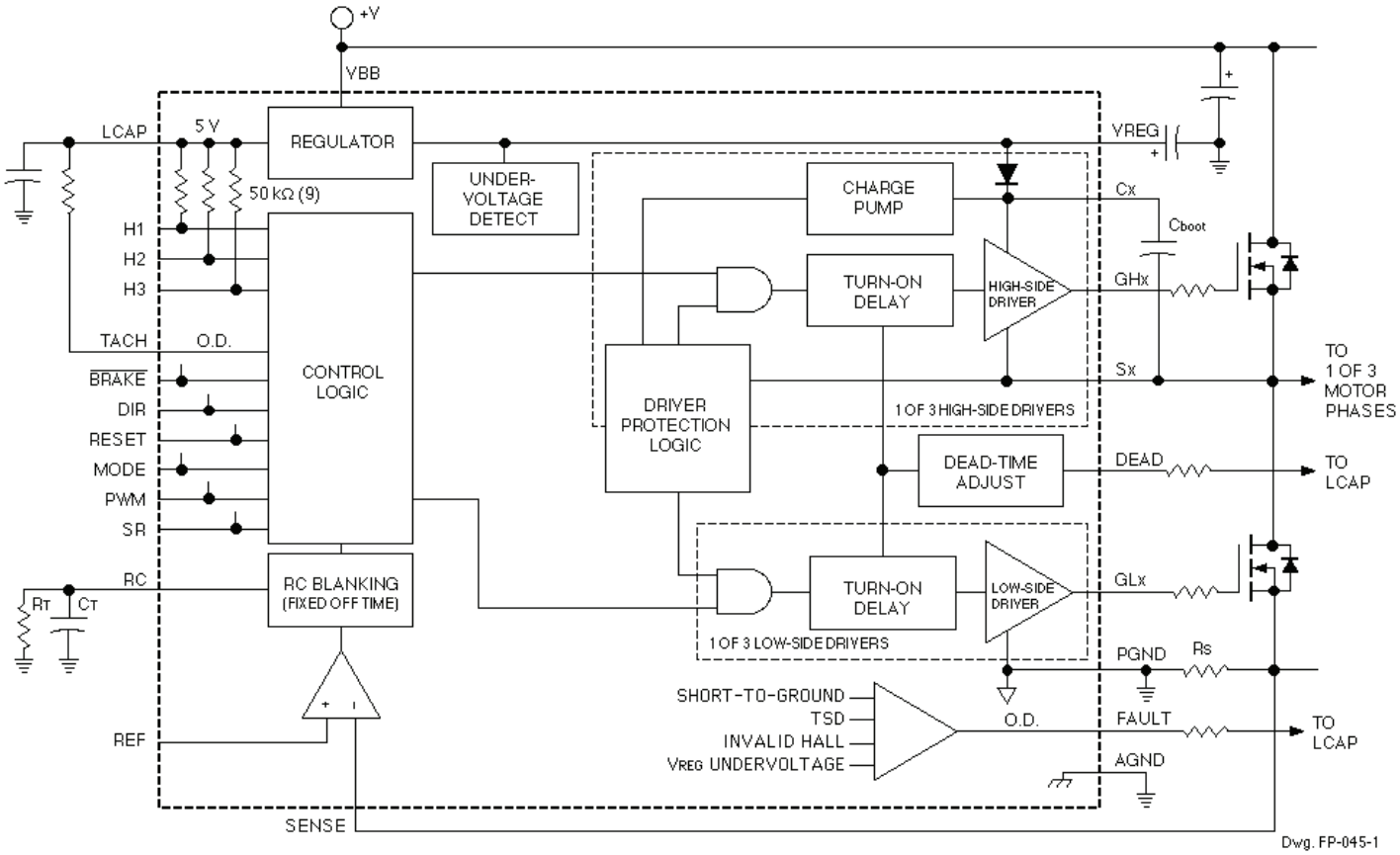
Functional Block Diagram



NOTE — For 12 V applications, VBB is shorted to VREG. The V_{REG} absolute maximum rating (15 V) must not be exceeded.

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ELECTRICAL CHARACTERISTICS: unless otherwise noted at T_A = 25°C; V_{BB} = 18 V to 50 V; C_{LCAP}, C_{boot} = 0.1 µF; C_{REG} = 10 µF; C_{load} = 3300 pF; f_{PWM} = 22.5 kHz Square Wave; Two Phases Active.

Parameter	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Supply Current						
Quiescent Current	I_{BB}	RESET high, coast mode, stopped	–	–	8.0	mA
Reference Voltage	V_{LCAP}	I_{LCAP} = -3 mA	4.75	5.0	5.25	V
Output Voltage	V_{REG}	V_{BB} = V_{REG} ≤15 V, I_{REG} = -10 mA	10.8	–	13.2	V
		18 V ≤ V_{BB} ≤ 50 V, I_{REG} = -10 mA	12.4	13	13.6	V
		V_{BB} = 13.2 V to 18 V, I_{REG} = -10 mA	–	V_{BB} - 2.5	–	V
Output Voltage Regulation	$\Delta V_{REG(\Delta IREG)}$	I_{REG} = -1 to -30 mA, coast	–	25	–	mV
	$\Delta_{VREG(\Delta VBB)}$	I_{REG} = -10 mA, coast	–	40	–	mV
Digital Logic Levels						
Logic Input Voltage	V_{IH}	All inputs except SR	2.0	–	–	V
		SR input only	3.0	–	–	V
	V_{IL}	All inputs except SR	–	–	0.8	V
		SR input only	–	–	1.8	V
Logic Input Current	I_{IH}	V_{IH} = 2 V	-30	–	-90	µA
	I_{IL}	V_{IL} = 0.8 V	-50	–	-130	µA
Gate Drive						
Low-Side Output Voltage	V_{GLxH}	I_{GLx} = 0	V_{REG} - 0.8	V_{REG} - 0.5	–	V
High-Side Output Voltage	V_{GHxH}	I_{GHx} = 0	10.4	11.6	12.8	V
Pulldown Switch Resistance	$r_{DS(on)}$	I_{GLx} = 50 mA	–	4.0	–	Ω
Pullup Switch Resistance	$r_{DS(on)}$	I_{GHx} = -50 mA	–	14	–	Ω
Low-Side Output Switching Time	t_{rGLx}	10% to 90%, with C_{load}	–	120	–	ns
	t_{fGLx}	90% to 10%, with C_{load}	–	60	–	ns
High-Side Output Switching Time	t_{rGHx}	10% to 90%, with C_{load}	–	120	–	ns
	t_{fGHx}	90% to 10%, with C_{load}	–	60	–	ns
Propagation Delay Time (PWM to gate output)	t_{pr}	GHx, GLx rising, C_{load} = 0	–	220	–	ns
	t_{pf}	GHx, GLx falling, C_{load} = 0	–	110	–	ns
Maximum Dead Time	t_{dead}	GHx to GLx, V_{DEAD} = 0 V, C_{load} = 0	3.5	5.6	7.6	µs
Minimum Dead Time	t_{dead}	GLx to GHx, I_{DEAD} = 780 µA, C_{load} = 0	50	100	150	ns

Continued —

NOTES: 1. Typical Data is for design information only.
2. Negative current is defined as coming out of (sourcing) the specified device terminal.

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Parameter	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Bootstrap Capacitor						
Bootstrap Charge Current	I_{Cx}		100	–	–	mA
Bootstrap Output Voltage	V_{Cx}	V_{Sx} = 0, I_{Cx} = 0, V_{REG} = 13 V	10.4	11.6	12.8	V
Bootstrap Resistance	r_{Cx}	I_{Cx} = -50 mA	–	9.0	12	Ω
Current Limit Circuitry						
Input Offset Voltage	V_{io}	0 V ≤ V_{IC} ≤ 1.5 V	–	–	±5.0	mV
SENSE Input Current	I_{SENSE}	V_{IC} ≥ 0 V, V_{ID} ≤ 1.5 V	–	-25	–	µA
REFERENCE Input Current	I_{REF}	V_{IC} ≥ 0 V, V_{ID} ≤ 1.5 V	–	0	–	µA
Blank Time	t_{blank}	R_T = 56 kΩ, C_T = 470 pF	–	0.91	–	µs
RC Charge Current	I_{RC}		-0.9	-1.0	-1.1	mA
RC Voltage Threshold	V_{RCL}		1.0	1.1	1.2	V
	V_{RCH}		2.7	3.0	3.3	V
Protection Circuitry						
Bootstrap Charge Threshold	I_{Cx}		–	-9.0	–	mA
Motor Short-to-Ground Monitor	V_{DSH}	V_{BB} - V_{SX}, high side on	1.3	2.0	2.7	V
Undervoltage Threshold	UVLO	Increasing V_{REG}	9.2	9.7	10.2	V
		Decreasing V_{REG}	8.6	9.1	9.6	V
FAULT Output Voltage	V_{FAULT}	I_O = 1 mA	–	–	0.5	V
TACH Output Voltage	V_{TACH}	I_O = 1 mA	–	–	0.5	V
TACH Output Pulse Width	t_{TACH}	I_O = 1 mA, C_{TACH} = 50 pF	–	0.75	–	µs
Thermal Shutdown Temp.	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J		–	10	–	°C
Thermal Resistance	$R_{\theta JA}$	Package EQ Four-layer PCB	–	37	–	°C/W
		Package LD Four-layer PCB	–	51	–	°C/W

NOTES:

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Terminal Descriptions

LD	Name
1	RESET
2	GLC
3	SC
4,5,18, 23,37,38	NC
6	GHC
7	CC
8	GLB
9	SB
10	GHB
11	CB
12	GLA
13	SA
14	GHA
15	CA
16	VREG
17	LCAP
19	FAULT
20	MODE
21	VBB
22	H1
24	H3
25	H2
26	DIR
27	$\overline{\text{BRAKE}}$
28	SR
29	TACH
30	PWM
31	RC
32	SENSE
33	REF
34	DEAD
35	AGND
36	PGND

RESET — A logic input used to enable the device, internally pulled up to V_{LCAP} (+5 V). A RESET = 1 will disable the device and force all gate drivers to 0 V, coasting the motor. A RESET = 0 allows the gate drive to follow the commutation logic. The RESET = 1 overrides $\overline{\text{BRAKE}}$.

GLA/GLB/GLC — Low-side, gate-drive outputs for external NMOS drivers. External series-gate resistors (as close as possible to the NMOS gate) can be used to control the slew rate seen at the power-driver gate, thereby controlling the di/dt and dv/dt of the SA/SB/SC outputs. GLx = 1 (or "high") means that the upper half (PMOS) of the driver is turned on and its drain will source current to the gate of the low-side FET in the external motor-driving bridge. GLx = 0 (or "low") means that the lower half (NMOS) of the driver is turned on and its drain will sink current from the external FET's gate circuit.

SA/SB/SC — Directly connected to the motor, these terminals sense the voltages switched across the load. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.

GHA/GHB/GHC — High-side, gate-drive outputs for external NMOS drivers. External series-gate resistors can be used to control the slew rate seen at the power-driver gate, thereby controlling the di/dt and dv/dt of the SA/SB/SC outputs. GHx = 1 (or "high") means that the upper half (PMOS) of the driver is turned on and its drain will source current to the gate of the high-side FET in the external motor-driving bridge. GHx = 0 (or "low") means that the lower half (NMOS) of the driver is turned on and its drain will sink current from the external FET's gate circuit.

CA/CB/CC — High-side connections for the bootstrap capacitors, positive supply for high-side gate drivers. The bootstrap capacitors are charged to approximately V_{REG} when the associated output Sx terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for N-channel power MOSFETs.

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Terminal Descriptions (cont'd)

FAULT — Open-drain output to indicate fault condition; FAULT = 1 (external pull-up) for any of the following:

1 – invalid HALL input code,

2 – undervoltage condition detected at VREG.

3 – thermal shutdown, or

4 – motor lead (SA/SB/SC) shorted to ground.

Except for a short-to-ground fault that only turns off the high-side drivers, faults will force a coast condition that turns off all power MOSFETs. Only the short-to-ground fault is latched but is cleared at each commutation. If the motor has stalled due to a short-to-ground being detected, toggling the RESET terminal or repeating a power-up sequence will clear the fault. Typically pulled up to V_{LCAP} (+5 V) with an external 5.1 kΩ resistor.

MODE — A logic input to set current-decay method, internally pulled up to V_{LCAP} (+5 V). When in slow-decay mode (MODE = 1), only the high-side MOSFET is switched off during a PWM-off cycle. The fast-decay mode (MODE = 0) switches both the high-side and low-side MOSFETs.

H1/H2/H3 — Hall-sensor inputs; internally pulled up to V_{LCAP} (+5 V). Configured for 120° electrical spacing.

DIR — A logic input to reverse rotation, see Commutation Truth Table. Internally pulled up to V_{LCAP} (+5 V).

$\overline{\text{BRAKE}}$ — An active-low logic input for a braking function. $\overline{\text{A BRAKE}}$ = 0 will turn on the low-side FETs and turn off the high-side FETs. This will effectively short-circuit the BEMF in the windings and brake the motor. The braking torque applied will depend on the speed. Internally pulled up to V_{LCAP} (+5 V). RESET = 1 overrides $\overline{\text{BRAKE}}$ and will coast the motor.

SR — Synchronous rectification input. An SR = 0 disables this feature, forcing current decay through the body diodes of the power MOSFETs. An SR = 1 will result in appropriate high- and low-side gate outputs to switch in response to a PWM-off command. Internally pulled up to V_{LCAP} (+5 V). See also the Input Logic table.

TACH — An open-drain digital output whose frequency is proportional to speed of rotation. A pulse appears at every HALL transition. Typically pulled up to V_{LCAP} (+5 V) with an external 5.1 kΩ resistor.

PWM — Speed control input, internally pulled up to V_{LCAP} (+5 V). A PWM = 0 turns off selected drivers. A PWM = 1 will turn on selected drivers as determined by H1/H2/H3 input logic. Holding PWM = 1 allows speed/torque control solely by the internal current-limit circuit with the REF analog voltage. See also the Input Logic table .

RC — An analog input used to set the fixed off time with an external resistor (R_T) and capacitor (C_T). The t_{blank} time is controlled by the value of the external capacitor (see Applications Information). See Application Information.

SENSE — An analog input to the current-limit comparator. A voltage representing load current appears on this terminal during on time, when it reaches REF voltage, the comparator trips and load current decays for the fixed off-time interval. Voltage transients seen at this terminal when the drivers turn on are ignored for time t_{blank}.

REF — An analog input to the current-limit comparator. Voltage applied here with respect to AGND sets the peak load current.

$$I_{peak} = V_{REF}/R_S.$$

VREG — A regulated 13 V output; supply for low-side gate drive and bootstrap capacitor charge circuits. It is good practice to connect a decoupling capacitor from this terminal to AGND, as close to the device terminals as possible. This terminal should be shorted to V_{BB} for 12 V applications.

VBB — The A3932 supply voltage. It is good practice to connect a decoupling capacitor from this terminal to AGND, as close to the device terminals as possible.

LCAP — Connection for 0.1 µF decoupling capacitor for the internal 5 V reference. This terminal can source no more than 3 mA for the DEAD input, TACH and FAULT outputs.

DEAD — An analog input. A resistor between DEAD and LCAP is selected to adjust the turn-off to turn-on time. This delay is needed to prevent shoot-through in the external power MOSFETs. See Applications Information for details on setting dead time.

AGND — The low-level (analog) reference point.

PGND — The return for all low-side gate drivers. This should be connected to the system power ground.

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Commutation Truth Table

Logic Inputs				Driver Outputs						Motor Terminals		
H1	H2	H3	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SA	SB	SC
1	0	1	1	0	0	1	1	0	0	H	Z	L
1	0	0	1	0	0	1	0	1	0	Z	H	L
1	1	0	1	1	0	0	0	1	0	L	H	Z
0	1	0	1	1	0	0	0	0	1	L	Z	H
0	1	1	1	0	1	0	0	0	1	Z	L	H
0	0	1	1	0	1	0	1	0	0	H	L	Z
1	0	1	0	1	0	0	0	0	1	L	Z	H
1	0	0	0	0	1	0	0	0	1	Z	L	H
1	1	0	0	0	1	0	1	0	0	H	L	Z
0	1	0	0	0	0	1	1	0	0	H	Z	L
0	1	1	0	0	0	1	0	1	0	Z	H	L
0	0	1	0	1	0	0	0	1	0	L	H	Z

Input Logic

MODE	PWM	SR	RESET	Operation
0	0	0	0	PWM chop mode, fast decay, all drivers off
0	1	0	0	Peak current limit, selected drivers on
1	0	0	0	PWM chop mode. slow decay, selected low side drivers on
1	1	0	0	Peak current limit, selected drivers on
0	0	1	0	PWM chop mode, fast decay with opposite of selected drivers on
0	1	1	0	Peak current limit, selected drivers on
1	0	1	0	PWM chop, slow decay with both low-side drivers on
1	1	1	0	Peak current limit, selected drivers on
X	X	X	1	All gate drive outputs off, clear fault logic, coast

L = Low (less positive) level
H = High (more positive) level
X = Don't care
Z = High impedance
1 = Active or true logic condition
0 = Inactive or false logic condition

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Applications Information

Synchronous Rectification. To reduce power dissipation in the external MOSFETs, the A3932 control logic turns on the appropriate low-side and high-side driver during the load-current recirculation, PWM-off cycle. Synchronous rectification allows current to flow through the MODE-selected MOSFET, rather than the body diode, during the decay time. The body diodes of the SR power MOSFETs will conduct only during the dead time required at each PWM transition.

Dead Time. It is required to have a dead-time delay between a high- or low-side turn off and the next turn-on event to prevent cross conduction. The potential for cross conduction occurs with synchronous rectification, direction changes, PWM, or after a bootstrap capacitor charging cycle. The dead time is set by a resistor (R_{dead}) between the DEAD terminal and LCAP (+5 V) and can be set between 100 ns and 5.5 µs.

The following equations are valid for R_{dead} between 5.6 kΩ and 470 kΩ. At 25°C,

$$t_{dead}\ (nom, ns) = 37 + (11.9 \times 10^{-3} \times (R_{dead} + 500))$$

For predicting worst case, over voltage and temperature extremes,

$$t_{dead}\ (min, ns) = 10 + (6.55 \times 10^{-3} \times (R_{dead} + 350))$$

$$t_{dead}\ (max, ns) = 63 + (17.2 \times 10^{-3} \times (R_{dead} + 650))$$

For comparison with I_{DEAD} test currents,

$$I_{DEAD} = (V_{LCAP} - V_{be})/(R_{dead} + R_{int})$$

where (nominal values) V_{LCAP} = 5 V, V_{be} = 0.7 V at 25°C, and R_{int} = 500 Ω.

Rather than use R_{dead} values near 470 kΩ, set DEAD = ground (V_{DEAD} = 0 V), which activates an internal (I_{DEAD} = 10 µA) current source.

The choice of power MOSFET and external series gate resistance determines the selection of the dead-time resistor. The dead time should be made long enough to cover the variation of the MOSFET gate capacitance and series gate resistance (both external and internal to the A3932) tolerances.

Decoupling. The internal reference, V_{REG}, supplies current for the gate-drive circuit. As the gates are driven high they will require current from an external capacitor to support the transients. This capacitor should be placed as close as possible to the V_{REG} terminal. Its value should be at least 20 times larger than the bootstrap capacitor.

Additionally, a 0.1 µF (or larger) decoupling capacitor should be connected between LCAP and AGND as close to the device terminals as possible.

Protection Circuitry. The A3932 has several protection features:

1) **Bootstrap Circuit.** The bootstrap capacitor is charged whenever a low-side MOSFET is on, Sx output goes low, and the load current recirculates. This happens constantly during normal operation. The high-side MOSFET will not be allowed to turn on before the charging has decayed to less than approximately 9 mA. No fault will be registered.

When a phase's high-side driver is on for a long time (100% duty cycle operation) its charge pump is designed to maintain $V_{GS} > 9$ V on the bridge FET if I_{GHx} (the load on the gate driver) < 10 µA.

2) **Hall Invalid.** Illegal codes for the HALL inputs (000 or 111) will force a fault and coast the motor. Noisy Hall lines may cause double TACH pulses and, therefore, code errors that produce faults. Additional external pullup loading and filtering may be required depending on the system.

3) **VREG Undervoltage.** An internal regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that V_{REG} is at the proper level before enabling any of the outputs. The undervoltage circuit is active during power-up and will force a motor coast condition (all gate drives, GHx and GLx = 0) until V_{REG} is greater than approximately 9.7 V.

4) **Thermal Shutdown.** A junction temperature greater than 165°C will signal a fault and coast the motor (all gate drives LOW). If the junction temperature then falls to less than 155°C (hysteresis), the fault will be cleared.

5) **Motor Lead Shorted to Ground.** The A3932 will signal a fault if a motor lead is shorted to ground. A short to ground is assumed after a high side is turned on and greater than 2 V is measured between the drain (V_{BB}) and source (SA/SB/SC) of the high-side power MOSFET. This fault is cleared at the beginning of each commutation. If a stalled motor results from a fault, the fault can only be cleared by toggling the RESET terminal or by a power-up sequence.

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Applications Information (cont'd)

Current Control. Internal fixed off-time PWM circuitry is implemented to limit load current to a desired value. When a high-side and low-side MOSFET are turned on, current will increase in the motor winding until it reaches a value given by

$$I_{TRIP} \approx V_{REF}/R_S.$$

At the trip point, the sense comparator resets the source-enable latch, turning off the high-side driver. Load inductance causes the current to recirculate (decay) for the fixed off time. The current path during recirculation is determined by the configuration of the MODE and SR inputs.

An external resistor (R_T) and capacitor (C_T), connected in parallel from the RC terminal to AGND, are used to set the fixed off-time period ($t_{off} = R_T \times C_T$). R_T should be in the range of 10 kΩ to 500 kΩ. The t_{off} should be in the range of 10 µs to 50 µs. Larger values for t_{off} can result in audible noise problems.

Torque control can be implemented by varying the REF input voltage as long as the PWM input stays high. If direct control of the torque/current is desired by PWM input, a voltage can be applied to the REF input to set an absolute maximum current limit.

PWM Blank. The capacitor (C_T) also serves as the means to set the blank time duration. At the end of the PWM off cycle, a high-side gate selected by the commutation logic will turn on. At this time, large current transients can occur during the reverse recovery time (t_{rr}) of the intrinsic body diodes of the external power MOSFETs. To prevent false tripping of the current-sense comparator, the blank function disables the comparator for a time

$$t_{blank} = 1.9 \times C_T/(0.001 - [2/R_T])$$

The user must ensure that C_T is large enough to cover the current-spike duration.

Braking. The A3932 will dynamically brake by forcing all low-side MOSFETs on and all high-side MOSFETs off. This will effectively short-circuit the BEMF and brake the motor. During braking, the load current can be approximated by:

$$I_{BRAKE} = V_{BEMF}/R_L$$

Because the load current does not flow through the sense resistor during a dynamic brake, care must be taken to ensure that the power MOSFET's maximum ratings are not exceeded.

RESET = 1 overrides $\overline{\text{BRAKE}}$ and turns all motor bridge FETs off, coasting the motor.

Low-Voltage Operation. Although VREG can be connected to VBB for 12 V systems, the V_{REG} maximum rating of 15 V must be observed *including* transients. If transients cannot be adequately controlled, use VREG in the regulator mode (not connected to VBB). With V_{BB} less than 18 V, the V_{REG} output voltage level specification may not be met. Note that in this mode the VREG undervoltage threshold may leave the system with little headroom if V_{BB} is less than 12 V.

Driving an H Bridge. The A3932 may be used to drive an H bridge (e.g., a brush dc motor load) by hard wiring one state for the Hall inputs (e.g., H1 = H2 = 1 (HIGH), H3 = 0 (LOW)). Leave the appropriate phase driver outputs floating (in this case CC, GHC, SC, and GLC because, from the Commutation Truth Table, SC = Z). The DIR input controls the motor rotation while the PWM, MODE, and SR inputs control the motor current behavior as described in the Input Logic table.

Layout. Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits.

1) The analog ground (AGND), the power ground (PGND), and the high-current return of the external MOSFETs (the negative side of the sense resistor) should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.

2) Minimize stray inductances by using short, wide copper runs at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power buss, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

3) Kelvin connect the SENSE terminal PC trace to the positive side of the sense resistor.

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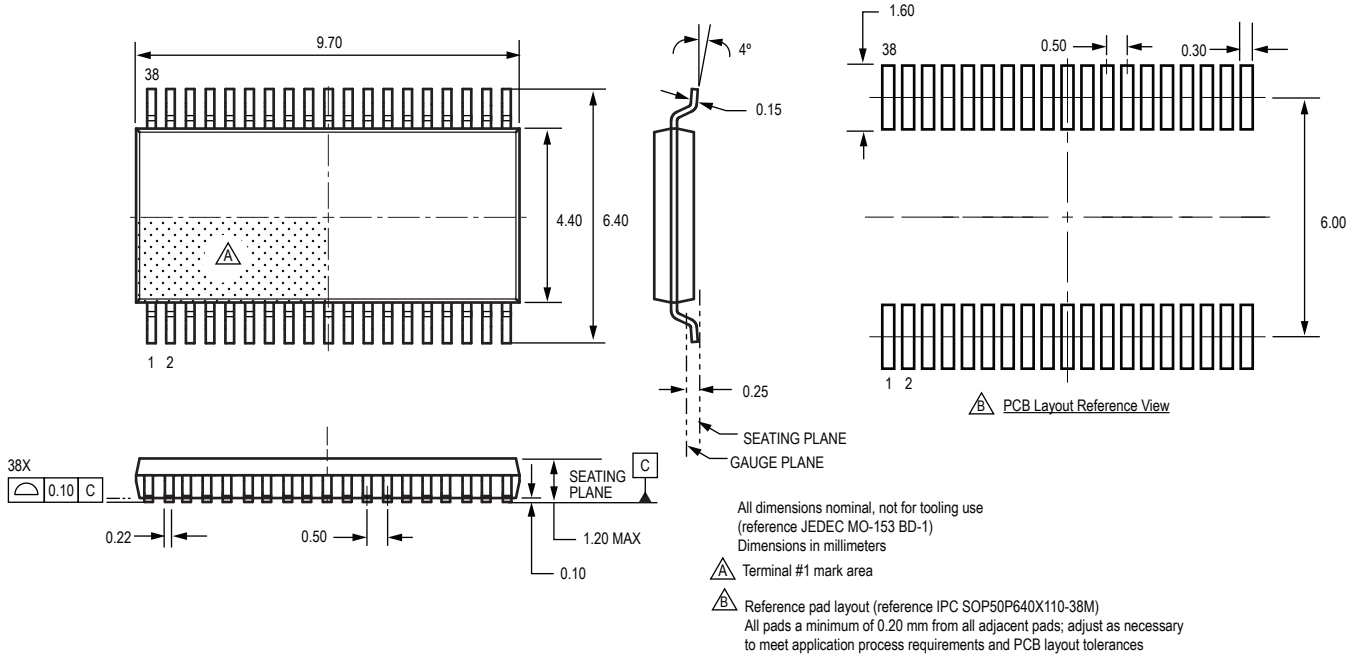
Package LD, 38-Pin TSSOP



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