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FAIRCHILD SEMICONDUCTOR®

April 2011

# FDMS3600AS

## PowerTrench® Power Stage

## Asymmetric Dual N-Channel MOSFET

### Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 5.6 mΩ at $V_{GS}$ = 10 V, $I_D$ = 15 A
- Max $r_{DS(on)}$ = 8.5 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 14 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 1.6 mΩ at $V_{GS}$ = 10 V, $I_D$ = 30 A
- Max $r_{DS(on)}$ = 2.4 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 25 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

### General Description

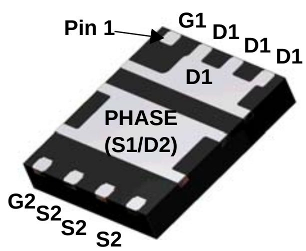
This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

### Applications

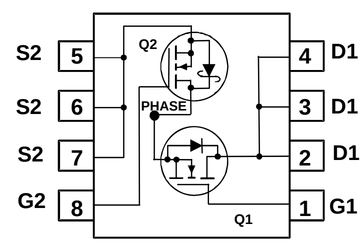
- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE

Top

Power 56




Bottom




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 25 | 25 | V |
| $V_{GS}$ | Gate to Source Voltage | (Note 3) | ±20 | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package limited) | $T_C$ = 25 °C | 30 | 40 | A |
| | -Continuous (Silicon limited) | $T_C$ = 25 °C | 65 | 155 | |
| | -Continuous | $T_A$ = 25 °C | 15[1a] | 30[1b] | |
| | -Pulsed | | 40 | 100 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | 50[4] | 200[5] | mJ |
| $P_D$ | Power Dissipation for Single Operation | $T_A$ = 25 °C | 2.2[1a] | 2.5[1b] | W |
| | Power Dissipation for Single Operation | $T_A$ = 25 °C | 1.0[1c] | 1.0[1d] | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 57[1a] | 50[1b] | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 125[1c] | 120[1d] | |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 3.5 | 2 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 22OA<br>N9OC | FDMS3600AS | Power 56 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|

### Off Characteristics

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V<br>$I_D$ = 1 mA, $V_{GS}$ = 0 V | Q1<br>Q2 | 25<br>25 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C<br>$I_D$ = 10 mA, referenced to 25 °C | Q1<br>Q2 | | 20<br>18 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>500 | μA<br>μA |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$= 0 V | Q1<br>Q2 | | | 100<br>100 | nA<br>nA |

### On Characteristics

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D$ = 250 μA<br>$V_{GS} = V_{DS}$, $I_D$ = 1 mA | Q1<br>Q2 | 1.1<br>1 | 1.8<br>1.5 | 2.7<br>3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C<br>$I_D$ = 10 mA, referenced to 25 °C | Q1<br>Q2 | | -6<br>-5 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 15 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 14 A<br>$V_{GS}$ = 10 V, $I_D$ = 15 A , $T_J$ = 125 °C | Q1 | | 4.3<br>6.2<br>5.9 | 5.6<br>8.5<br>8.7 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 30 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 25 A<br>$V_{GS}$ = 10 V, $I_D$ = 30 A , $T_J$ = 125 °C | Q2 | | 1.3<br>1.7<br>1.8 | 1.6<br>2.4<br>2.7 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 15 A<br>$V_{DS}$ = 5 V, $I_D$ = 30 A | Q1<br>Q2 | | 67<br>171 | | S |

### Dynamic Characteristics

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | Q1:<br>$V_{DS}$ = 13 V, $V_{GS}$ = 0 V, f = 1 MHZ<br>Q2:<br>$V_{DS}$ = 13 V, $V_{GS}$ = 0 V, f = 1 MHZ | Q1<br>Q2 | | 1330<br>4255 | 1770<br>5660 | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | | 358<br>1270 | 475<br>1690 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 61<br>156 | 90<br>235 | pF |
| $R_g$ | Gate Resistance | | Q1<br>Q2 | 0.2<br>0.2 | 0.6<br>0.9 | 2<br>3 | Ω |

### Switching Characteristics

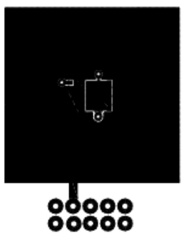
| Symbol | Parameter | Test Conditions | | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-On Delay Time | Q1:<br>$V_{DD}$ = 13 V, $I_D$ = 15 A, $R_{GEN}$ = 6 Ω<br>Q2:<br>$V_{DD}$ = 13 V, $I_D$ = 30 A, $R_{GEN}$ = 6 Ω | | Q1<br>Q2 | | 7.9<br>13 | 16<br>23 | ns |
| $t_r$ | Rise Time | | | Q1<br>Q2 | | 2<br>5.3 | 10<br>11 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | Q1<br>Q2 | | 19<br>38 | 34<br>60 | ns |
| $t_f$ | Fall Time | | | Q1<br>Q2 | | 1.8<br>3.9 | 10<br>10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V | Q1<br>$V_{DD}$ = 13 V,<br>$I_D$ = 15 A<br>Q2<br>$V_{DD}$ = 13 V,<br>$I_D$ = 30 A | Q1<br>Q2 | | 19<br>59 | 27<br>82 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V | | Q1<br>Q2 | | 9<br>27 | 13<br>38 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | Q1<br>Q2 | | 3.9<br>11 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | Q1<br>Q2 | | 2.4<br>5.8 | | nC |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Drain-Source Diode Characteristics** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 15 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 30 A (Note 2) | Q1<br>Q2 | | 0.8<br>0.8 | 1.2<br>1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | Q1<br>$I_F$ = 15 A, di/dt = 100 A/μs<br>Q2<br>$I_F$ = 30 A, di/dt = 300 A/μs | Q1<br>Q2 | | 21<br>32 | 34<br>51 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | Q1<br>Q2 | | 6.6<br>36 | 13<br>58 | nC |

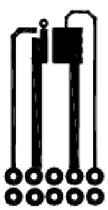
**Notes:**

**1:** $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

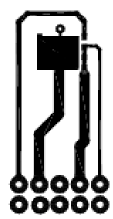


a. 57 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper

b. 50 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

**2:** Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

**3:** As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

**4:** $E_{AS}$ of 50 mJ is based on starting $T_J$ = 25 $^oC$; N-ch: L = 1 mH, $I_{AS}$ = 10 A, $V_{DD}$ = 23 V, $V_{GS}$ = 10 V. 100% test at L=0.3 mH, $I_{AS}$ = 15 A.

**5:** $E_{AS}$ of 200 mJ is based on starting $T_J$ = 25 $^oC$; N-ch: L = 1 mH, $I_{AS}$ = 20 A, $V_{DD}$ = 23 V, $V_{GS}$ = 10 V. 100% test at L=0.3 mH, $I_{AS}$ = 30 A.

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

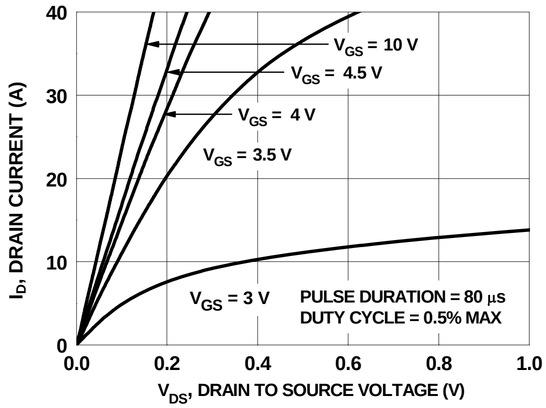



**Figure 1. On Region Characteristics**

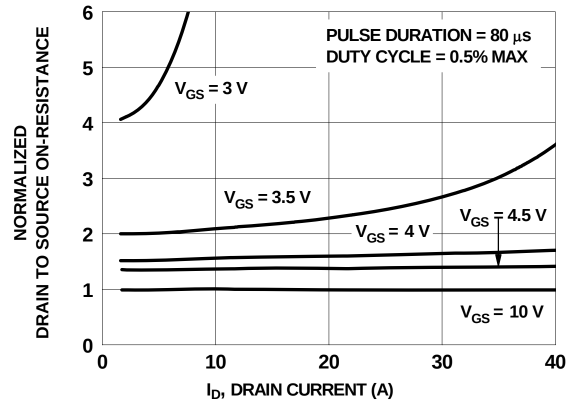



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

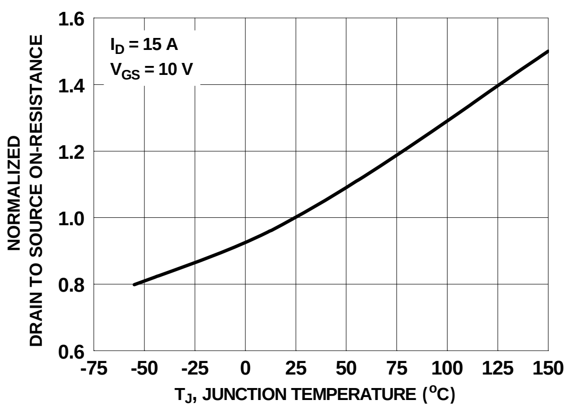



**Figure 3. Normalized On Resistance vs Junction Temperature**

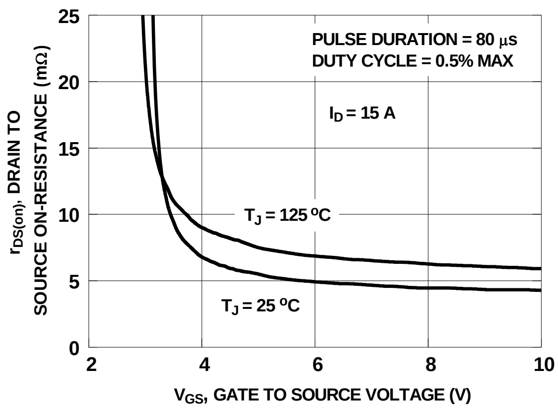



**Figure 4. On-Resistance vs Gate to Source Voltage**

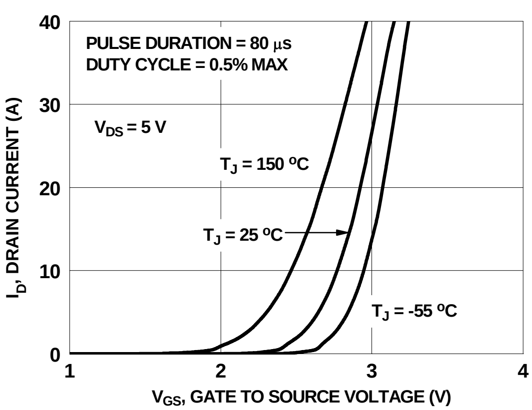



**Figure 5. Transfer Characteristics**

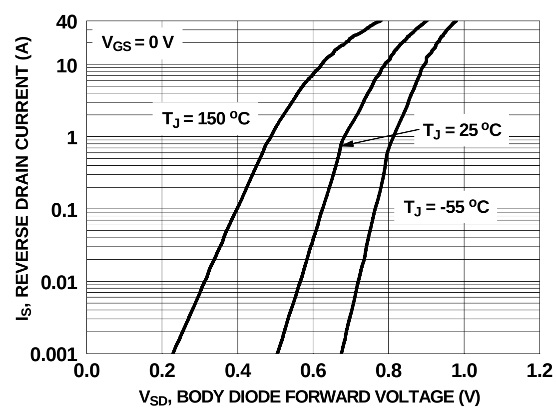



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

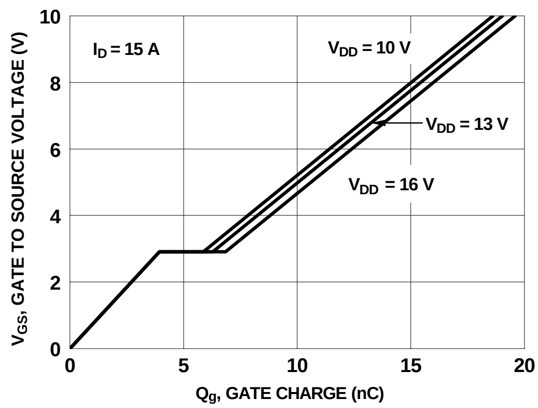



**Figure 7. Gate Charge Characteristics**

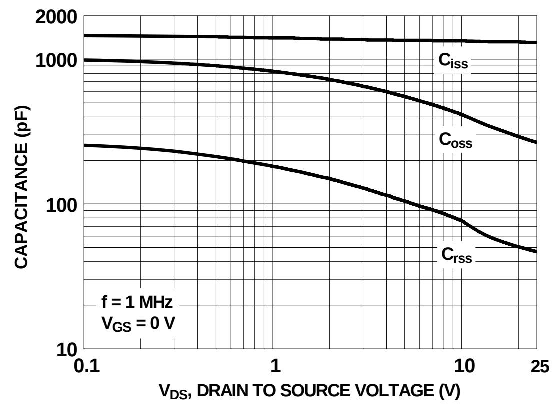



**Figure 8. Capacitance vs Drain to Source Voltage**

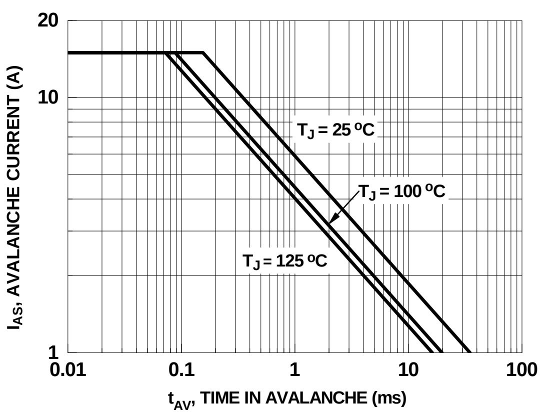



**Figure 9. Unclamped Inductive Switching Capability**

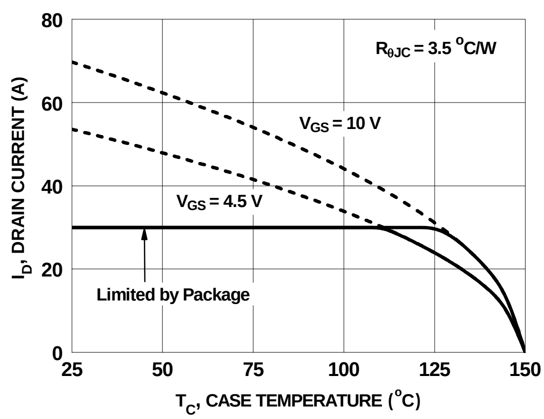



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

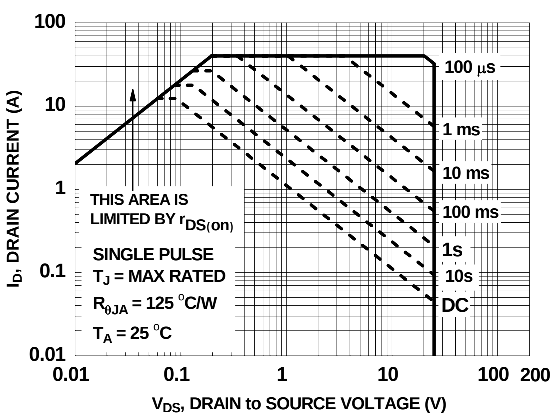



**Figure 11. Forward Bias Safe Operating Area**

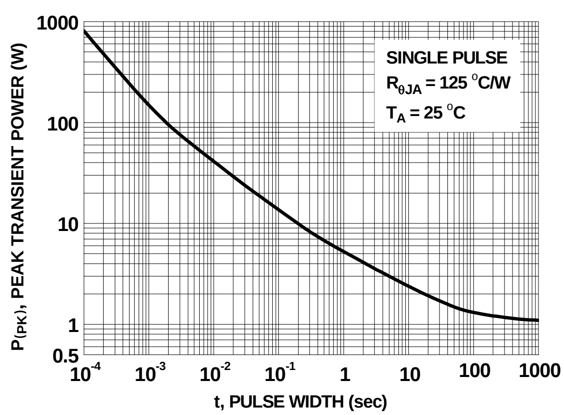



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25 °C unless otherwise noted

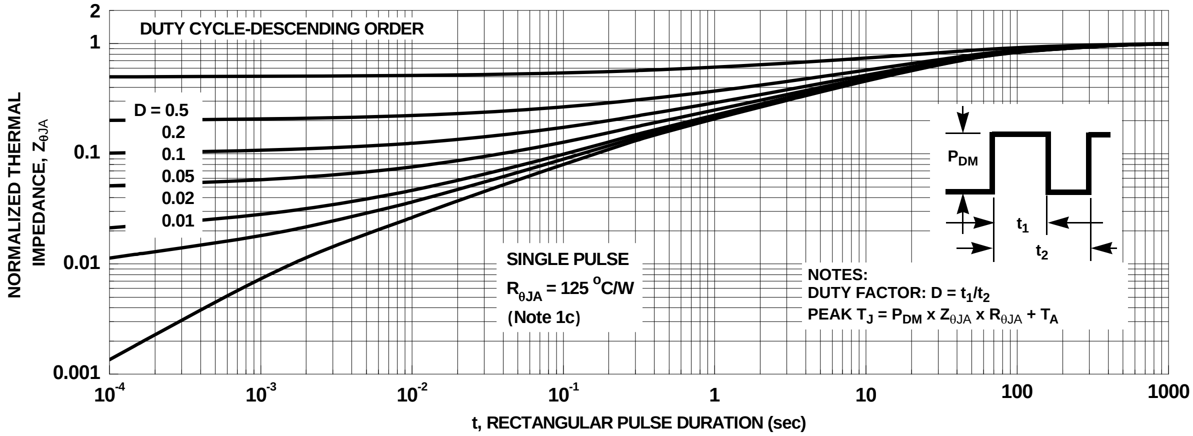



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

## Typical Characteristics (Q2 N-Channel) $T_J$ = 25 °C unlenss otherwise noted

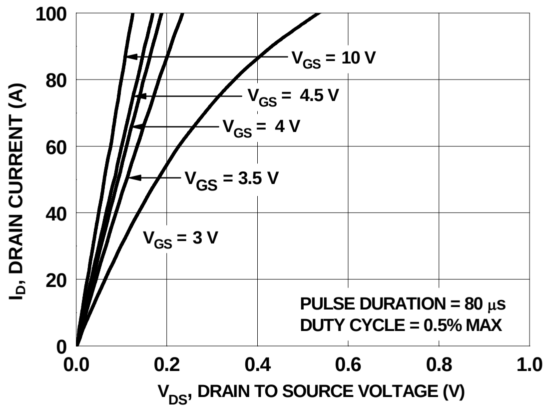



Figure 14. On-Region Characteristics

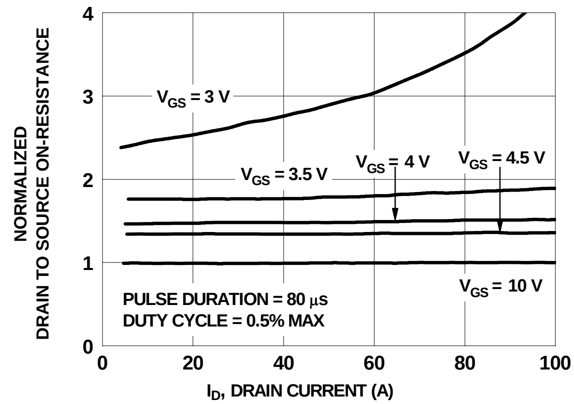



Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

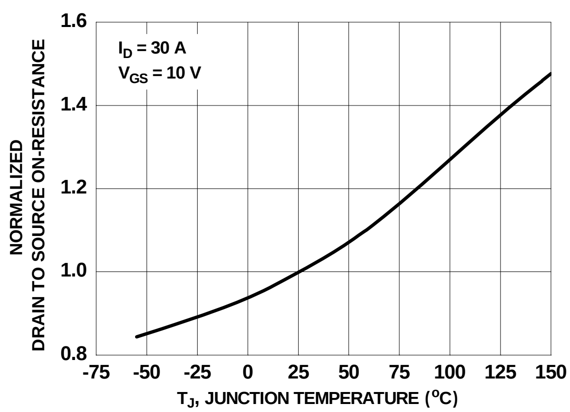



Figure 16. Normalized On-Resistance vs Junction Temperature

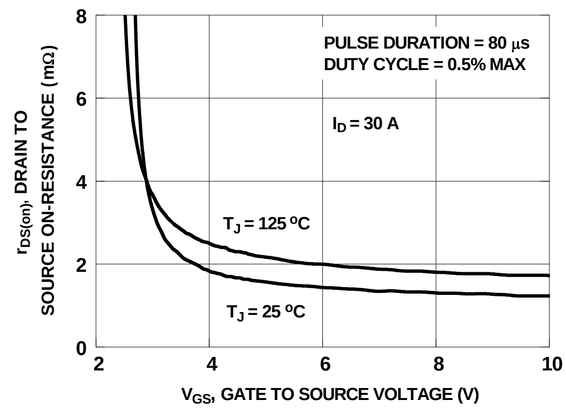



Figure 17. On-Resistance vs Gate to Source Voltage

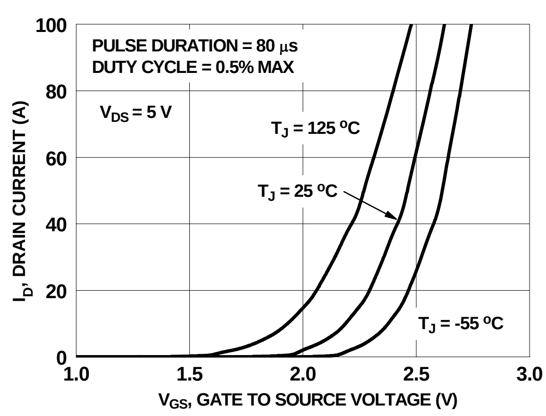



Figure 18. Transfer Characteristics

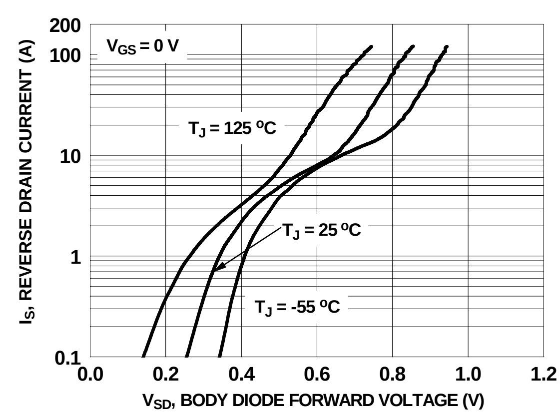



Figure 19. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics (Q2 N-Channel) $T_J$ = 25 °C unless otherwise noted

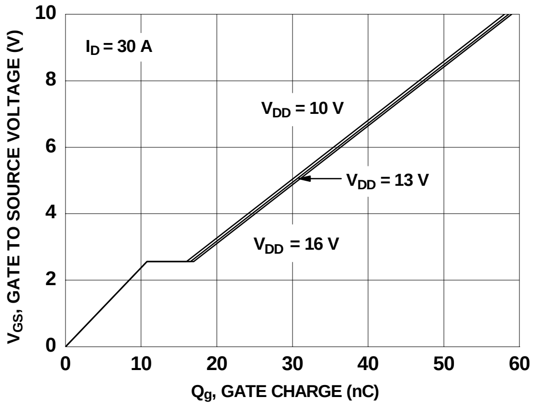



**Figure 20. Gate Charge Characteristics**

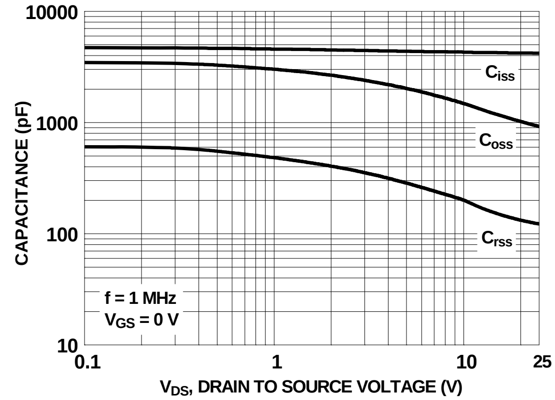



**Figure 21. Capacitance vs Drain to Source Voltage**

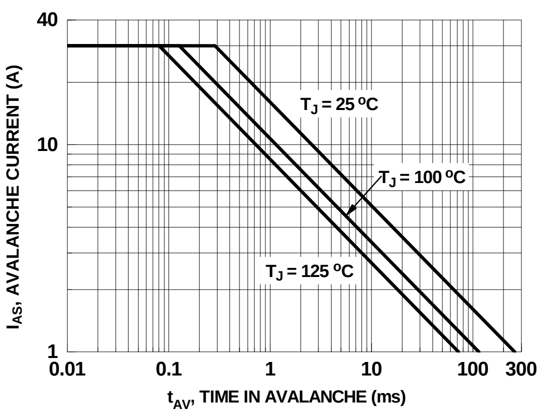



**Figure 22. Unclamped Inductive Switching Capability**

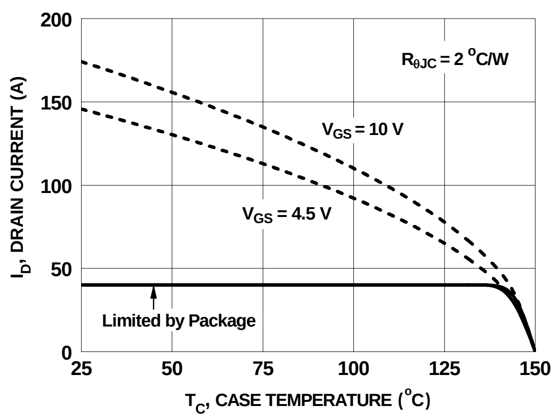



**Figure 23.Maximun Continuous Drain Current vs Case Temperature**

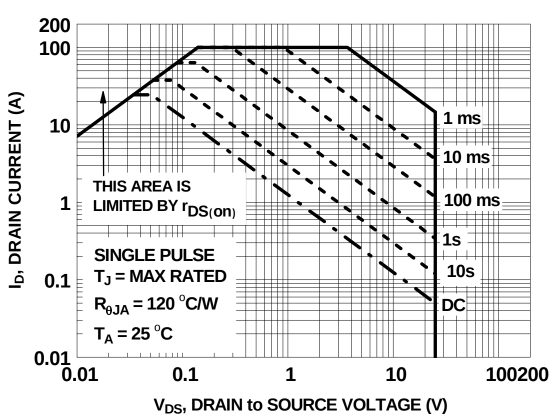



**Figure 24. Forward Bias Safe Operating Area**

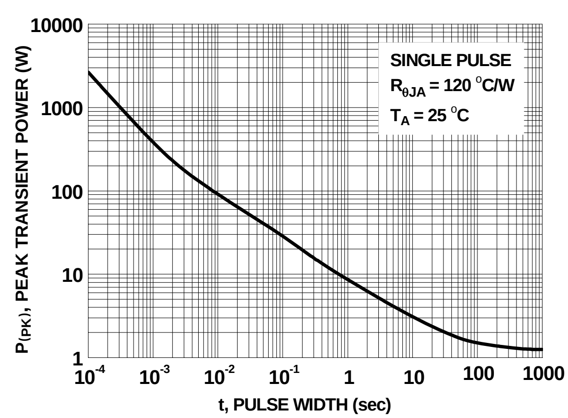



**Figure 25. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q2 N-Channel) $T_J = 25\ ^oC$ unless otherwise noted

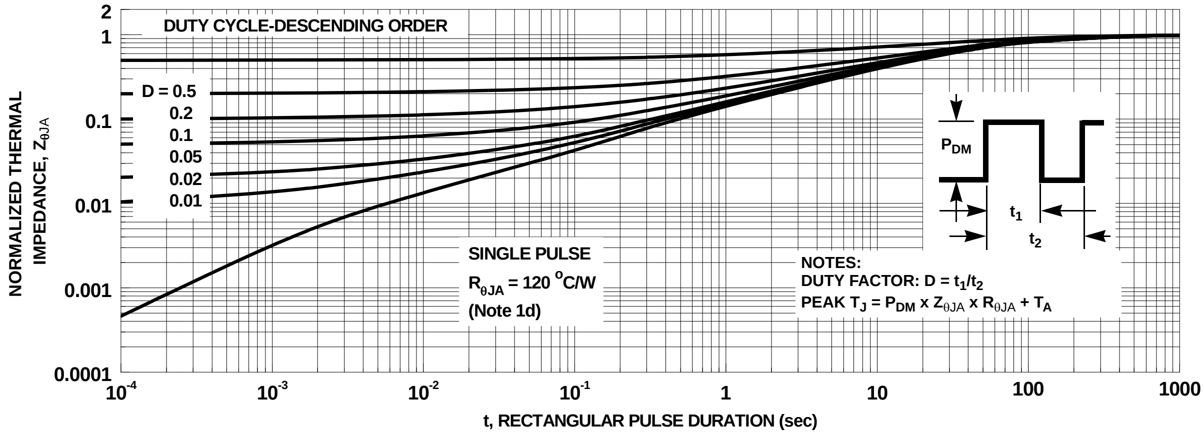


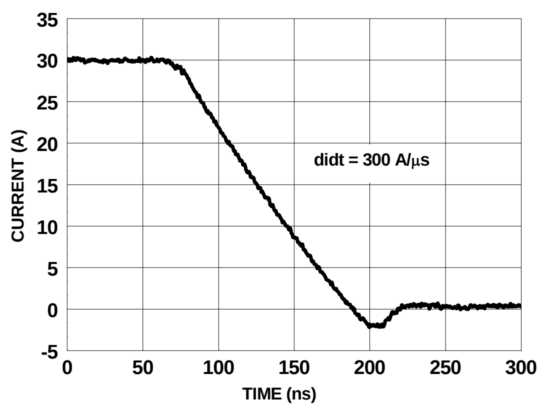

**Figure26. Junction-to-Ambient Transient Thermal Response Curve**

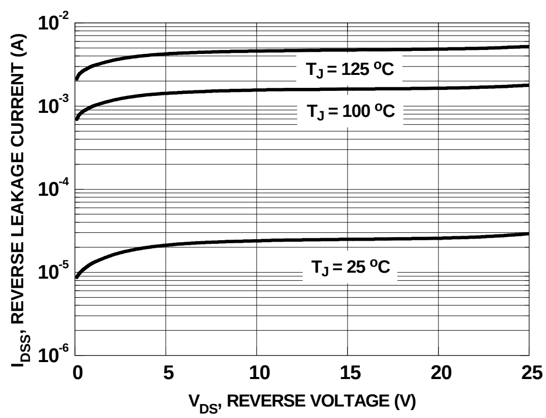
## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3600AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

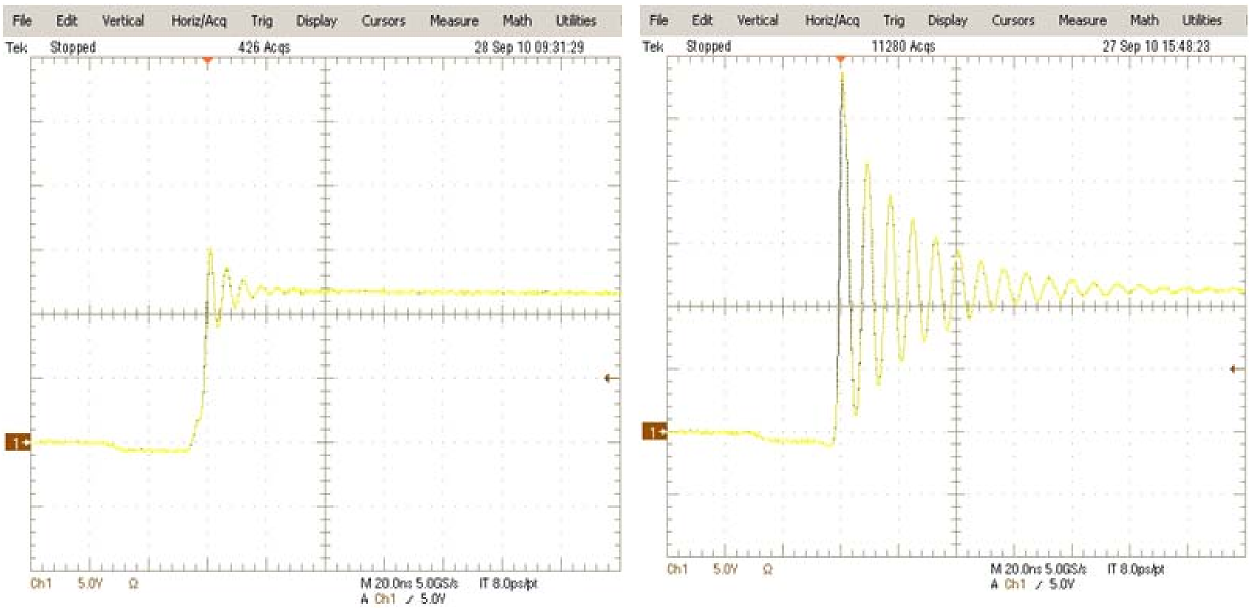


## Application Information

### 1. Switch Node Ringing Suppression

Fairchild's Power Stage products incorporate a proprietary design* that minimizes the peak overshoot, ringing voltage on the switch node (PHASE) without the need of any external snubbing components in a buck converter. As shown in the figure 29, the Power Stage solution rings significantly less than competitor solutions under the same set of test conditions.




**Power Stage Device** **Competitors solution**

**Figure 29. Power Stage phase node rising edge, High Side Turn on**

*Patent Pending

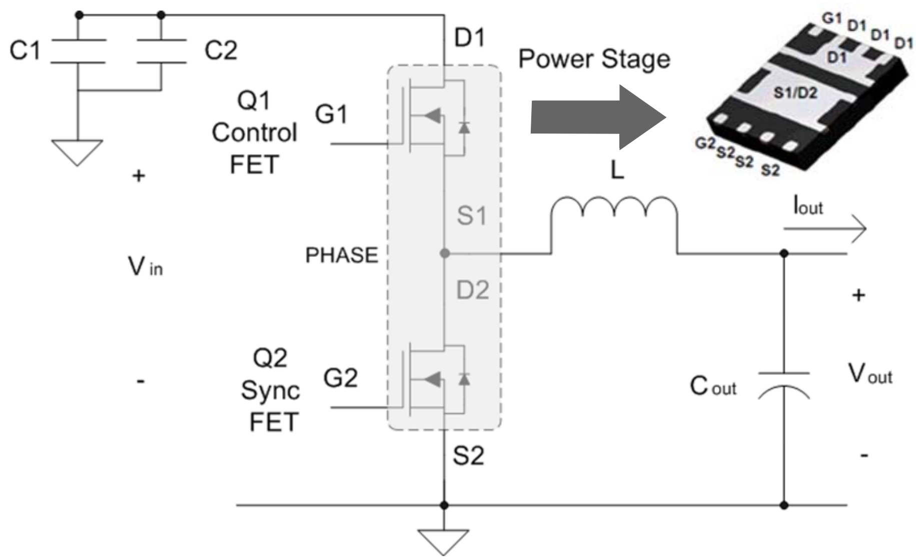
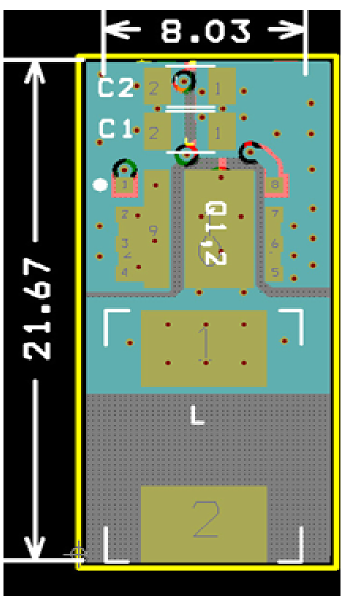


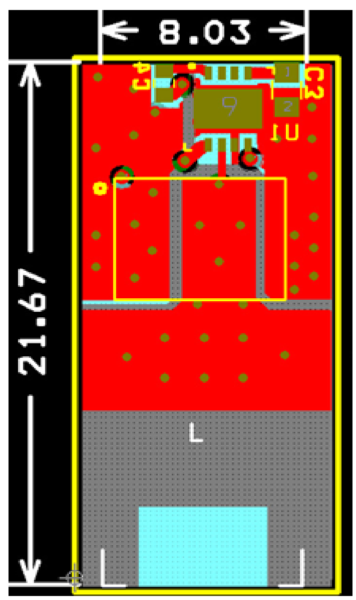

**Figure 30. Shows the Power Stage in a buck converter topology**

## 2. Recommended PCB Layout Guidelines

As a PCB designer, it is necessary to address critical issues in layout to minimize losses and optimize the performance of the power train. Power Stage is a high power density solution and all high current flow paths, such as VIN (D1), PHASE (S1/D2) and GND (S2), should be short and wide for better and stable current flow, heat radiation and system performance. A recommended layout procedure is discussed below to maximize the electrical and thermal performance of the part.




Top Layer




Bottom Layer

**Figure 31. Recommended PCB Layout**

**Following is a guideline, not a requirement which the PCB designer should consider:**

1. Input ceramic bypass capacitors C1 and C2 must be placed close to the D1 and S2 pins of Power Stage to help reduce parasitic inductance and High Frequency conduction loss induced by switching operation. C1 and C2 show the bypass capacitors placed close to the part between D1 and S2. Input capacitors should be connected in parallel close to the part. Multiple input caps can be connected depending upon the application.

2. The PHASE copper trace serves two purposes; In addition to being the current path from the Power Stage package to the output inductor (L), it also serves as heat sink for the lower FET in the Power Stage package. The trace should be short and wide enough to present a low resistance path for the high current flow between the Power Stage and the inductor. This is done to minimize conduction losses and limit temperature rise. Please note that the PHASE node is a high voltage and high frequency switching node with high noise potential. Care should be taken to minimize coupling to adjacent traces. The reference layout in figure 31 shows a good balance between the thermal and electrical performance of Power Stage.

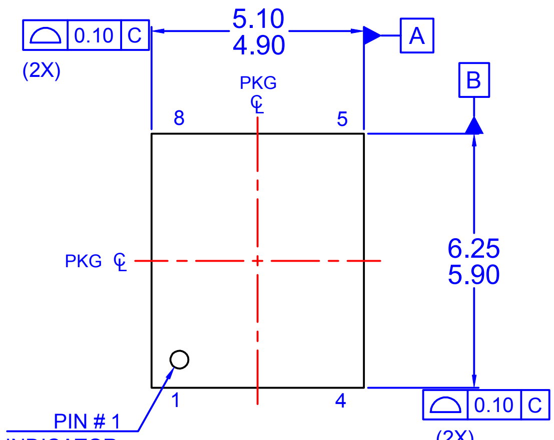
3. Output inductor location should be as close as possible to the Power Stage device for lower power loss due to copper trace resistance. A shorter and wider PHASE trace to the inductor reduces the conduction loss. Preferably the Power Stage should be directly in line (as shown in figure 31) with the inductor for space savings and compactness.

4. The PowerTrench® Technology MOSFETs used in the Power Stage are effective at minimizing phase node ringing. It allows the part to operate well within the breakdown voltage limits. This eliminates the need to have an external snubber circuit in most cases. If the designer chooses to use an RC snubber, it should be placed close to the part between the PHASE pad and S2 pins to dampen the high-frequency ringing.

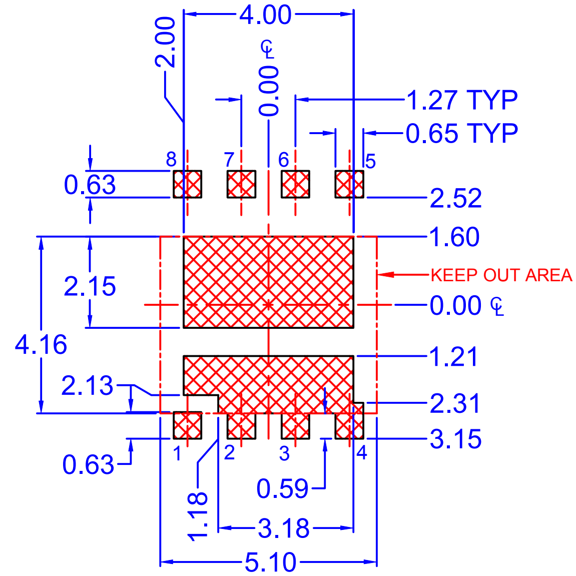
5. The driver IC should be placed close to the Power Stage part with the shortest possible paths for the High Side gate and Low Side gates through a wide trace connection. This eliminates the effect of parasitic inductance and resistance between the driver and the MOSFET and turns the devices on and off as efficiently as possible. At higher-frequency operation this impedance can limit the gate current trying to charge the MOSFET input capacitance. This will result in slower rise and fall times and additional switching losses. Power Stage has both the gate pins on the same side of the package which allows for back mounting of the driver IC to the board. This provides a very compact path for the drive signals and improves efficiency of the part.

6. S2 pins should be connected to the GND plane with multiple vias for a low impedance grounding. Poor grounding can create a noise transient offset voltage level between S2 and driver ground. This could lead to faulty operation of the gate driver and MOSFET.

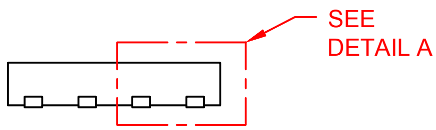
7. Use multiple vias on each copper area to interconnect top, inner and bottom layers to help smooth current flow and heat conduction. Vias should be relatively large, around 8 mils to 10 mils, and of reasonable inductance. Critical high frequency components such as ceramic bypass caps should be located close to the part and on the same side of the PCB. If not feasible, they should be connected from the backside via a network of low inductance vias.



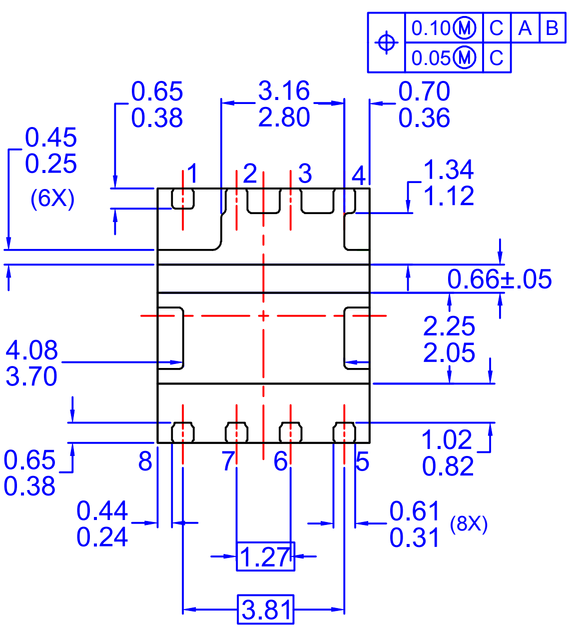

TOP VIEW




RECOMMENDED LAND PATTERN
FOR SAWN / PUNCHED TYPE

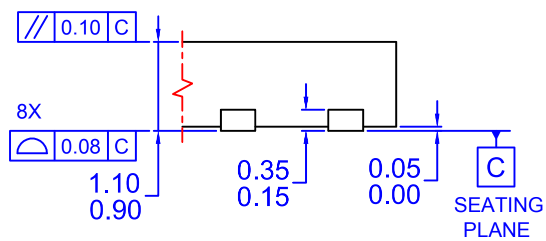



SIDE VIEW




BOTTOM VIEW

OPTION - A (SAWN TYPE)




DETAIL 'A'
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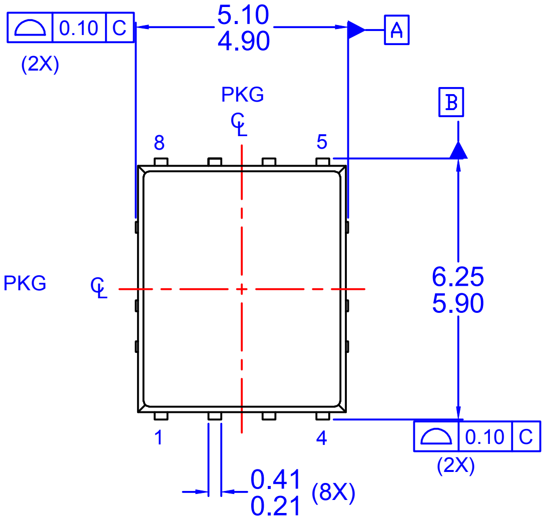
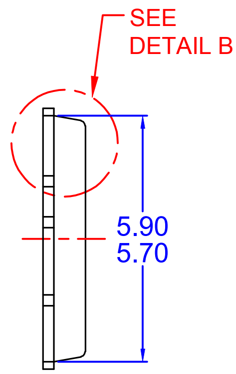
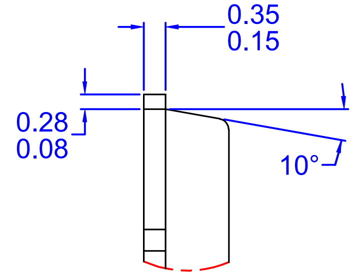
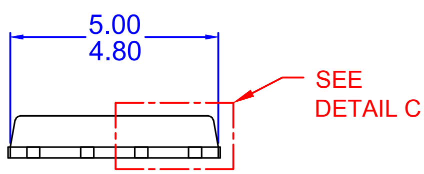



TOP VIEW

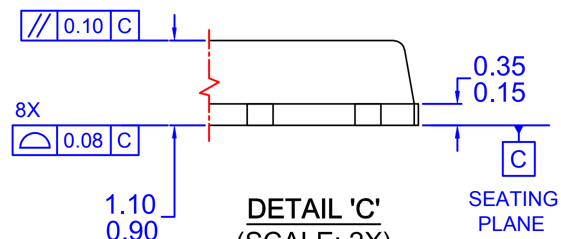


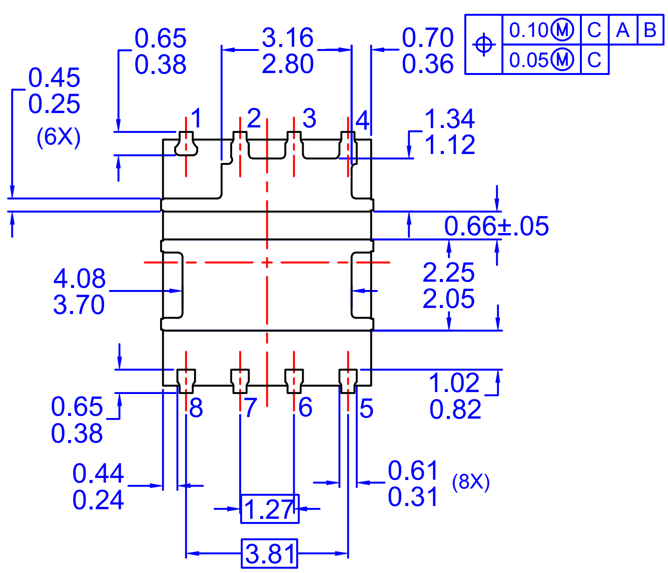

DETAIL 'B'
(SCALE: 2X)




SIDE VIEW




DETAIL 'C'
(SCALE: 2X)




BOTTOM VIEW

OPTION - B (PUNCHED TYPE)

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: PQFN08EREV6.

G) FAIRCHILD SEMICONDUCTOR

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