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DOCUMENT DESCRIPTION

Schematic Checklist for the LAN8741, 32-pin QFN Package

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Document Number	Revision
SC471241	A

Schematic Checklist for LAN8741

Information Particular for the 32-pin QFN Package

LAN8741 QFN Phy Interface:

1. TXP (pin 29); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDDA (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TXN (pin 28); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDDA (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. RXP (pin 31); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDDA (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. RXN (pin 30); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDDA (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

7. For added EMC flexibility in a LAN8741 design, the designer should include four low valued capacitors on the TXP, TXN, RXP & RXN pins. Low valued capacitors (less than 15 ρF) can be added to each line and terminated to digital ground. These components can be added to the schematic and should be designated as Do Not Populate (DNP).

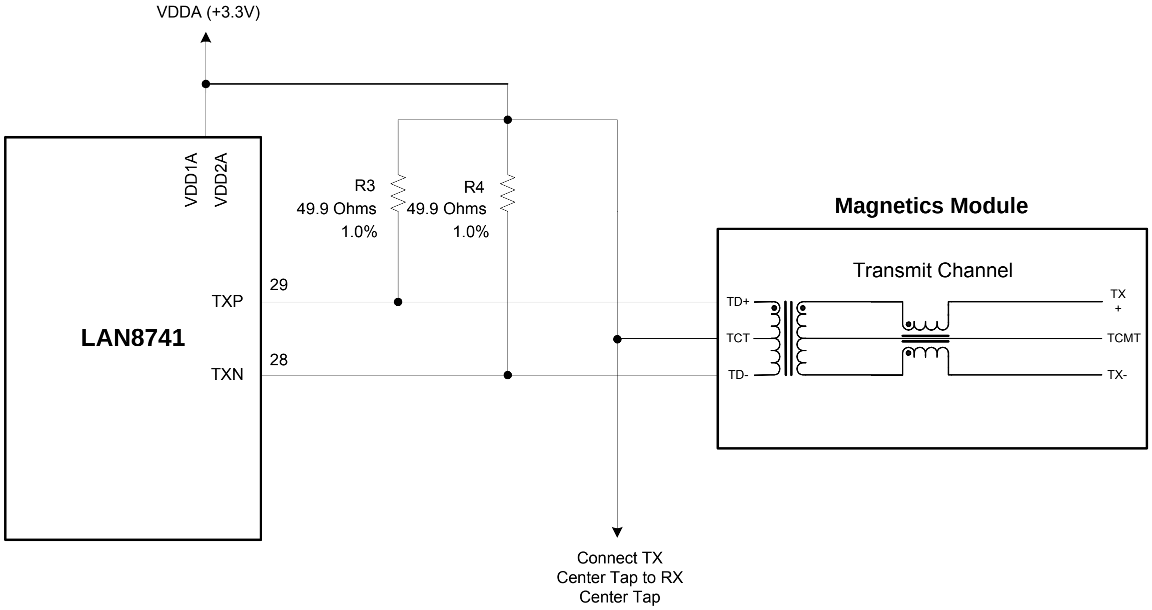


Figure 1 – Transmit Channel Connections and Terminations

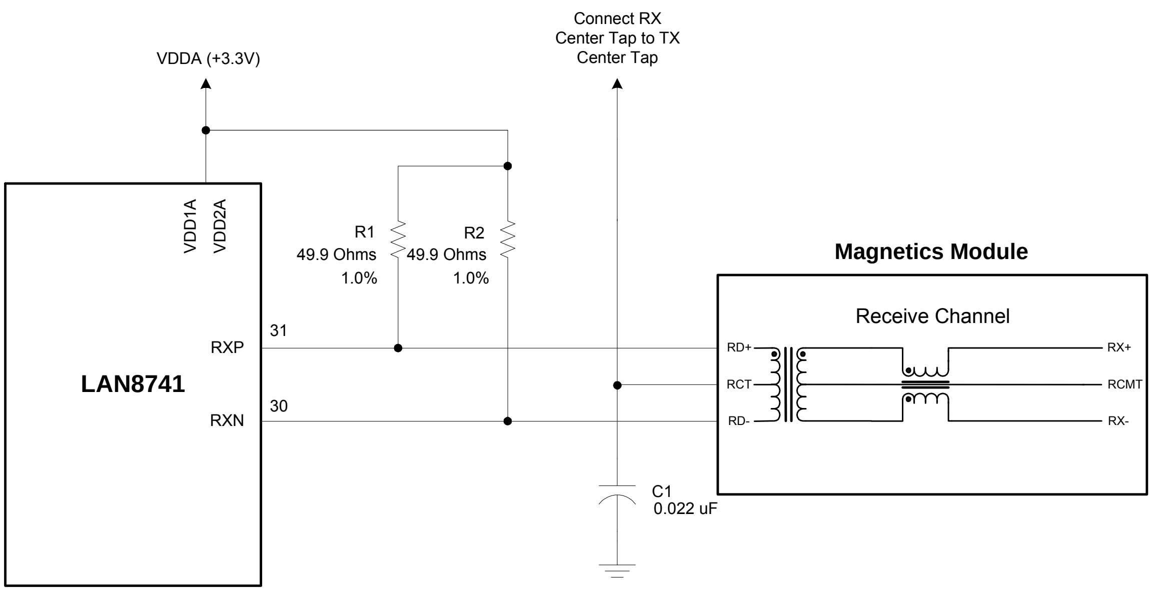


Figure 2 - Receive Channel Connections and Terminations

LAN8741 QFN Magnetics:

1. The center tap connection on the LAN8741 side for the transmit channel must be connected to VDDA (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN8741 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 29) of the LAN8741 QFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN (pin 28) of the LAN8741 QFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 31) of the LAN8741 QFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN (pin 30) of the LAN8741 QFN.

10. When using the SMSC LAN8741 device in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

   a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

   b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

   a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

   b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Power Supply Connections:

1. The analog supply (VDD1A & VDD2A) pins on the LAN8741 QFN are 1 & 27. They require a connection to VDDA (created from +3.3V through a ferrite bead). Be sure to place bulk capacitance on each side of the ferrite bead.

   Note: Pins 1 & 27 (VDD1A & VDD2A) must always be connected to a +3.3V power supply; even in the case of having the internal +1.2V regulator of the LAN8741 disabled. Other blocks within the LAN8741 require power from +3.3V.

2. Each VDDxA pin should have one .01 µF (or smaller) capacitor to decouple the LAN8741. The capacitor size should be SMD_0603 or smaller.

3. Pin 12 (VDDIO) is a variable supply voltage for the I/O pads. This pin must be connected to a voltage supply between +1.8V and +3.3V.

4. The VDDIO pin should have one .01 µF (or smaller) capacitor to decouple the LAN8741. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. The digital ground pins (GND), the analog ground pins (AVSS) and the GND_CORE pins on the LAN8741 QFN are all connected internally to the exposed die paddle ground. The EDP Ground pad on the underside of the LAN8741 must be connected directly to a solid, contiguous digital ground plane.

2. We recommend that all Ground connections be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

VDDCR:

1. VDDCR (pin 6), this pin is used to provide bypassing for the +1.2V core regulator. This pin requires a 470 ρF bypass capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 6 requires a bulk capacitor placed as close as possible to pin 6. The bulk capacitor must have a value of at least 1.0 µF, and have an ESR (equivalent series resistance) of no more than 1.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

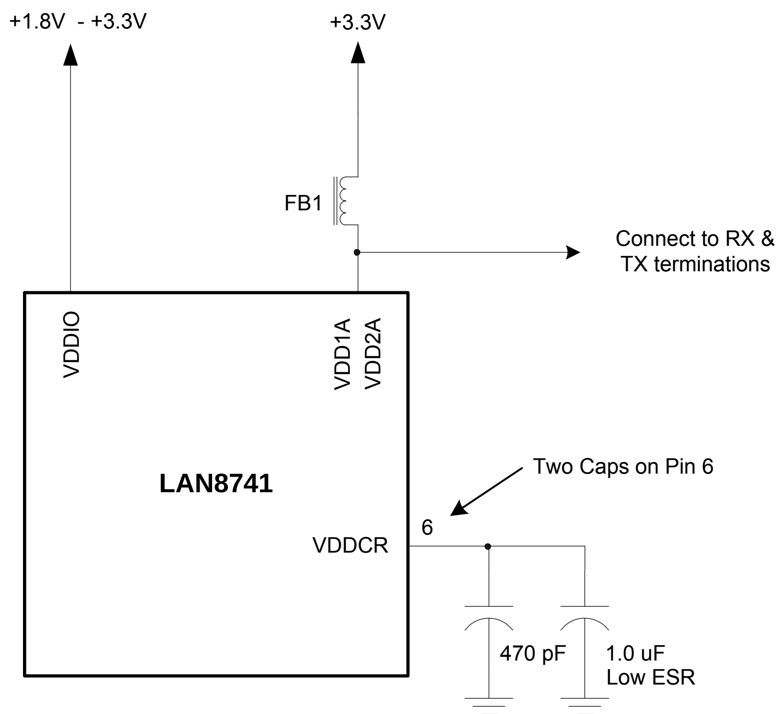


Figure 3 - LAN8741 Power Connections

Crystal Connections:

1. When using the LAN8741 QFN in MII mode, a 25.000 MHz crystal should be used to provide the clock source. For exact specifications and tolerances refer to the latest revision of the LAN8741 data sheet.

2. XTAL1/CLKIN (pin 5) on the LAN8741 QFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 4) on the LAN8741 QFN is the clock circuit output. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

4. Since every system design is unique, the value for the capacitors are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN8741 QFN.

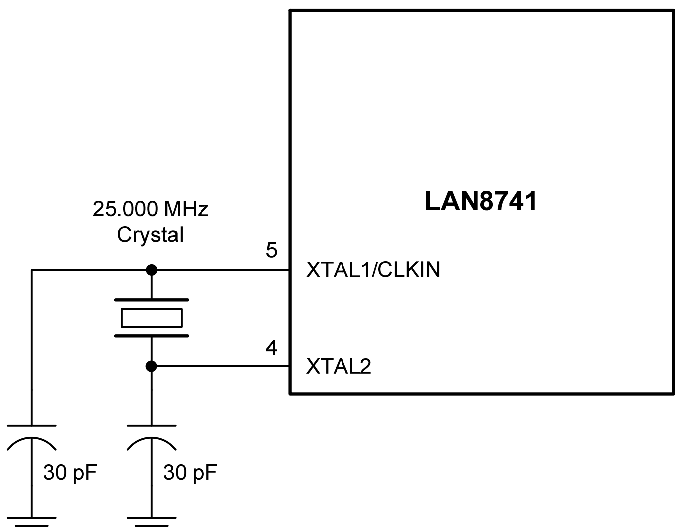


Figure 4 – LAN8741 Crystal Connections

Clock Oscillator Connections:

1. A 50.000 MHz clock oscillator may be used to provide the clock source for the LAN8741. The clock oscillator must provide a 50.000 MHz clock for the PHY and RMII MAC in the design. For exact specifications and tolerances refer to the latest revision LAN8741 data sheet.

2. In order to provide two copies of the 50.000 MHz clock, it is recommended that the designer use two series 33 Ω resistors. The values can then be adjusted to compensate for any PCB trace inconsistencies.

3. XTAL1/CLKIN (pin 5) on the LAN8741 QFN is the clock circuit input. With low VDDIO voltages (+1.8V), CLKIN voltage may range from +1.8V to +3.3V.

4. XTAL2 (pin 4) on the LAN8741 QFN is the clock circuit output. When using a single ended clock source, this pin can be left floating as a No Connect (NC).

5. Since every system design is unique, the PCB design, oscillator selected, and layout all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, stability, and voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

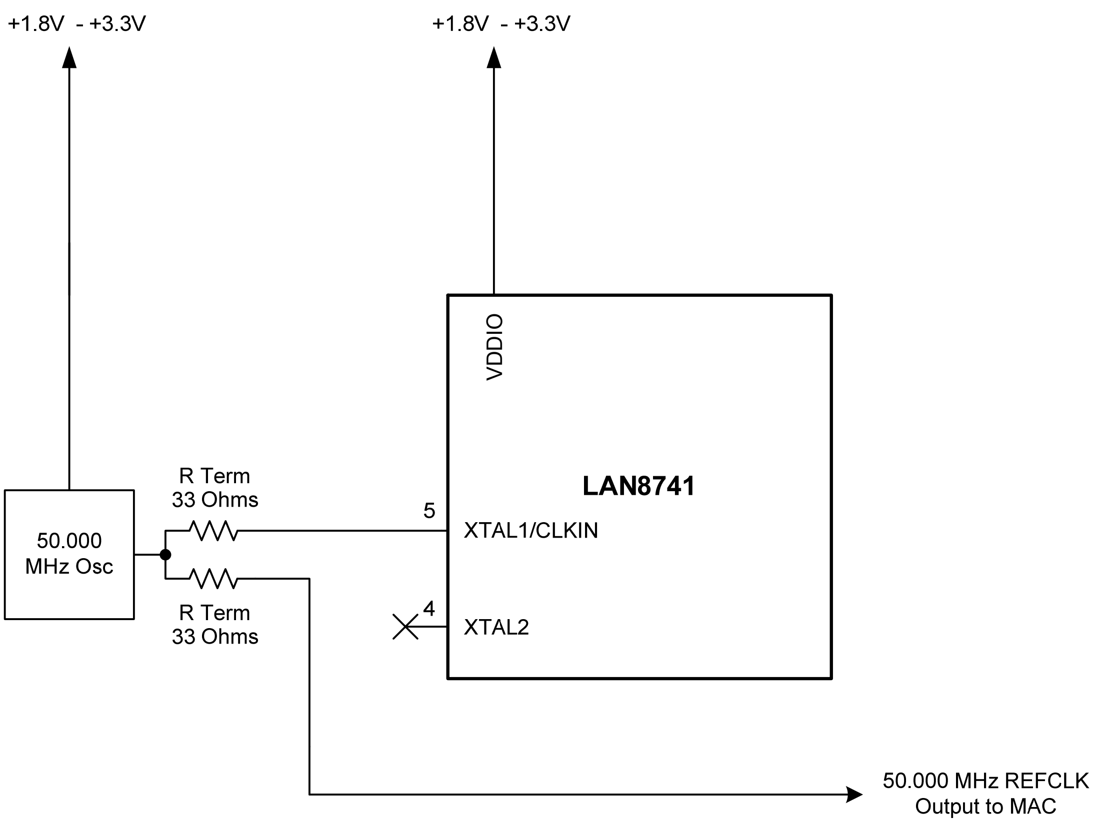


Figure 5 – LAN8741 Clock Oscillator Connections

MAC REFCLK Connections:

1. A 50.000 MHz REFCLK output from the MAC may be used to provide the clock source for the LAN8741. For exact specifications and tolerances refer to the latest revision LAN8741 data sheet.

2. It is recommended that the designer use a series 33 Ω resistor at the MAC to connect to the Phy. The value can then be adjusted to compensate for any PCB trace inconsistencies.

3. XTAL1/CLKIN (pin 5) on the LAN8741 QFN is the clock circuit input. With low VDDIO voltages (+1.8V), CLKIN voltage may range from +1.8V to +3.3V.

4. XTAL2 (pin 4) on the LAN8741 QFN is the clock circuit output. When using a single ended clock source, this pin can be left floating as a No Connect (NC).

5. Since every system design is unique, the PCB design and layout all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, stability, and voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

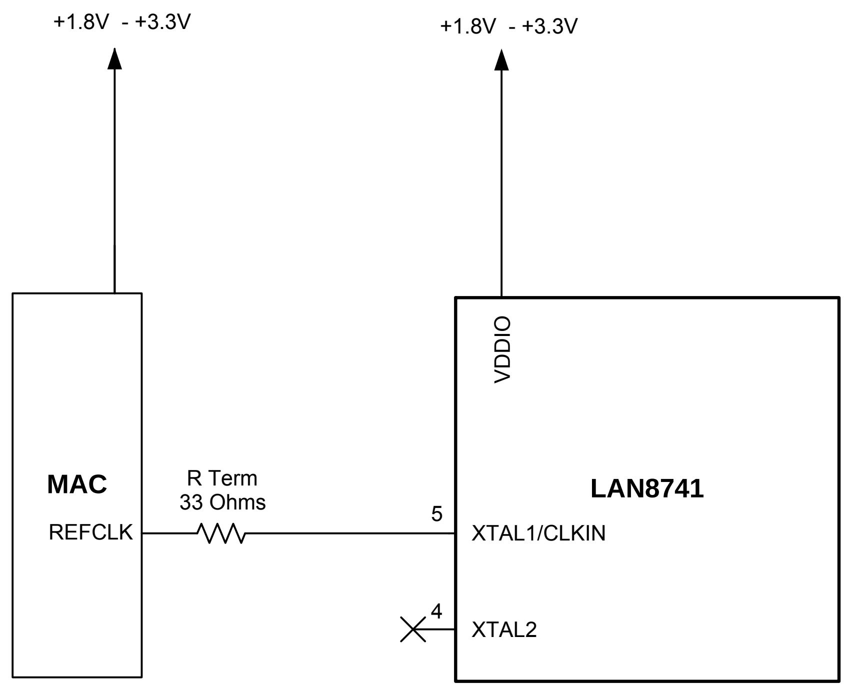


Figure 6 – LAN8741 MAC REFCLK Connections

RBIAS Resistor:

1. RBIAS (pin 32) on the LAN8741 QFN should connect to digital ground through a 12.1K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

MII Interface:

1. When utilizing either an external MII MAC interface or an MII Connector, the following table indicates the proper connections for the 18 signals.

From:	Connects To:	
LAN8741 QFN	**MII MAC Device**	**MII Connector**
RXD0 (pin 11)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 10)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 9)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 8)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 26)	RX_DV	RX_DV (contact 8)
RX_ER (pin 13)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 7)	RX_CLK	RX_CLK (contact 9)
TX_ER (pin 18)	TX_ER	TX_ER (contact 11)
TXD0 (pin 22)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 23)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 24)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 25)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 21)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 20)	TX_CLK	TX_CLK (contact 12)
CRS (pin 14)	CRS	CRS (contact 19)
COL (pin 15)	COL	COL (contact 18)
MDIO (pin 16)	MDIO	MDIO (contact 2)
MDC (pin 17)	MDC	MDC (contact 3)

2. RMIISEL (pin 9) this defines the MII/RMII Bus operation of the LAN8741. A low on this pin configures the LAN8741 for normal MII Bus operation. This input is latched on the rising edge of reset. This pin has a weak internal pull-down and can be left as a no-connect for MII Bus operation.

3. TXER/TXD4 (pin 18) this pin provides the transmit error functionality on the MII Bus interface (if required). To enable the TXER functionality on pin 18, the LED2/nINTSEL pin (pin 2) must be pulled down through an external 10.0K resistor to ground. The LED2/nINTSEL pin has a weak internal pull-up and must be pulled low externally to select the TXER functionality.

4. Provisions should be made for series terminations for all outputs on the MII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8741 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 100.0 Ω.

RMII Interface:

1. When utilizing an external RMII MAC interface, the following table indicates the proper connections for the 9 signals.

From:	Connects To:	
LAN8741 QFN	**RMII MAC Device**	**Notes**
RXD0 (pin 11)	RXD<0>	
RXD1 (pin 10)	RXD<1>	
RXD2 (pin 9)	RXD<2>	Not Used in RMII Mode
RXD3 (pin 8)	RXD<3>	Not Used in RMII Mode
RX_DV (pin 26)	RX_DV	Not Used in RMII Mode
RX_ER (pin 13)	RX_ER	This signal is optional in RMII Mode
RX_CLK (pin 7)	RX_CLK	Not Used in RMII Mode
TX_ER (pin 18)	TX_ER	Not Used in RMII Mode
TXD0 (pin 22)	TXD<0>	
TXD1 (pin 23)	TXD<1>	
TXD2 (pin 24)	TXD<2>	Not Used in RMII Mode; TXD2 Should be grounded
TXD3 (pin 25)	TXD<3>	Not Used in RMII Mode; TXD3 Should be grounded
TX_EN (pin 21)	TX_EN	
TX_CLK (pin 20)	TX_CLK	Not Used in RMII Mode
CRS_DV (pin 15)	CRS_DV	
CRS (pin 14)	CRS	Not Used in RMII Mode
COL (pin 15)	COL	
MDIO (pin 16)	MDIO	
MDC (pin 17)	MDC	

2. RMIISEL (pin 9) this defines the MII/RMII Bus operation of the LAN8741. A high on this pin configures the LAN8741 for RMII Bus operation. This input is latched on the rising edge of reset. Since this pin has a weak internal pull-down, an external pull-up resistor must be used to configure the LAN8741 for RMII Bus operation. A 10.0K pull-up to VDDIO on this pin will configure the phy for RMII mode.

3. Provisions should be made for series terminations for all outputs on the RMII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN8741 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependant and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω.

MII/RMII Series Terminations:

	Series Terminations	
Signal	**MII Mode**	**RMII Mode**
RXD0	100 Ω	10 Ω
RXD1	100 Ω	10 Ω
RXD2	100 Ω	n/a
RXD3	100 Ω	n/a
RX_CLK	100 Ω	n/a
RX_ER	100 Ω	10 Ω
RX_DV	100 Ω	n/a
CRS_DV	n/a	10 Ω
COL	100 Ω	n/a
CRS	100 Ω	n/a
TX_CLK	100 Ω	n/a

Required External Pull-ups:

1. nINT (pin 18) requires an external pull-up resistor to VDDIO as this output is an Open Drain type.

2. When using the MII or the RMII interface of the LAN8741 QFN with a MAC device on board, a pull-up resistor on the MDIO signal (pin 16) is required. A pull-up resistor of 1.5KΩ to VDDIO is required for this application.

Mode Pins:

1. The Mode pins of the LAN8741 (MODE[2:0]) control the default configuration of the 10/100 phy. Speed, Duplex, Auto-Negotiation & power down functionality can be configured through these pins. The value of these three pins are latched in upon power-up and reset. The values latched in are reflected in Register 0 & Register 4 of the LAN8741. See the LAN8741 data sheet for complete details for the operation of these pins. These three pins have weak internal pull-ups and can be left as no-connects. To set any Mode bit low, an external 10K pull-down resistor should be used.

Phy Address Pins:

1. The Phy Address pins of the LAN8741 (PHYAD[2:0]) determine which of 8 Phy addresses of the 32 possible addresses the LAN8741 will respond to. The value of these three pins are latched in upon power-up and reset. The values latched in are reflected in Register 18 of the LAN8741. See the LAN8741 data sheet for complete details for the operation of these pins. These three pins have weak internal pull-downs and can be left as no-connects. To set any Phy Address bit high, an external 10K pull-up resistor to VDDIO should be used. Address bits PHYAD3 & PHYAD4 are tied low inside the LAN8741.

2. A basic Phy Address of 01h is usually recommended.

3. The Phy Address pins are shared with three MII signals on the LAN8741. The pinouts are as follows:

   Phy Address 0 is shared with RX_ER on pin 13.
   Phy Address 1 is shared with RX_CLK on pin 7.
   Phy Address 2 is shared with RXD3 on pin 8.
   Phy Address 3 is tied low.
   Phy Address 4 is tied low.

LED Pins:

1. The LAN8741 provides two LED signals. These indicators will display speed, link and activity information about the current state of the Phy. The LED outputs have the ability to be either active high or active low. The polarity is determined by the level latched in at nRST or POR. The LAN8741 senses each strap level value and changes the polarity of the LED signal accordingly. If the strap value is set as a level one, the LED polarity will be set to an active-low. If the strap value is set as a level zero, the LED polarity will be set to an active high. See the LAN8741 data sheet for further details on how to strap each pin for correct operation and LED polarity outcomes.

2. The LED functionality signal pins are shared with the REGOFF & nINTSEL functionality of the LAN8741. The pinouts are as follows:

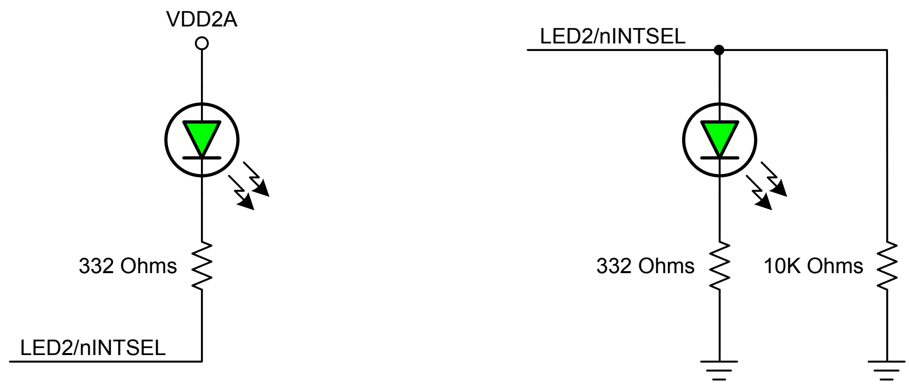
   LED1 is shared with REGOFF on pin 3.
   LED2 is shared with nINTSEL on pin 2.

Interrupt Functionality:

1. For added flexibility, the LAN8741 QFN has a discrete interrupt line for embedded applications. This is advantageous as there is no interrupt facility across the standard MII Bus interface.

2. nINT (pin 18) this pin provides the interrupt signal from the LAN8741. To enable the interrupt functionality on pin 18, the LED2/nINTSEL pin (pin 2) must be left as a no-connection. The LED2/nINTSEL pin has a weak internal pull-up and therefore can be left as a no-connect to select the interrupt functionality. The LED2/nINTSEL level is latched in on POR or nRST.

3. When the LED2/nINTSEL pin (pin 2) is used in conjunction with a LED, refer to Figure 7 below for details.



nINTSEL Bit = 1

LED Output Signal from LAN8741 is Active Low

Interrupt Functionality Selected for Pin 18

nINTSEL Bit = 0

LED Output Signal from LAN8741 is Active High

TX_ER/TXD4 Functionality Selected for Pin 18

Figure 7 Interrupt Select / LED Polarity

EEE Considerations:

1. EEE functionality is only available in systems utilizing the entire MII bus. EEE is not possible when using the RMII interface.

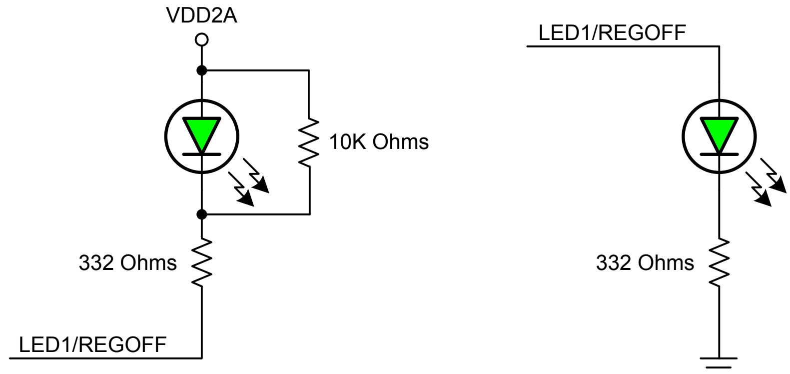
2. The TX_ER signal is required for EEE signaling and must be utilized on the MII bus.

3. Both the Phy and the MAC must support the EEE in order to enable the EEE functionality.

Miscellaneous:

1. REGOFF (pin 3) this pin enables/disables the internal +1.2V core regulator of the LAN8741. This pin has a weak internal pull-down and can be left as a no-connect to enable the internal +1.2V regulator. To disable the +1.2V regulator, this pin should be pulled high with a 10.0K resistor to VDD2A. The REGOFF level is latched in on POR only.

2. When the LED1/REGOFF pin (pin 3) is used in conjunction with a LED, refer to Figure 8 below for details.



REGOFF Bit = 1

LED Output Signal from LAN8741 is Active Low

Internal +1.2V Core Regulator is Disabled

REGOFF Bit = 0

LED Output Signal from LAN8741 is Active High

Internal +1.2V Core Regulator is Enabled (Default)

Figure 8 REGOFF / LED Polarity

3. nRST (pin 19), this pin is an active-low reset input. This signal resets all logic and registers within the LAN8741. This pin has a weak internal pull-up termination. A hardware reset (nRST assertion) is required following power-up. Please refer to the latest copy of the LAN8741 data sheet for reset timing requirements. SMSC does not recommend the use of an RC circuit for this required pin reset. A reset generator / voltage monitor is one option to provide a proper reset. Better yet, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, SMSC recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

4. Due to possible lower I/O voltages used on the LAN8741, lower strapping resistor values need to be used to ensure the strapped configuration is properly latched into the phy device upon power-on reset. Refer to the latest revision of the LAN8741 QFN data sheet for details of proper resistor values when using lower I/O voltages on VDDIO.

5. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

6. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

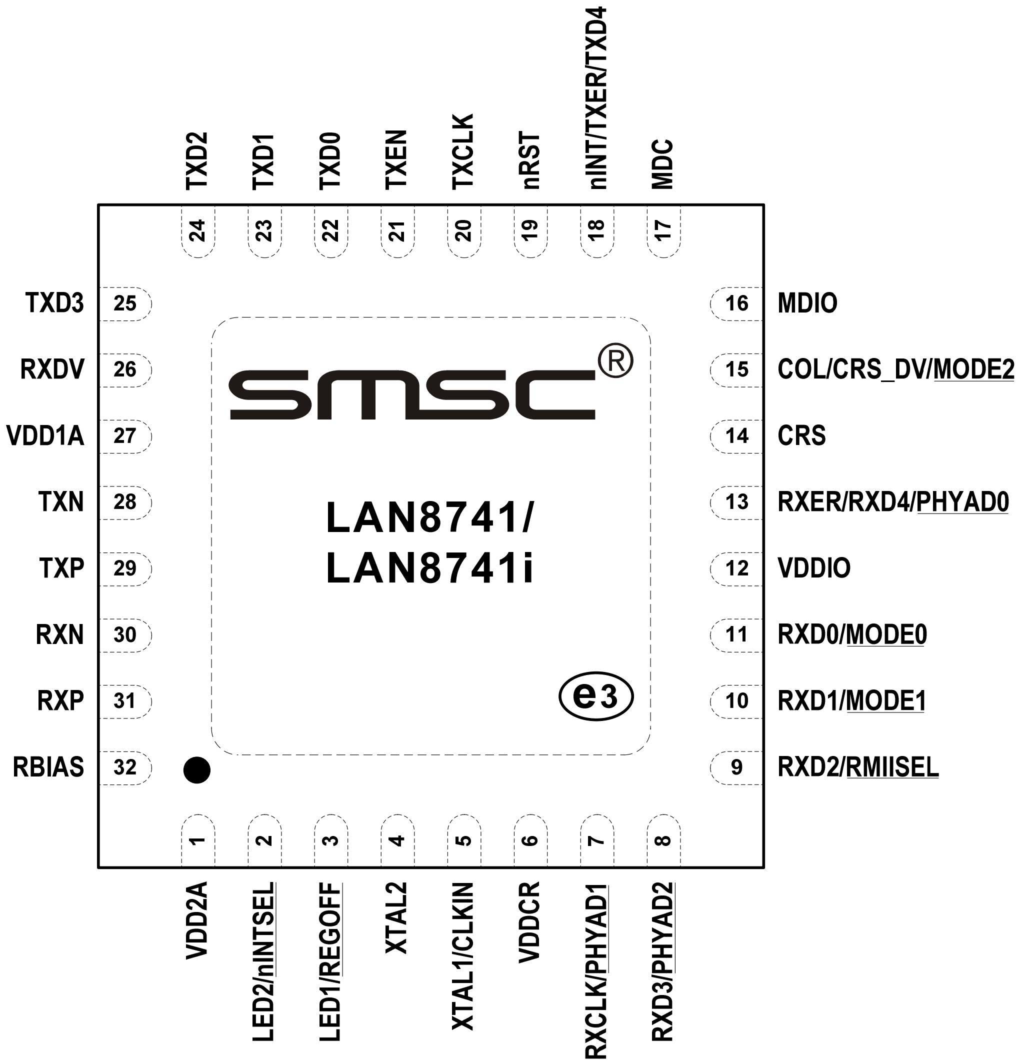
LAN8741 QFN QuickCheck Pinout Table:

Use the following table to check the LAN8741 QFN shape in your schematic.

LAN8741 QFN			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
1	**VDD2A**	17	**MDC**
2	**LED2 / nINTSEL**	18	**nINT / TXER / TXD4**
3	**LED1 / REGOFF**	19	**nRST**
4	**XTAL2**	20	**TXCLK**
5	**XTAL1 / CLKIN**	21	**TXEN**
6	**VDDCR**	22	**TXD0**
7	**RXCLK / PHYAD1**	23	**TXD1**
8	**RXD3 / PHYAD2**	24	**TXD2**
9	**RXD2 / RMIISEL**	25	**TXD3**
10	**RXD1 / MODE1**	26	**RXDV**
11	**RXD0 / MODE0**	27	**VDD1A**
12	**VDDIO**	28	**TXN**
13	**RXER / RXD4 / PHYAD0**	29	**TXP**
14	**CRS**	30	**RXN**
15	**COL / CRS_DV / MODE2**	31	**RXP**
16	**MDIO**	32	**RBIAS**
33		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN8741 QFN Package Drawing:



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Reference Material:

1. SMSC LAN8741 Data Sheet; check web site for latest revision.
2. SMSC LAN8741 CEB Schematic, Assembly No. 6695; check web site for latest revision.
3. SMSC LAN8741 CEB PCB, Assembly No. 6695; order PCB from web site.
4. SMSC LAN8741 CEB PCB Bill of Materials, Assembly No. 6695; check web site for latest revision.
5. CEB stands for Customer Evaluation Board.
6. SMSC LAN8741 Reference Design, check web site for latest revision.
7. SMSC Reference Designs are schematics only; there are no associated PCBs.
8. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smsc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smsc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm