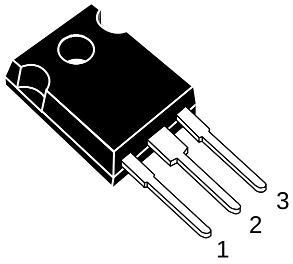
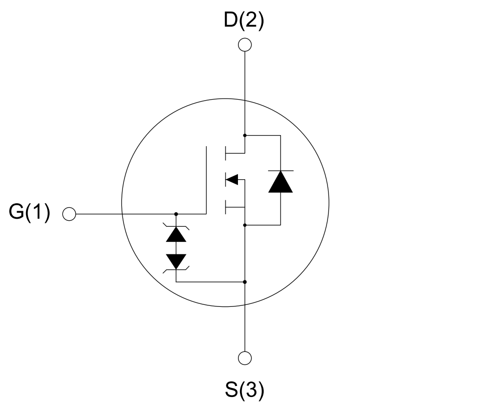
N-channel 850 V, 0.2 Ω typ., 19 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW23N85K5	850 V	0.275 Ω	19 A	250 W

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW23N85K5	23N85K5	TO-247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_{case} = 25 °C	19	A
	Drain current (continuous) at T_{case} = 100 °C	12.4	
I_{DM} [(1)]	Drain current (pulsed)	250	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	250	W
dv/dt [(2)]	Peak diode recovery voltage slope	6	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Operating junction temperature		

Notes:

(1) Pulse width is limited by safe operating area.

(2) I_{SD} ≤ 19 A, di/dt=100 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	45	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} [(1)]	Avalanche current, repetitive or not repetitive	6	A
E_{AS} [(2)]	Single pulse avalanche energy	200	mJ

Notes:

(1) Pulse width limited by T_{jmax}.

(2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	850			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 850 V			10	µA
		V_{GS} = 0 V, V_{DS} = 850 V, T_{case} = 125 °C			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9.5 A		0.2	0.275	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1650	-	pF
C_{oss}	Output capacitance		-	115	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 680 V, V_{GS} = 0 V	-	185	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 60 A, V_{GS} = 10 V (see *Figure 17: "Gate charge test circuit"*)	-	38	-	nC
Q_{gs}	Gate-source charge		-	11	-	
Q_{gd}	Gate-drain charge		-	20	-	

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 9.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 16: "Switching times test circuit for resistive load"* and *Figure 21: "Switching time waveform"*)	-	22	-	ns
t_r	Rise time		-	14	-	
$t_{d(off)}$	Turn-off delay time		-	55	-	
t_f	Fall time		-	8	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}[(1)]	Source-drain current (pulsed)		-		76	A
V_{SD}[(2)]	Forward on voltage	V_{GS} = 0 V, I_{SD} = 19 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	510		ns
Q_{rr}	Reverse recovery charge		-	11		µC
I_{RRM}	Reverse recovery current		-	43		A
t_{rr}	Reverse recovery time	I_{SD} = 19 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 18: "Test circuit for inductive load switching and diode recovery times"*)	-	684		ns
Q_{rr}	Reverse recovery charge		-	14		µC
I_{RRM}	Reverse recovery current		-	41		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

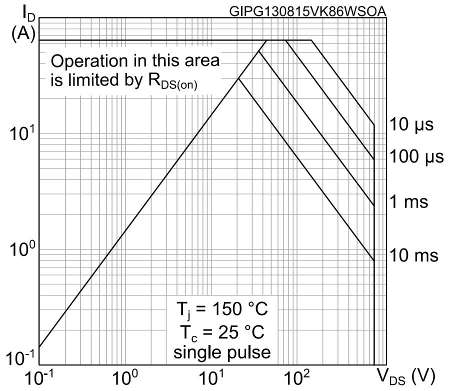


Figure 3: Thermal impedance

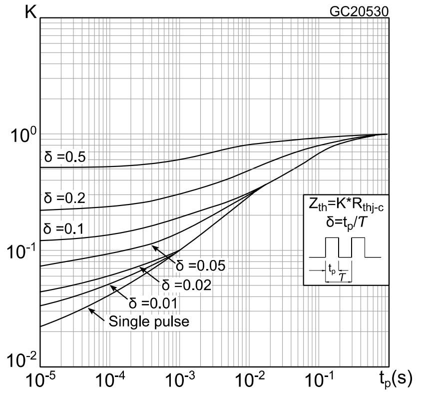


Figure 4: Output characteristics

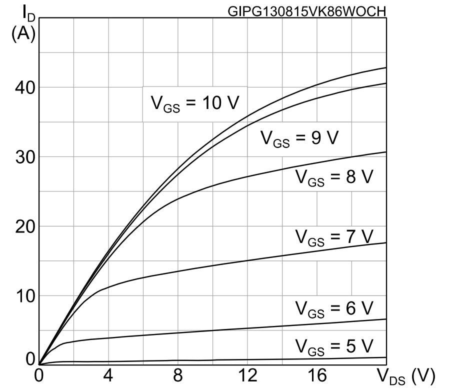


Figure 5: Transfer characteristics

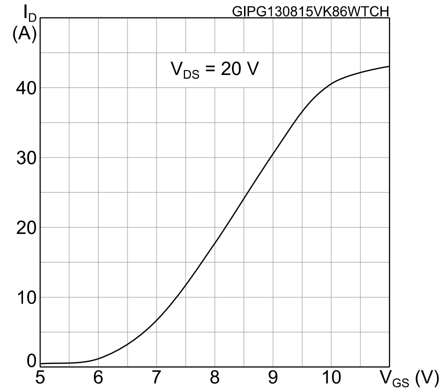


Figure 6: Gate charge vs gate-source voltage

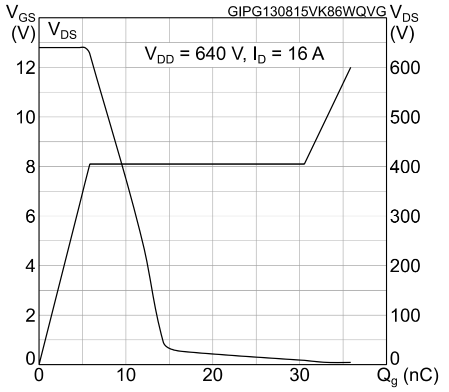
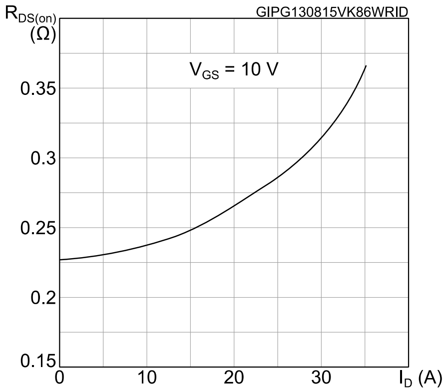


Figure 7: Static drain-source on-resistance



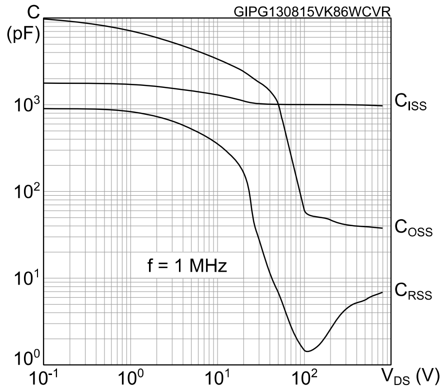


Figure 8: Capacitance variations

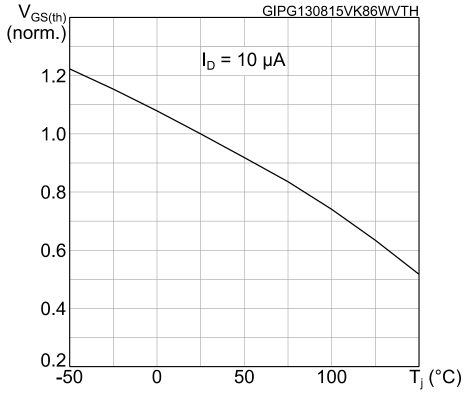


Figure 9: Normalized gate threshold voltage vs temperature

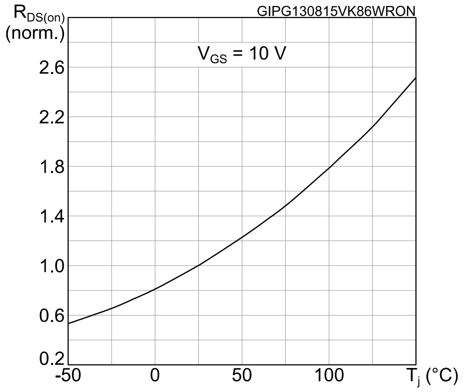


Figure 10: Normalized on-resistance vs temperature

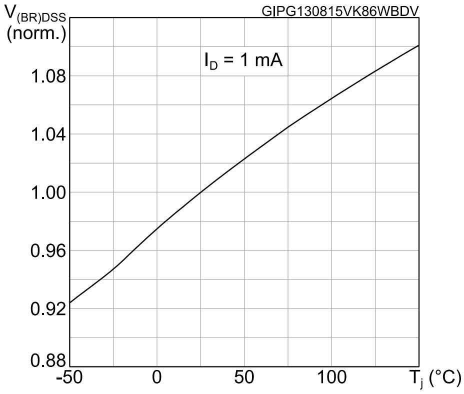


Figure 11: Normalized V(BR)DSS vs temperature

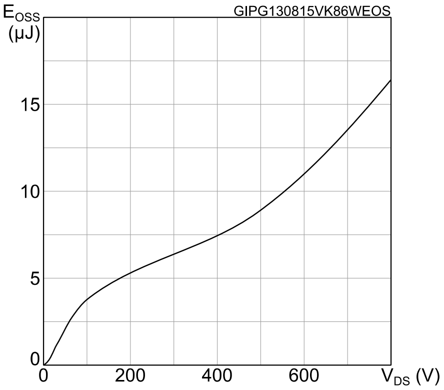


Figure 12: Output capacitance stored energy

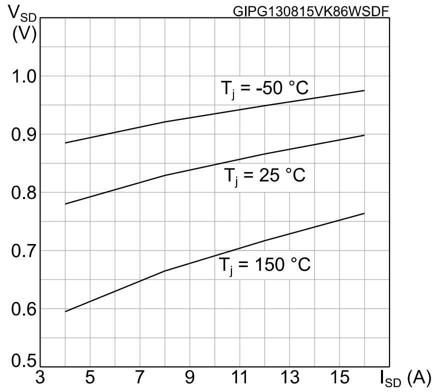


Figure 13: Source- drain diode forward characteristics

Figure 14: Maximum avalanche energy vs temperature (ID = 3.5 A)

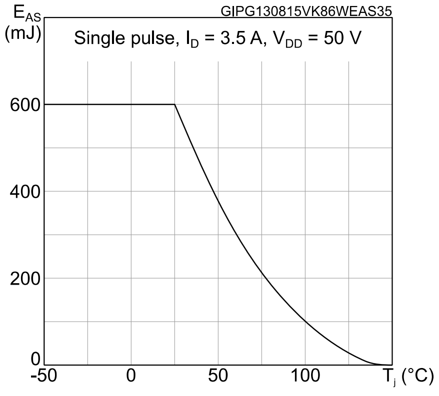
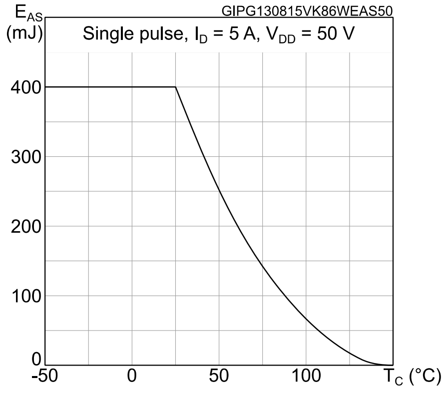


Figure 15: Maximum avalanche energy vs temperature (ID = 5.0 A)



3 Test circuits

Figure 16: Switching times test circuit for resistive load

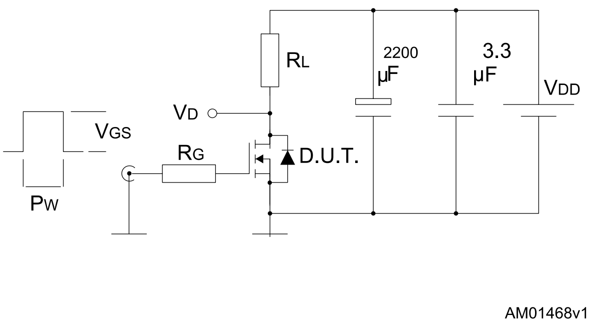


Figure 17: Gate charge test circuit

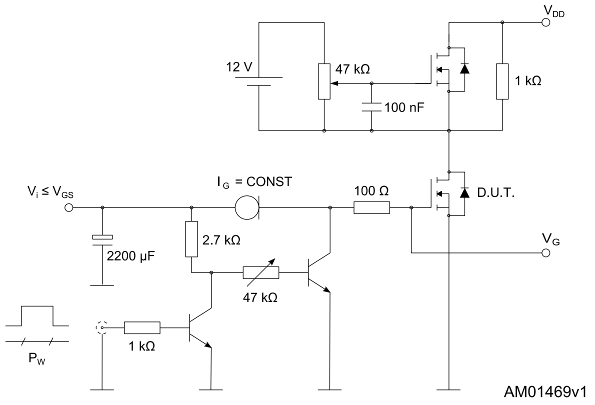


Figure 18: Test circuit for inductive load switching and diode recovery times

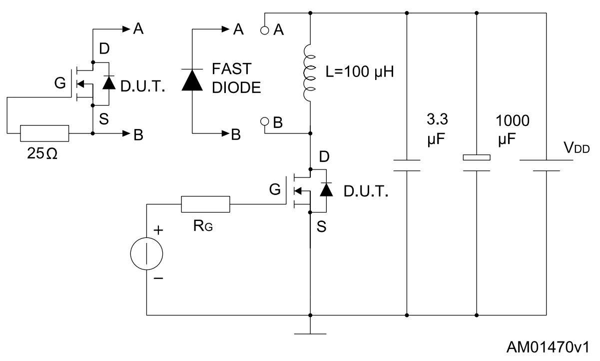


Figure 19: Unclamped inductive load test circuit

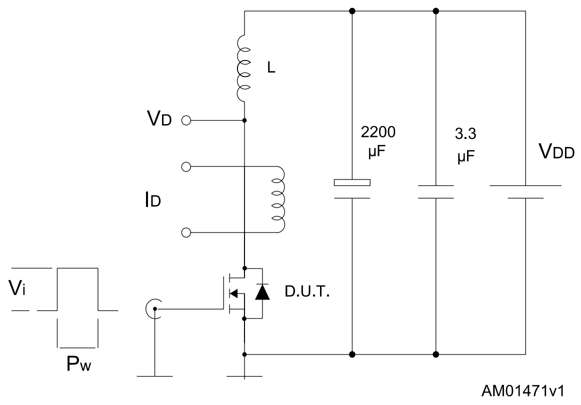


Figure 20: Unclamped inductive waveform

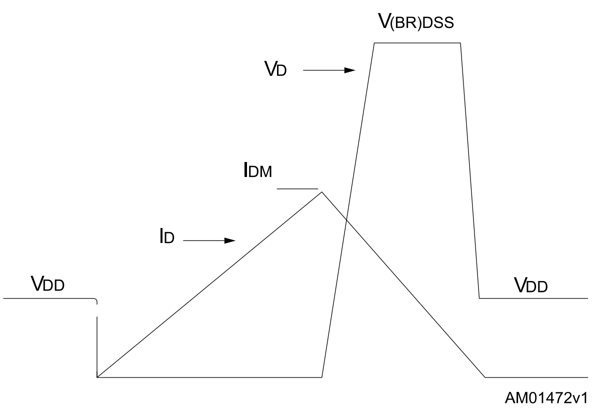
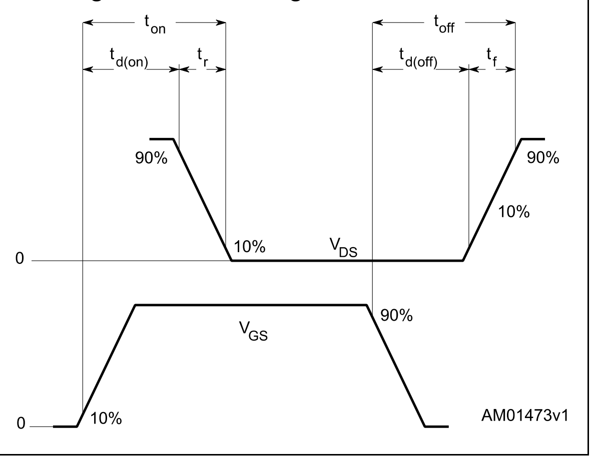


Figure 21: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 22: TO-247 package outline

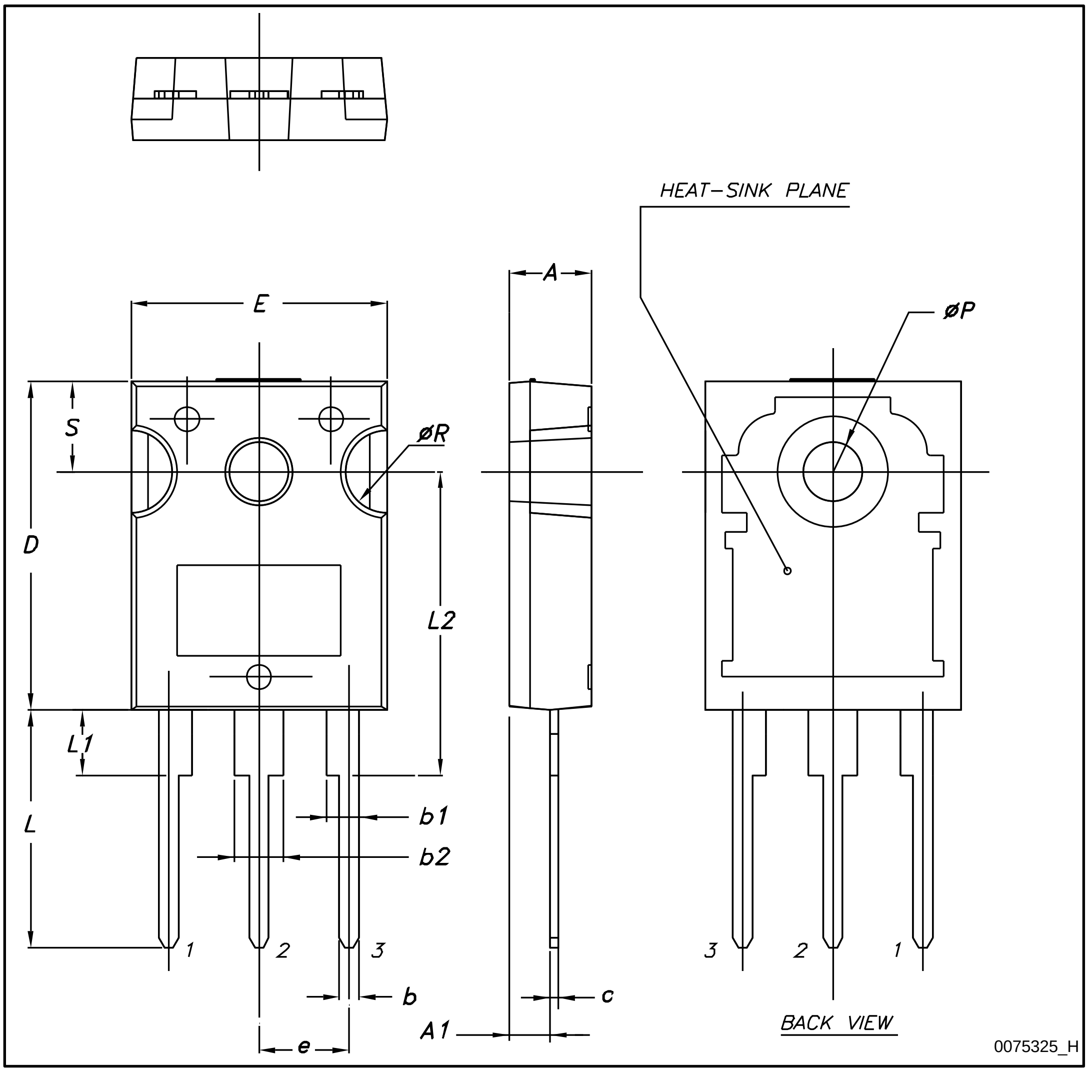


Table 9: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-Aug-2012	1	First release.
21-Jan-2014	2	Document status promoted from preliminary to production data. Added Figure 12: Maximum avalanche energy vs temperature.
13-Aug-2015	3	Text and formatting changes throughout document. On cover page: - updated *Title*, *Features* and *Description* Updated Section *Electrical characteristics* Updated Section *Electrical characteristics (curves)* Updated and renamed Section *Package information* (was Package mechanical data)

IMPORTANT NOTICE – PLEASE READ CAREFULLY