TIDA-00570 Test Results

September 2015

High Speed DLP Sub-system for Industrial 3D Printing and Digital Lithography

About Test Results

The High Speed DLP Sub-system for Industrial 3D Printing and Digital Lithography reference design utilizes Texas Instruments' DLP technology to deliver TI's highest performance combination of speed and resolution.

This design features multiple TI components, highlighted by the DLP9000X chipset, which incorporates the DLP9000X DMD and the DLPC910 controller. These associated devices and reference design were built and tested at TI to validate the design operation up through the 480MHz input data bus width, and that the DLPC910 could support streaming data at that data bus rate.

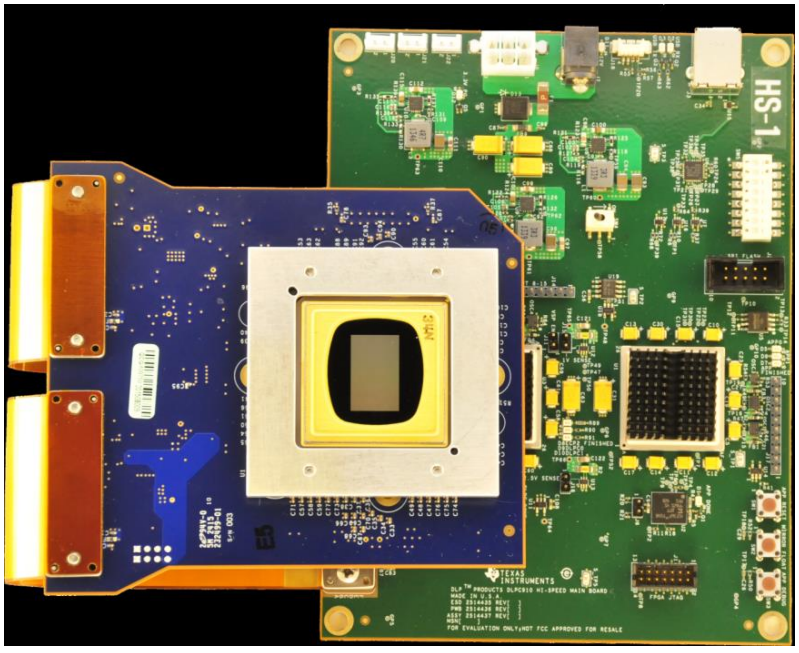

Figure 1 - Reference Design Boards

Related Documentation From Texas Instruments

DLP9000X Data Sheet: *DLP9000 Family of 0.9 WQXGA MVSP Type A DMDs*, TI literature number DLPS036
DLPC910 Data Sheet: *DLPC910 Digital Controller for Advanced Light Control*, TI literature number DLPS064
DLPR910 Data Sheet: *DLPR910 DLP® Configuration PROM*, TI literature number DLPS065

If You Need Assistance

Search for answers on the DLP and MEMS TI E2E Community support forums

1. Reference Design Goals

The goals for this reference design are two-fold: 1) to create a platform with which the DLP9000X-DLPC910 system level validation can be performed, and 2) to provide this reference design to potential customers looking to design their own Industrial 3D Printers and Digital Lithography end equipment for use as a starting point and a reference.

The reference design was created in a schematic capture tool, built, assembled, and tested. The design includes the following DLP components:

- DLPC910 Controller
- DLPR910 Configuration PROM
- DLP9000X High Speed WQXGA DMD

Other components such as power supply ICs were added to complete the reference design as necessary. The design also includes a Xilinx FPGA which is used to simulate an Application Processor that one might find in a Digital Lithography or 3D Print system. This Applications Processor is used to formulate and frame WQXGA resolution, binary (single bit) images to be sent to the inputs of the DLPC910. The DLPC910 subsequently provides this data and relevant control information to the DLP9000X DMD.

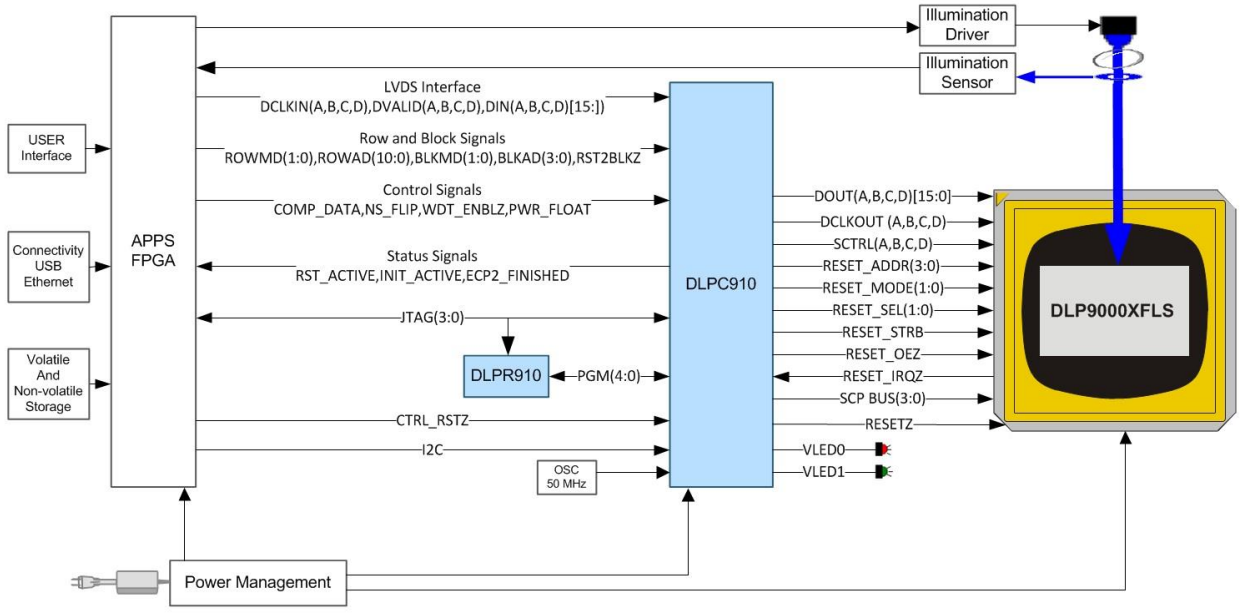

Figure 2 - Reference Design Block Diagram

In the reference design, data streams from the Applications Processor FPGA into the DLPC910 which provides the data to the DLP9000X DMD. The DLPC910 also translates control commands it receives from the Applications Processor into commands which the DMD

understands. The reference design uses test patterns in the Applications Processor to simulate the streaming of data to the DLPC910-DLP9000X as it would occur in a 3-D Printing or Digital Lithography application. In those applications, the Applications Processor FPGA would be replaced with a customer designed Application Processor and the data would relate to the actual exposures of polymers or resists as defined and implemented by the customer.

2. Setup and Hold Measurements

A Tektronix TDS6404 4GHz oscilloscope with P6330 differential probes was used to capture the DLP9000X input LVDS data bus timing. Multiple DMDs were used to make sure there were no measureable differences between devices which could affect input setup and hold timing.

Below is a picture of a DLP9000X input data bit setup time measurement while running the DCLK at 480MHz. The yellow signal is the DCLK from the DLPC910 and the blue signal shows multiple transitions both positive and negative for the Bus D data bit 6 from the DLPC910. Measurements were taken as close to the inputs of the DLP9000X as possible. The measured setup time of 350ps exceeds the datasheet required setup time of 200ps for the DLP9000X DMD.

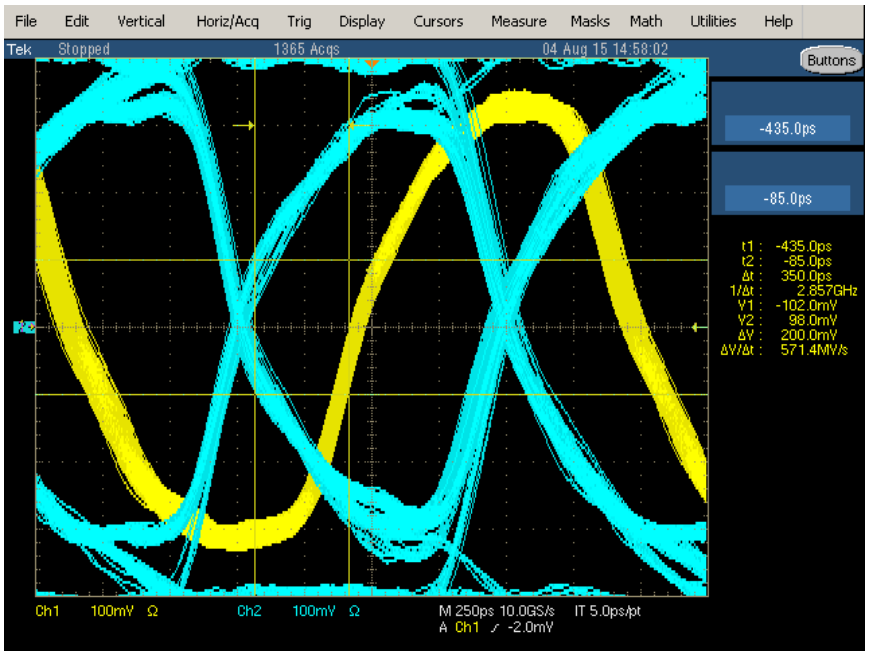

Figure 3 - Measured Setup Time

Below is a picture of a DLP9000X input data bit hold time measurement while running the DCLK at 480MHz. The yellow signal is the DCLK and the blue signal shows multiple transitions both positive and negative for the Input Data Bit 6 of Bus D. The measured hold time of 435ps exceeds the datasheet required hold time of 400ps for the DLP9000X DMD.

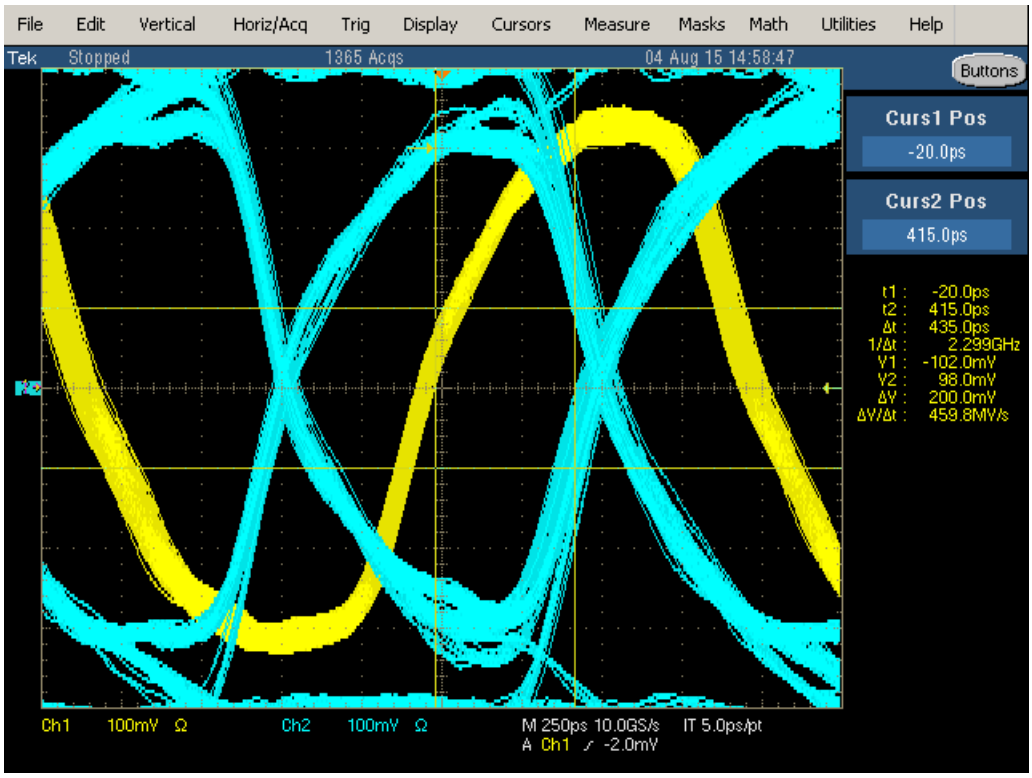

Figure 4 - Measured Hold Time

The data bus signal measurements detailed above were initially taken with a 5” flexible PCB connecting the DLPC910 output data bus signals on the Main Board to the DLP9000X data bus inputs on the DMD board. Follow-on measurements were also taken using 12” flexible PCBs - No measureable differences in signal setup and hold times were perceived using the 12” version.

3. Projection Testing

The DLP9000X DMD PCB of the reference design was mounted up to a modified commercial lamp-based DLP projector such that test patterns internally generated by the applications processor (Xilinx FGPA) could be projected onto a screen for visual validation. Because the DLP9000X WQXGA DMD is of such high resolution, the choice was made to project the images onto a very large wall mounted screen so that the projected patterns could be easily seen and any pattern discrepancies could be identified and debugged.

Several patterns were created within the Applications Processor FPGA. Patterns were created to best allow detection of setup and hold pixel errors or DMD data clocking errors. Figure 5 shows one of these projected patterns.

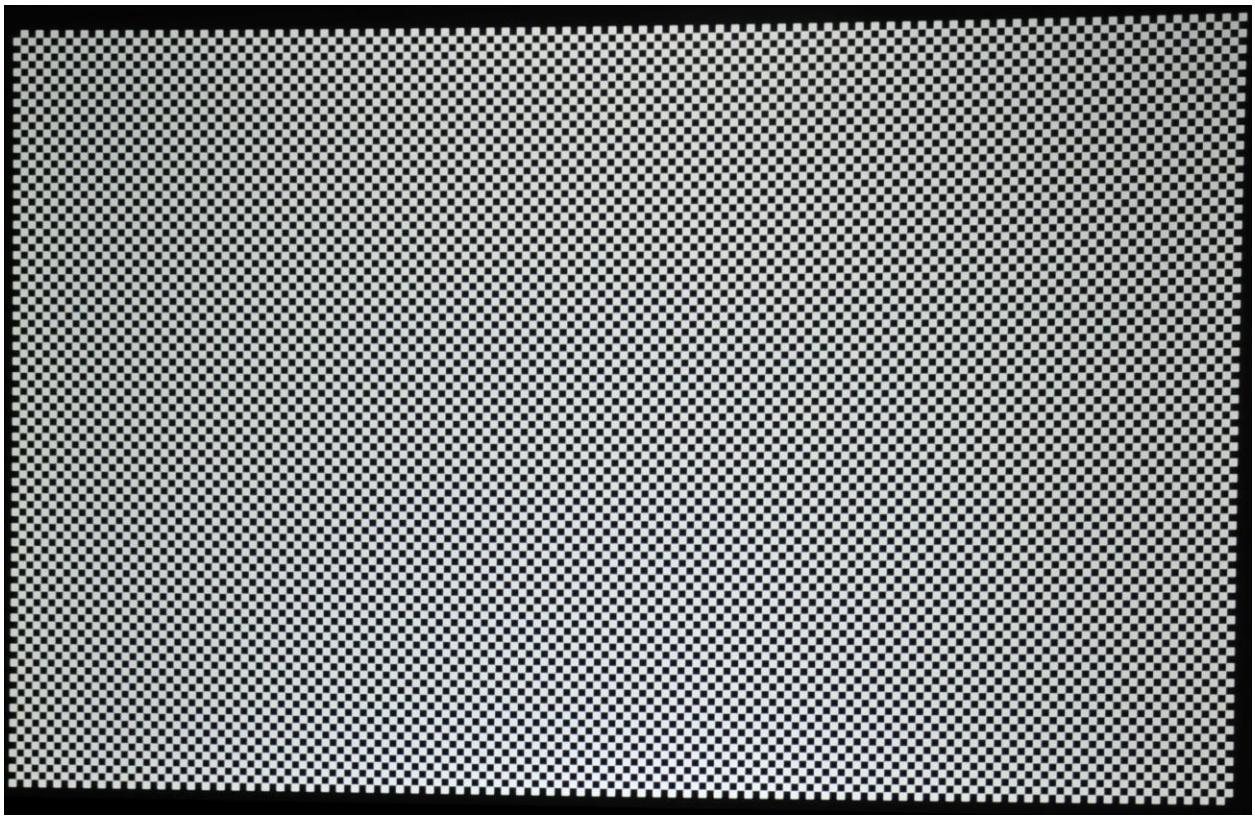

Figure 5 - Displayed Checkerboard Pattern

All patterns were single bit patterns and were sent repeatedly from the Applications Processor to the DLPC910 to the DLP9000X until a new pattern was selected. Testing covered the range of datasheet min and max parameters. DMD VCC and VCCI voltages were varied from minimum to maximum datasheet values without any errors visible in the patterns. Voltages were varied outside the data sheet specifications, thereby indicating sufficient margins for customers operating within the specification limits.

4. Test Summary

Through testing, we have shown that the DLP9000X and DLPC910 chipset has provided good margin for operation in a Digital Lithography or 3D Printing application. Setup and Hold times of the DMD have been met with additional margin for a typical system design. The application of multiple worst case factors during the testing should provide the additional robustness needed in these demanding industrial applications. Our reference design will provide a great starting point and direction for designers of these applications, allowing the designers to focus more on how they would like to use DLP technology instead of how to implement DLP technology.

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