ON Semiconductor®

Final Product/Process Change Notification

Document # : FPCN22170Z
Issue Date: 07 February 2019

Title of Change:	Re-design by metal tune of NCV7425DW0(R2)G and NCV7425DW5(R2)G to correct a design marginality.
Proposed Changed Material First Ship Date:	07 February 2020 *or earlier upon customer approval*
Product Category:	Active components – Integrated circuits
Contact information:	Contact your local ON Semiconductor Sales Office or <jean-jacques.goubet@onsemi.com>
Samples:	Contact your local ON Semiconductor Sales Office to place sample order or <PCN.samples@onsemi.com> Sample requests are to be submitted no later than 45 days after publication of this change notification.
Sample Availability Date:	31 May 2018
PPAP Availability Date:	15 February 2019
Additional Reliability Data:	Contact your local ON Semiconductor Sales Office
Type of Notification:	This is a Final Product/Process Change Notification (FPCN) sent to customers. FPCNs are issued 12 months prior to implementation of the change or earlier upon customer approval. ON Semiconductor will consider this proposed change and it's conditions acceptable, unless an inquiry is made in writing within 45 days of delivery of this notice. To do so, contact PCN.Support@onsemi.com.

Change Category	**Type of Change**
Design	Design Change in Routing

Description and Purpose:

The main change for the two OPN's NCV7425DW0(R2)G and NCV7425DW5(R2)G is a re-design in the digital core (via metal tune only) to correct a design marginality that could lead to a racing condition for some specific LIN and EN signal transitions and timings. This racing condition may lead to a deadlock situation where it is not possible to wake-up the IC anymore. It only occurs in very specific conditions that may not occur in some types of customer applications.

The opportunity of the re-design was used to implement some other quality improvements in order to better comply with more recent internal ON-Semicondutor requirements:

- Implementation of ring bond pads in place of stacked bond pads (improved bonding reliability)
- Replacement of single via's by double via's when this was possible without re-routing (layout for quality improvements)
- Updated metal 3 level spacings around the MIM capacitor to comply with the latest antenna rules (layout for quality improvements)

The layers that are changed are: metal 1, via 1, metal 2, via 2, metal 3, nitride and polyimide layers.

There are no product material changes as a result of this change.

There is no product marking change as a result of this change.

Reason / Motivation for Change:	**- Change benefits for customer:** The re-design version will guarantee that the IC can be waken-up in any conditions thus be functional as expected under all LIN and EN signal transitions and timings circumstances. **- Risk for late release for customer:** Based on previous experience with similar changes and quality improvements implemented at layout level, the risk associated with the changes is negligible. On the opposite, quality will be improved. The efficiency of the re-design to fix the racing condition has been confirmed by evaluation of prototypes mplementing the design change. So the risk that the re-design would not fix the design marginality is ruled-out. Approval at the customer will improve the quality and broaden the functionality of the product under all LIN and EN signals timing conditions. **- Quality improvement:** ring bond pads, double via's and metal 3 layer spacing's updates are implemented and are expected to bring manufacturability and quality improvements.

Anticipated impact on fit, form, function, reliability, product safety or manufacturability	The device has been qualified and validated based on the same Product Specification. The device has successfully passed the qualification tests. Potential impacts can be identified, but due to testing performed by ON Semiconductor in relation to the PCN, associated risks are verified and excluded. No anticipated impacts.	
Sites Affected:	ON Semiconductor Sites: ON Oudenaarde, Belgium	External Foundry/Subcon Sites: None
Marking of Parts/ Traceability of Change:	The new re-designed versions will **replace** the current variants. The same OPN's will be used. The affected parts will be identified with date codes that ensure product traceability.	

Reliability Data Summary:

QV DEVICE NAME : 0C618 and 0C619
(NCV7425DW0{R2}G and NCV7425DW5{R2}G)
PACKAGE: SOIC-16-EP

The following qualification have been performed on the re-designed version :

Test	Specification	Condition	Interval	Results
ESD	AEC-Q100-011 (CDM) Mil-Std-883C-Meth-3015.7 (HBM)	Per standard	N/A	0 failure ; 3 samples per voltage level (CDM) 0 failure ; 3 samples per voltage level (HBM)
LU	JEDEC standard EIA/JESD78	Per standard	N/A	0 failure / 6 samples
Electrical distributions	AEC-Q100-009	• Electrical tests at 3 temperatures: 130degC, 25 degC and -40 degC • Sample size: >200 samples from C618 + >200 samples from C619.	N/A	No impact of re-design on Cpk's

Electrical Characteristic Summary:

The electrical characteristics are not impacted by the changes detailed in this FPCN.

List of Affected Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.

Current Part Number	New Part Number	Qualification Vehicle
NCV7425DW0G	NA	NCV7425DW0G
NCV7425DW0R2G	NA	NCV7425DW0R2G
NCV7425DW5G	NA	NCV7425DW5G
NCV7425DW5R2G	NA	NCV7425DW5R2G

Appendix A: Changed Products

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Product	Customer Part Number	New Part Number	Qualification Vehicle
NCV7425DW0R2G		NA	NCV7425DW0R2G
NCV7425DW5R2G		NA	NCV7425DW5R2G