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REFERENCE DESIGN 1117 INCLUDES: ✓Tested Circuit ✓Schematic ✓Description ✓Test Data

# Small Photodiode Receiver Handles Fiber-Optic Data Rates to 800kbps

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*Abstract: Combining a photodiode with two op amps and a comparator forms a fiber-optic receiver capable of data rates to 800kbps while occupying little board space.*

Combining a photodiode with two op amps and a comparator (**Figure 1**) forms a fiber-optic receiver capable of data rates to 800kbps. Small packages (5-pin SOT23 for the op amps, 8-pin  $\mu$ MAX® for the comparator) minimize the required real estate on a PC board or hybrid substrate.

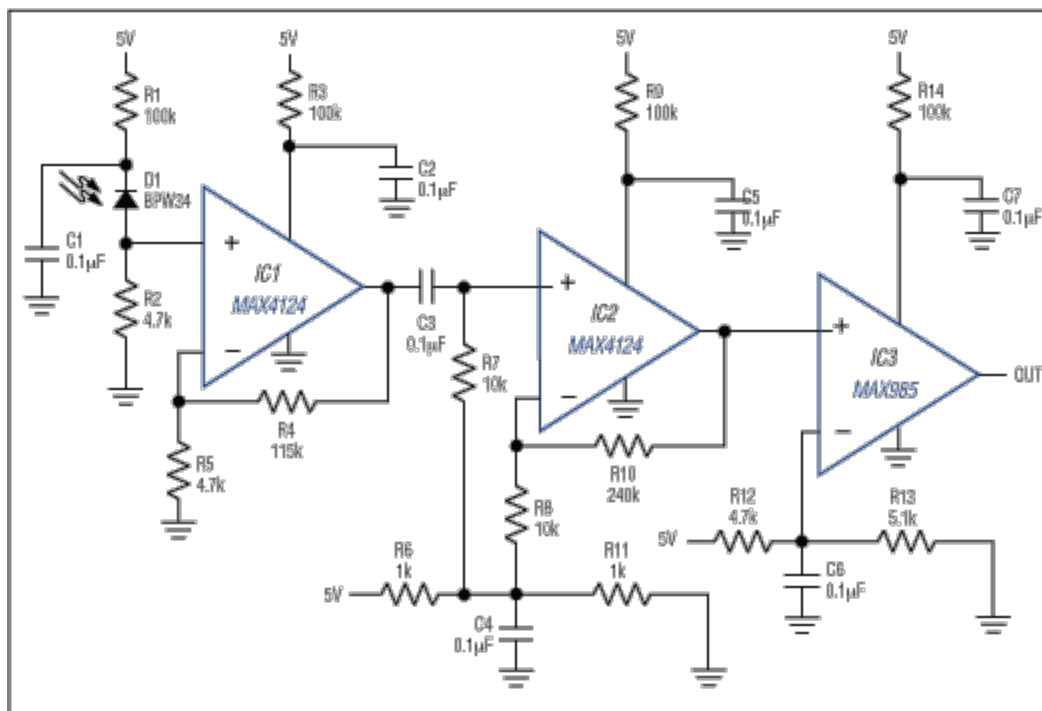


Figure 1. These two op amps and this comparator form a tiny photodiode receiver for data rates to 800kbps.

The photodiode operates in the photoconductive mode, producing a signal voltage at IC1 whose transimpedance gain is equal to the value of R2 (4700 $\Omega$ , in this case). The op amps (IC1 and IC2) are configured as noninverting amplifiers with gains of approximately 25V/V each; therefore, the circuit's overall transimpedance gain is just under 3M $\Omega$ : 4700 $\Omega$   $\times$  25  $\times$  25 = 2.99M $\Omega$ . The op amps' gain-

bandwidth capability sets the maximum practical data rate at 800kbps.

Capacitive coupling between IC1 and IC2 negates the amplification of IC1's offset voltage. To achieve an optimum signal amplitude and symmetry, the R6/R11 divider sets IC2's reference voltage at 2.5V. The R12/R13 divider, which sets the comparator's reference somewhat higher (2.6V), provides a noise margin for the system and ensures that the comparator output remains low during a "no-signal" condition.

Capacitive coupling cannot maintain a DC signal; instead, it allows DC portions of the signal to "relax" toward the reference level, as shown in **Figure 2**. This effect, particularly noticeable for signals that appear after a long quiet period, is directly affected by the R7C3 time constant. R7C3 should be as large as possible to minimize the relaxation effect, but R7 should remain approximately 10kΩ (to minimize offset voltage by matching the inverting-input source resistance). The comparator cannot switch when its input is below the reference level, so too much relaxation can cause a loss of data at the end of a long string of 1s or 0s (**Figure 3**).

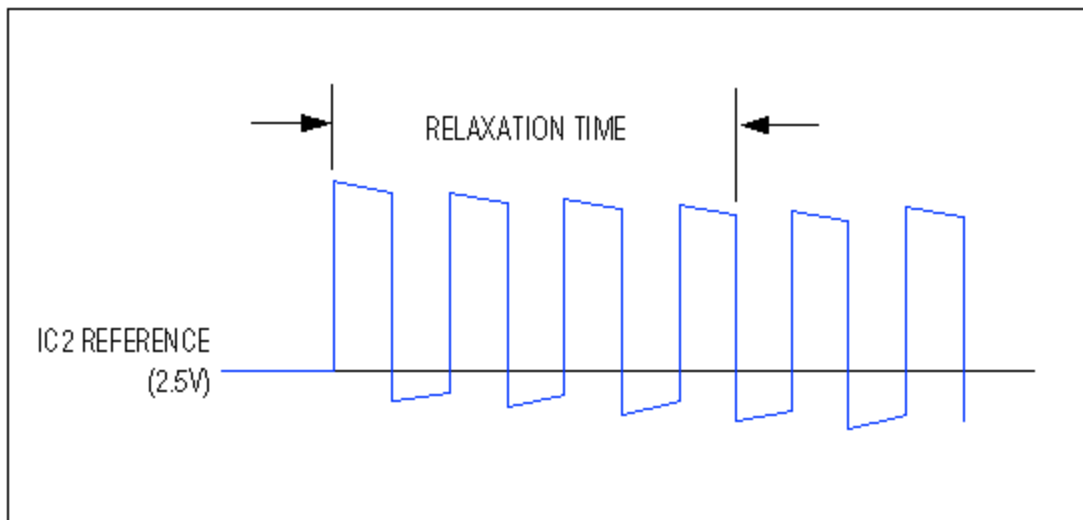


Figure 2. Figure 1's coupling capacitor (C3) causes a "signal relaxation" in the waveform at IC2's output and noninverting input.

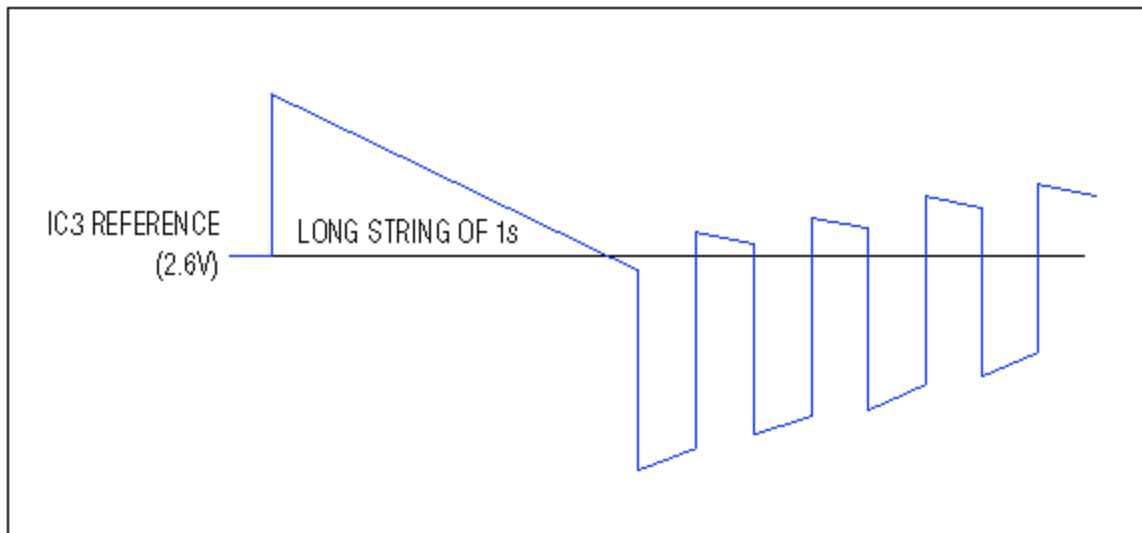


Figure 3. This waveform (from Figure 1's IC2 output) shows that signal relaxation can cause data loss. (The comparator output goes low when the waveform crosses its reference level.)

Again, the IC3 reference should be slightly higher than the IC2 reference for a logic-low no-signal output (otherwise, set the IC3 reference lower). This  $\Delta V_{REF}$  provides a system noise margin that can be adjusted via the R12/R13 divider, but be aware of the trade-off:  $\Delta V_{REF}$  going too low allows erroneous output transitions and going too high degrades timing of the received signal. Set  $\Delta V_{REF}$  as low as possible without causing erroneous transitions, making an allowance for the offset voltages in IC2 and IC3.

The system is designed for 5V operation, but with a minor degradation in data rate it can operate at 3.3V or even 3V. Reducing the supply voltage increases the photodiode's internal capacitance (inversely proportional to the applied bias voltage), which forms a lowpass pole with R2 that limits the photodiode's frequency response. To a lesser degree, the lower supply voltage also limits response by producing a smaller gain-bandwidth product in the amplifiers. The circuitry is designed to accommodate a change in supply voltage with only one adjustment:  $\Delta V_{REF}$  changes with supply voltage, so the R12/R13 divider must be adjusted as required to re-establish the desired noise margin.

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REFERENCE DESIGN 1117, AN1117, AN 1117, APP1117, Appnote1117, Appnote 1117

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