NXP Semiconductors
Technical Data

Document Number: A2T21S260W12N
Rev. 0, 1/2017

RoHS

RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 56 W RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2200 MHz.

2100 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, P_{out} = 56 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

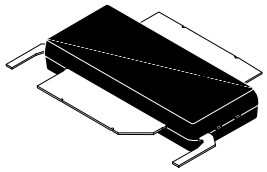
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	17.0	30.0	6.9	–35.2	–11
2140 MHz	17.6	30.8	6.9	–34.2	–16
2170 MHz	17.9	31.8	6.8	–33.5	–25
2200 MHz	18.2	32.9	6.6	–32.9	–15

Features

- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Optimized for Doherty applications

A2T21S260W12NR3

2110–2200 MHz, 56 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



OM–880X–2L2L
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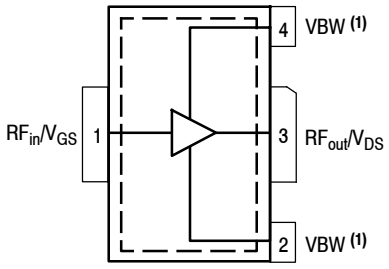


(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. Device can operate with V_{DD} current supplied through pin 2 and pin 4.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 56 W Avg., W-CDMA, 28 Vdc, I_{DQ} = 1600 mA, 2155 MHz	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 320 μAdc)	$V_{GS(th)}$	1.2	1.7	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1600 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.2 Adc)	$V_{DS(on)}$	0.1	0.17	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

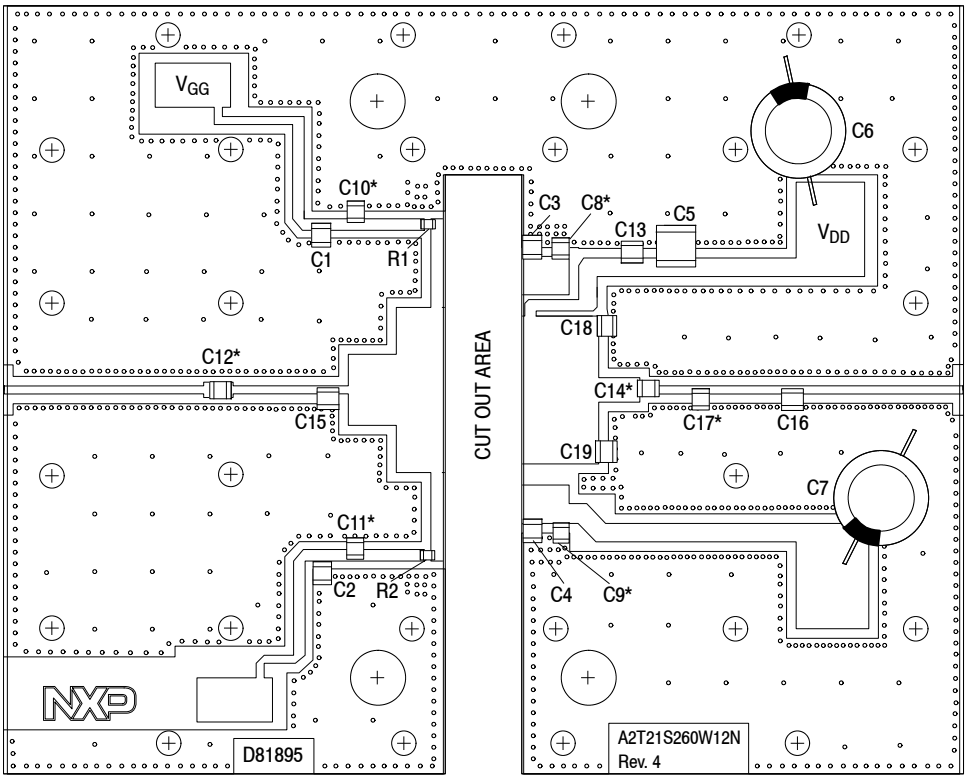
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, P_{out} = 56 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	16.5	17.9	19.0	dB
Drain Efficiency	η_D	29.0	31.8	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.4	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	–33.5	–31.0	dBc
Input Return Loss	IRL	—	–25	–8	dB
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQ} = 1600 mA, f = 2140 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 390 W Pulsed CW Output Power (3 dB Input Overdrive from 320 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1600 mA, 2110–2200 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, Pulsed CW	P1dB	—	218	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2200 MHz frequency range.)	Φ	—	–16	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 90 MHz Bandwidth @ P_{out} = 56 W Avg.	G_F	—	1.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T21S260W12NR3	R3 Suffix = 250 Units, 56 mm Tape Width, 13-inch Reel	OM-880X-2L2L

1. Part internally matched both on input and output.



*C8, C9, C10, C11, C12, C14 and C17 are mounted vertically.

Figure 2. A2T21S260W12NR3 Test Circuit Component Layout

Table 7. A2T21S260W12NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	2.2 μF Chip Capacitor	C3227X7R2A225M	TDK
C3, C4	4.7 μF Chip Capacitor	C4532X7S2A475M230KB	TDK
C5	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C6, C7	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C8, C9, C10, C11, C12	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C13, C14	12 pF Chip Capacitor	ATC800B120JT500XT	ATC
C15	0.2 pF Chip Capacitor	ATC100B0R24BT500XT	ATC
C16	0.4 pF Chip Capacitor	ATC800B0R4BT500XT	ATC
C17, C18, C19	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2	2.2 Ω, 1/8 W Chip Resistor	CRCW08052R20JNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D81895	MTL

TYPICAL CHARACTERISTICS — 2110–2200 MHz

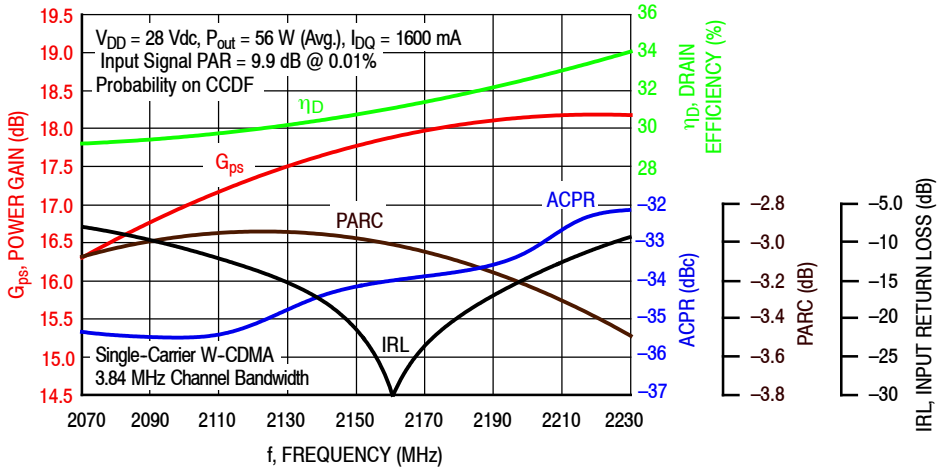


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 56 Watts Avg.

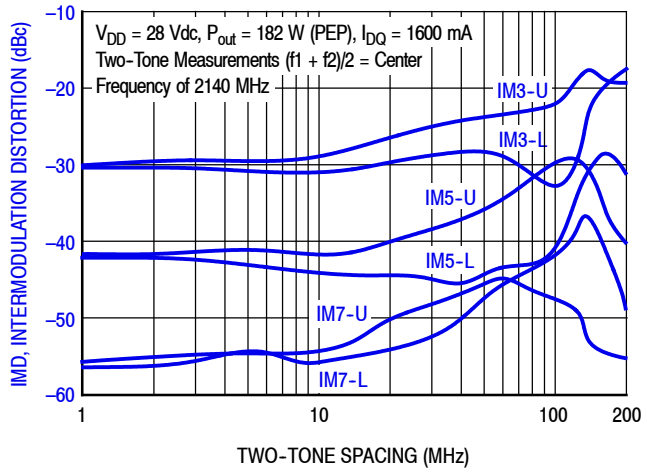


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

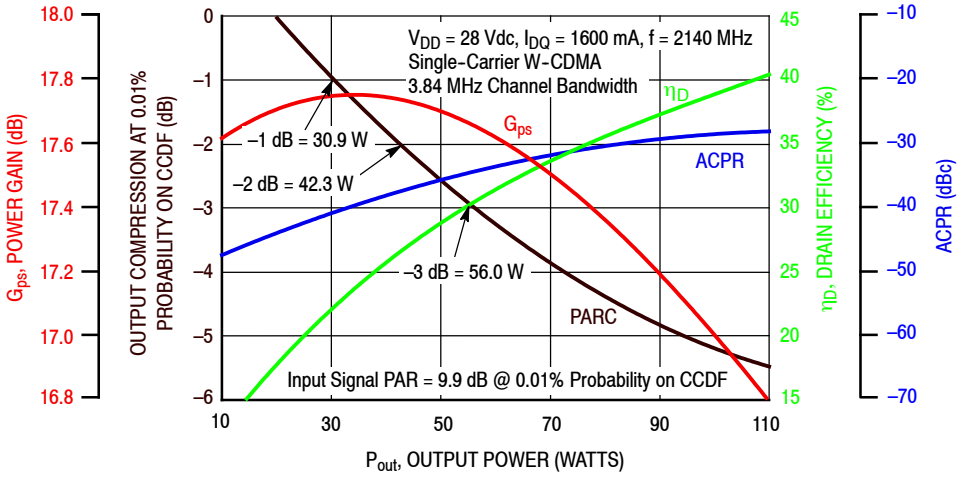


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2200 MHz

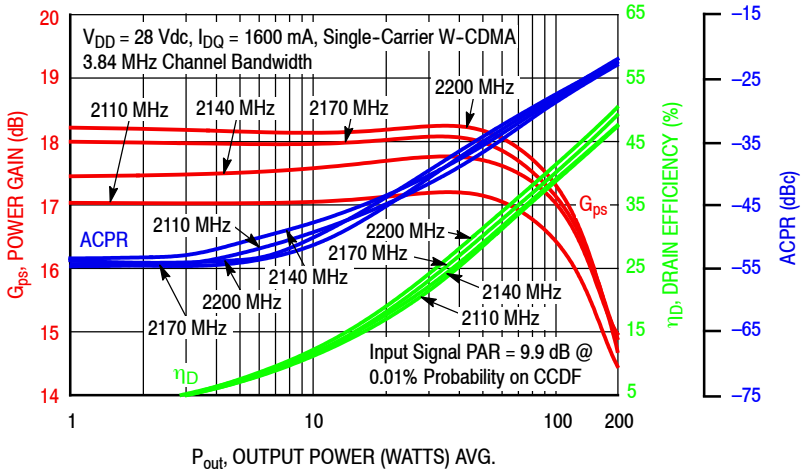


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

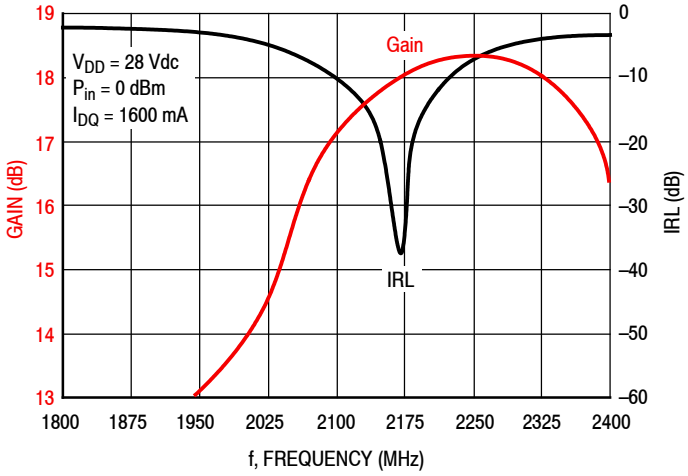


Figure 7. Broadband Frequency Response

Table 8. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1607 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.82 – j4.10	0.86 + j3.79	0.62 – j3.93	16.5	54.9	311	54.3	–11
2140	0.95 – j4.36	1.04 + j3.98	0.63 – j4.00	16.8	54.9	311	54.8	–11
2170	1.08 – j4.63	1.19 + j4.22	0.62 – j4.03	16.6	54.8	302	52.8	–12
2200	1.32 – j5.00	1.40 + j4.48	0.57 – j3.99	16.7	54.7	294	51.3	–12

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.82 – j4.10	0.82 + j3.91	0.63 – j4.03	14.3	55.7	368	54.9	–15
2140	0.95 – j4.36	0.99 + j4.13	0.62 – j4.06	14.6	55.6	366	55.1	–16
2170	1.08 – j4.63	1.15 + j4.39	0.62 – j4.09	14.4	55.5	356	53.5	–16
2200	1.32 – j5.00	1.41 + j4.68	0.59 – j4.19	14.1	55.4	343	50.1	–16

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1607 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.82 – j4.10	0.81 + j3.85	1.07 – j3.18	19.4	52.9	196	66.0	–19
2140	0.95 – j4.36	0.97 + j4.04	1.01 – j3.30	19.4	53.2	207	66.1	–19
2170	1.08 – j4.63	1.14 + j4.30	0.94 – j3.32	19.2	53.0	199	63.6	–19
2200	1.32 – j5.00	1.35 + j4.54	0.89 – j3.29	19.5	52.6	183	62.6	–20

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	0.82 – j4.10	0.75 + j3.93	1.00 – j3.27	17.1	53.8	242	66.2	–25
2140	0.95 – j4.36	0.91 + j4.16	0.99 – j3.30	17.4	53.7	237	65.9	–26
2170	1.08 – j4.63	1.09 + j4.43	0.93 – j3.35	17.1	53.7	233	63.1	–26
2200	1.32 – j5.00	1.33 + j4.70	0.90 – j3.44	17.2	53.7	237	62.2	–25

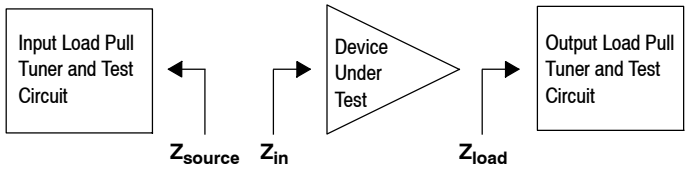
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

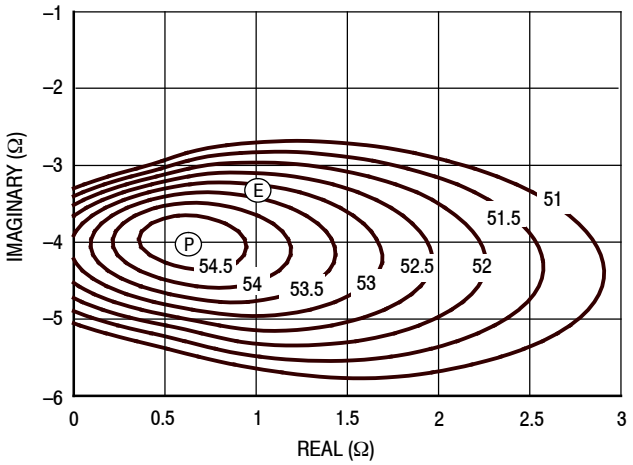


Figure 8. P1dB Load Pull Output Power Contours (dBm)

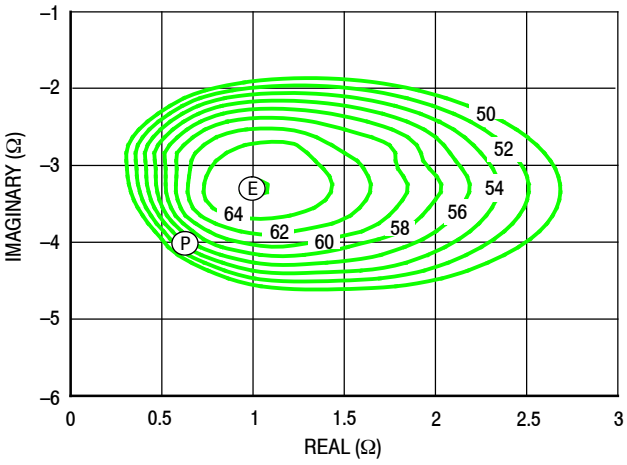


Figure 9. P1dB Load Pull Efficiency Contours (%)

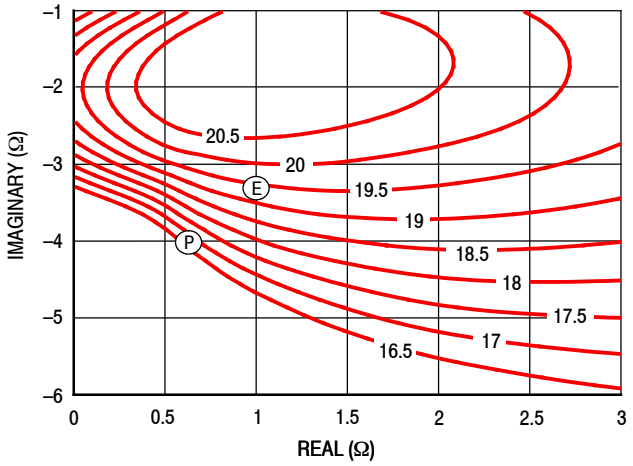


Figure 10. P1dB Load Pull Gain Contours (dB)

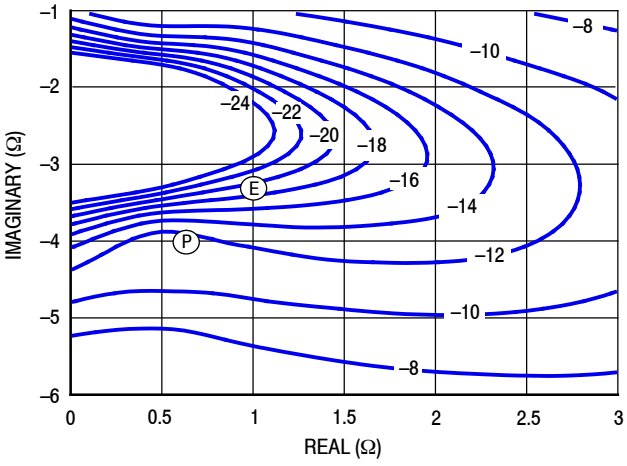


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 2140 MHz

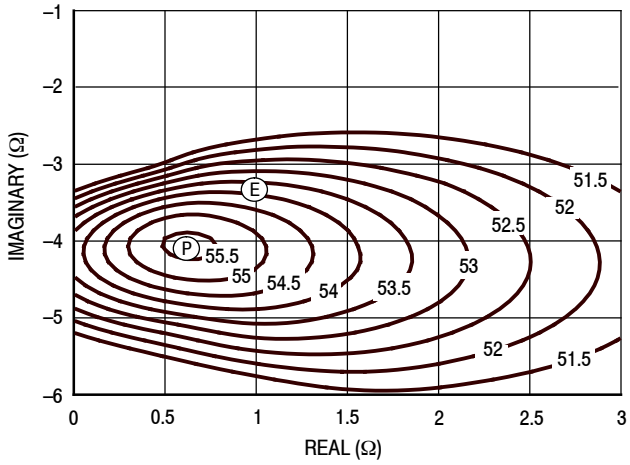


Figure 12. P3dB Load Pull Output Power Contours (dBm)

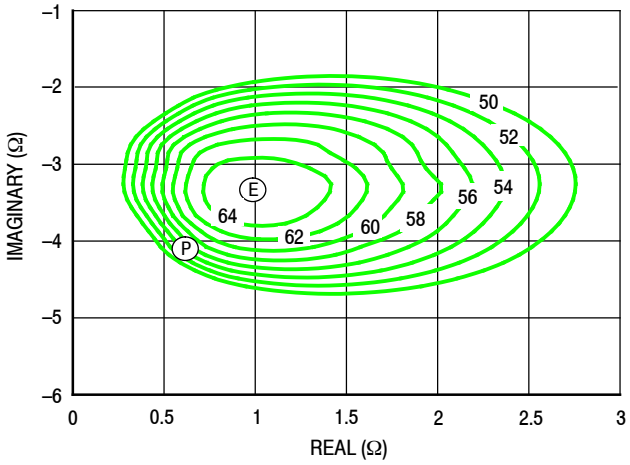


Figure 13. P3dB Load Pull Efficiency Contours (%)

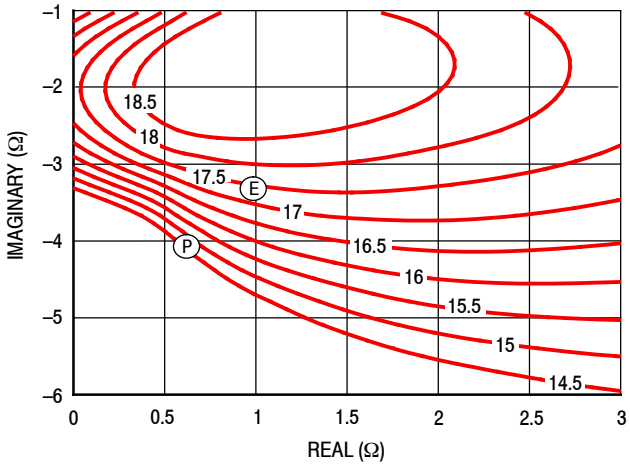


Figure 14. P3dB Load Pull Gain Contours (dB)

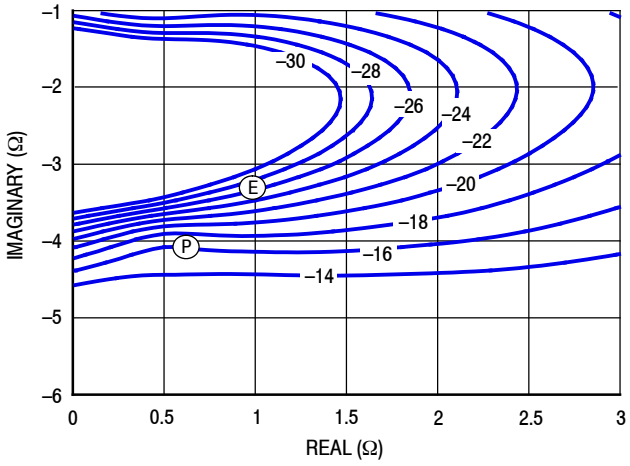
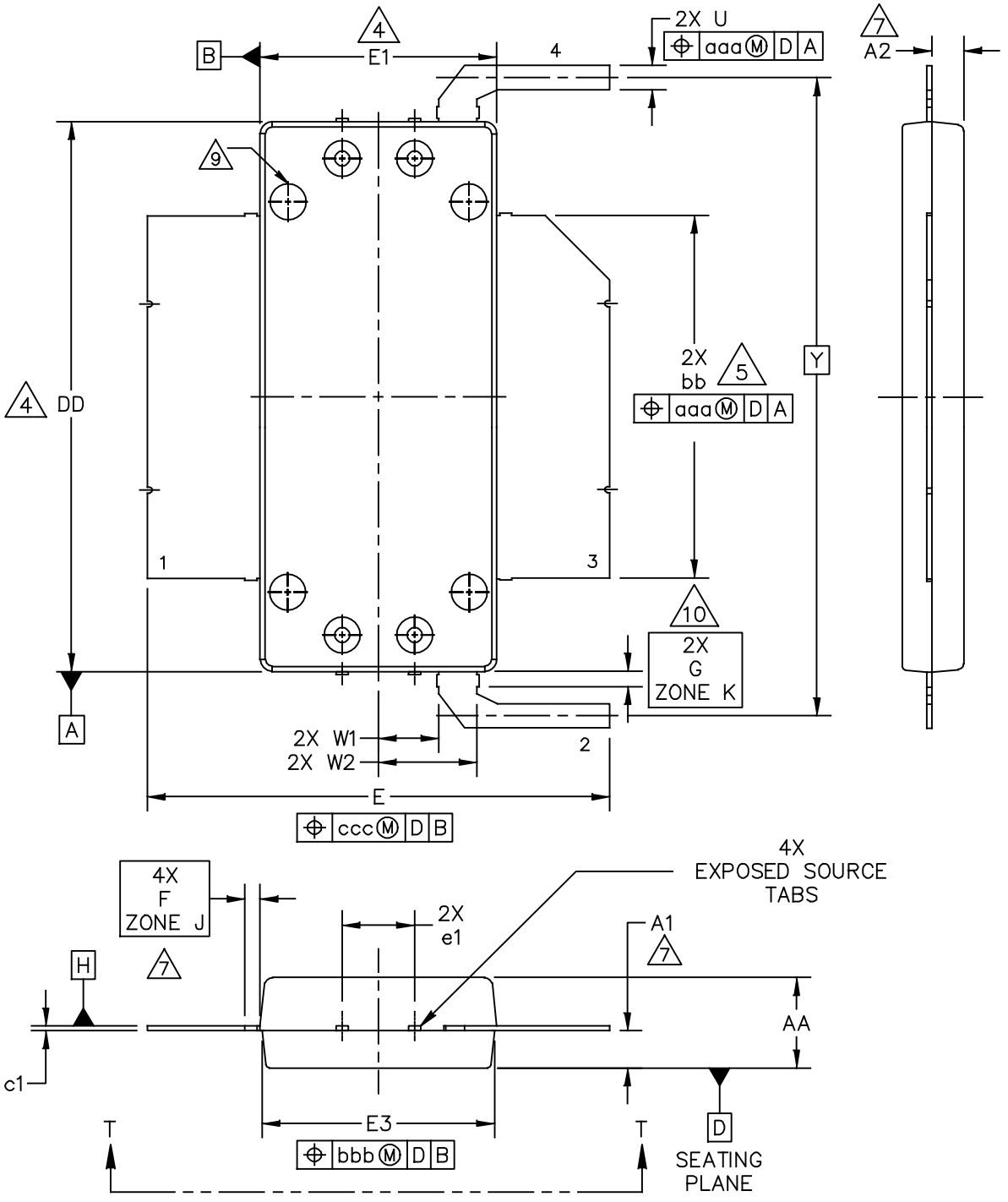


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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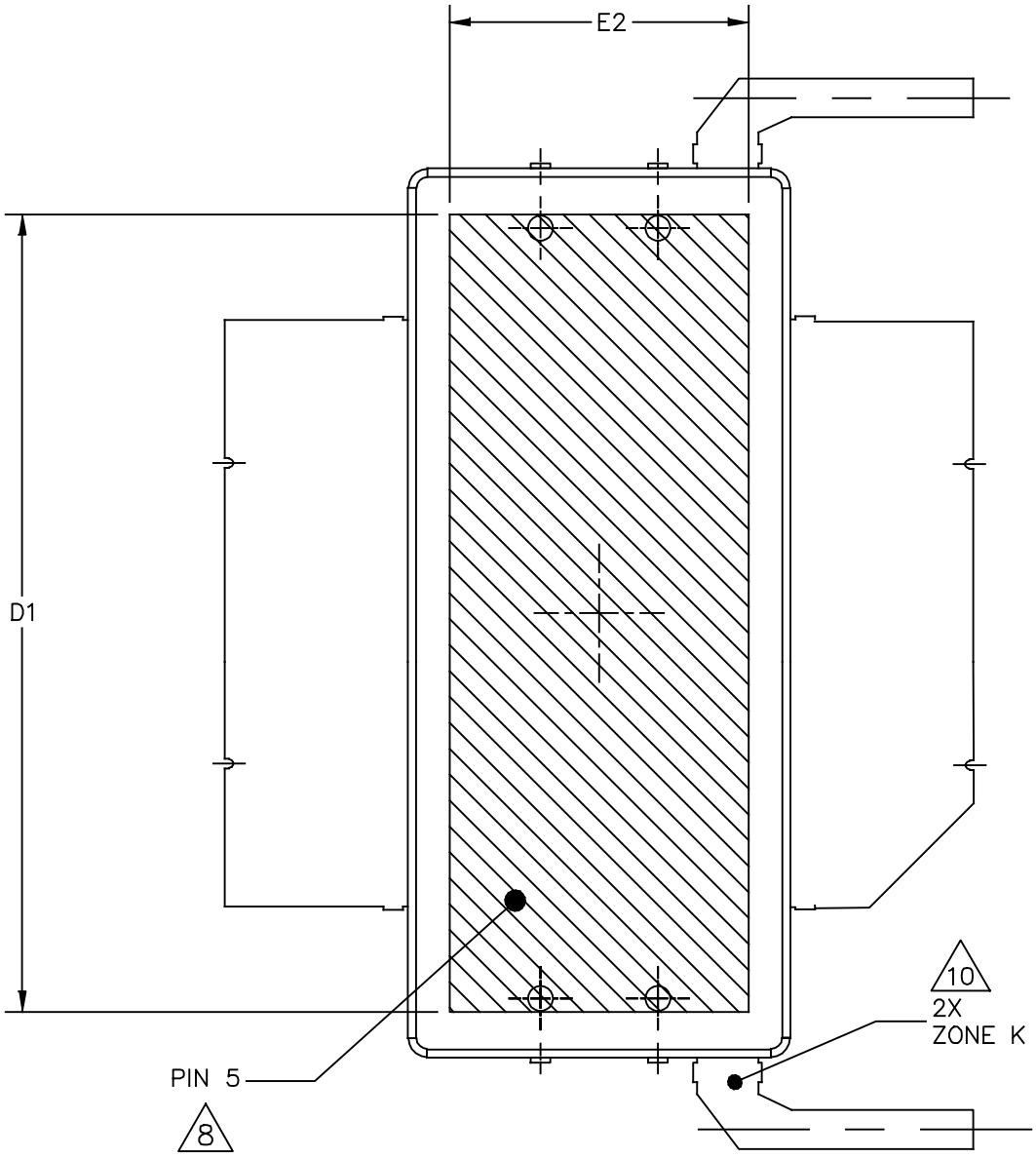

BOTTOM VIEW
VIEW T–T

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	STANDARD: NON–JEDEC	
	SOT1817–1	09 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS A1 AND A2 APPLIES WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1 AND 3. A2 APPLIES TO PINS 2 AND 4.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

9. DIMPLED HOLE REPRESENTS INPUT SIDE.

10. ZONE K REPRESENTS NON-SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.148	.152	3.76	3.86	W1	.095	.105	2.41	2.67
A1	.059	.065	1.50	1.65	W2	.158	.168	4.01	4.27
A2	.056	.068	1.42	1.73	U	.037	.043	0.94	1.09
DD	.908	.912	23.06	23.16	Y	1.056 BSC		26.82 BSC	
D1	.816	----	20.73	----	bb	.597	.603	15.16	15.32
E	.762	.770	19.35	19.56	c1	.007	.011	0.18	0.28
E1	.390	.394	9.91	10.01	e1	.116	.124	2.95	3.15
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83	aaa	.004		0.10	
F	.025 BSC		0.64 BSC		bbb	.006		0.15	
G	.030 BSC		0.76 BSC		ccc	.010		0.25	

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TITLE: OM-880X-2L2L

DOCUMENT NO: 98ASA00549D REV: A

STANDARD: NON-JEDEC

SOT1817-1 09 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Over-Molded Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2017	• Initial release of data sheet

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Document Number: A2T21S260W12N
Rev. 0, 1/2017