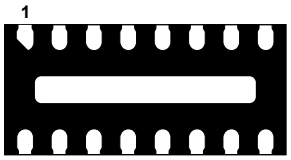
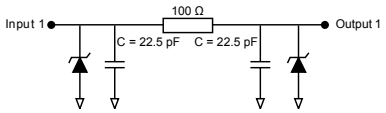
EMIF08-1005M16

Datasheet

8-line IPAD™ low capacitance EMI filter and ESD protection in QFN package



QFN 16L 3.3 mm x 1.5 mm
(bottom view)



Typical line capacitance = 45 pF typ.@ 0 V

Product status
EMIF08-1005M16

Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering:
  - Greater than -34 dB attenuation at frequencies from 900 MHz to 1.8 GHz
- Cut-off frequency: 100 MHz
- Very low PCB space consuming: 3.3 mm x 1.5 mm
- Very thin package: 0.6 mm max.
- High reliability offered by monolithic integration
- RoHS package
- Complies with following standards:
  - IEC 61000-4-2 level 4 input and output pins
    15 kV (air discharge)
    8 kV (contact discharge)
  - MIL STD 883G - Method 3015-7 Class 3B (all pins)
- UL94 V0

Applications

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU boards

Description

The EMIF08-1005M16 is an 8-line, highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the input or output pins.

1 Characteristics

Figure 1. Pin configuration

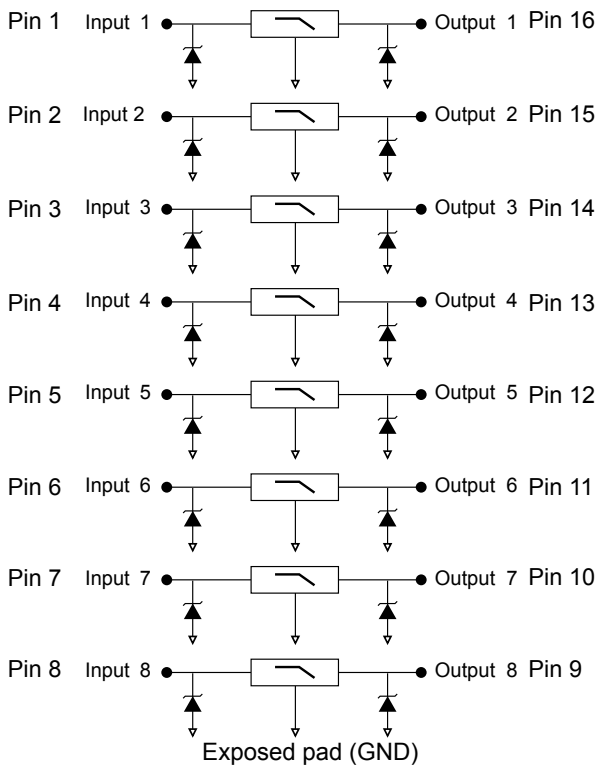


Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC 61000-4-2, air discharge ESD IEC 61000-4-2 contact discharge	15 15	kV
T_j	Maximum junction temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Figure 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current at VRM
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Input capacitance per line

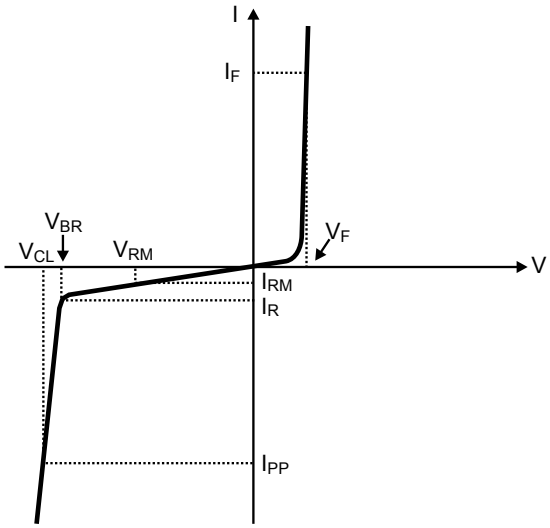


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	v
V_F	I_F = 10 mA	0.5	1.0	1.5	v
I_{RM}	V_{RM} = 3 V per line			200	nA
$R_{I/O}$	Tolerance ± 10%	90	100	110	Ω
C_{line}	V_{LINE} = 0 V dc, V_{OSC} = 30 mV, F = 1 MHz	38	45	52	pF

1.1 Characteristics (curves)

Figure 3. S21 attenuation measurement

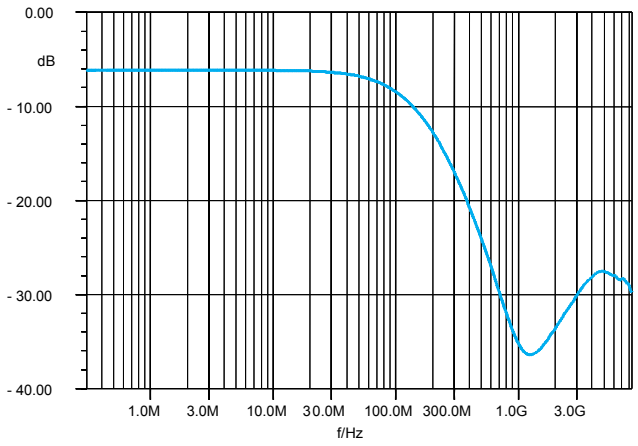


Figure 4. Analog cross talk measurements

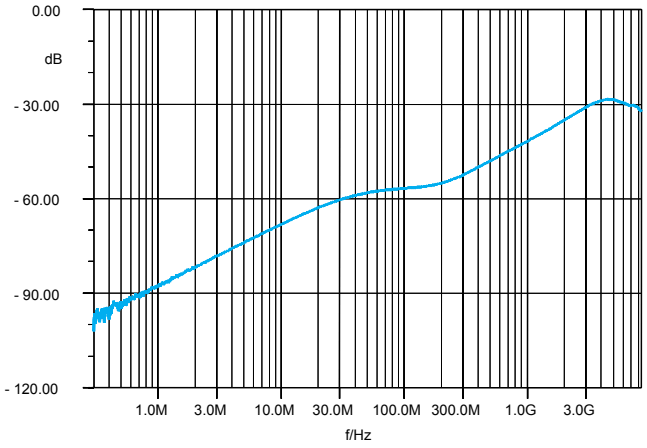


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

Figure 6. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

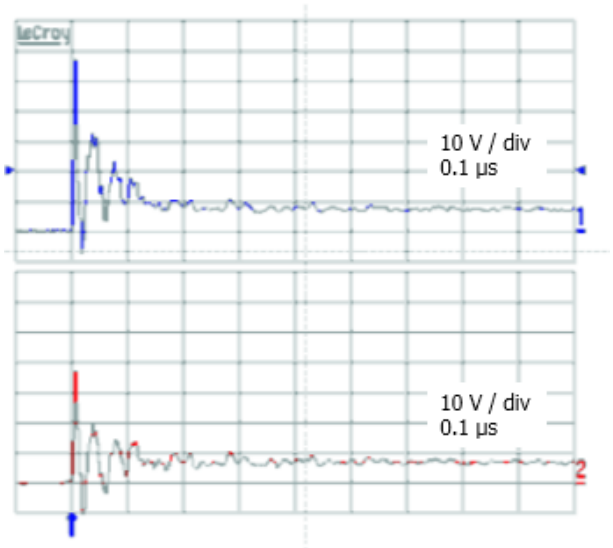
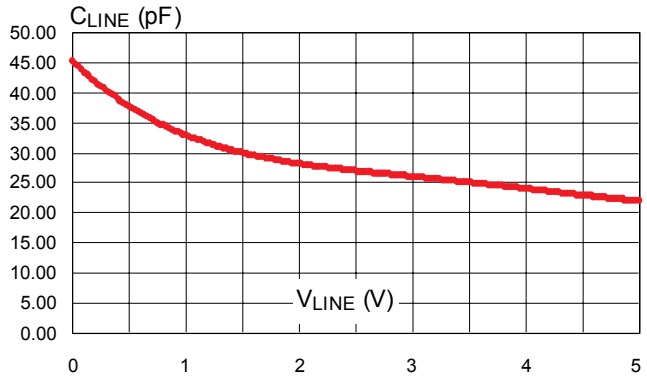


Figure 7. Line capacitance versus reverse voltage applied



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 QFN 3.3x1.5-16L package information

Figure 8. QFN 3.3x1.5-16L package outline

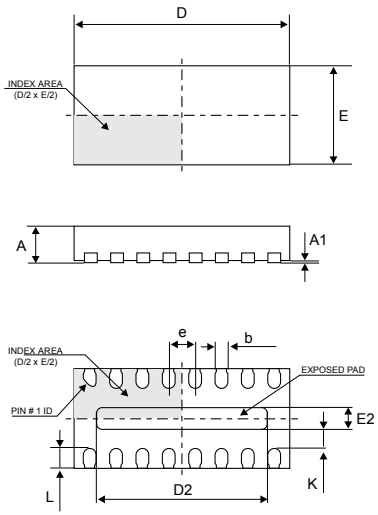


Table 3. QFN 3.3x1.5-16L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.20	3.30	3.40	0.126	0.130	0.134
D2	2.45	2.60	2.70	0.096	0.102	0.106
E	1.40	1.50	1.60	0.055	0.059	0.063
E2	0.20	0.35	0.45	0.008	0.014	0.018
e		0.40			0.016	
K	0.20			0.008		
L	0.20	0.30	0.40	0.008	0.012	0.016

Figure 9. QFN 3.3x1.5-16L footprint (dimensions in mm)

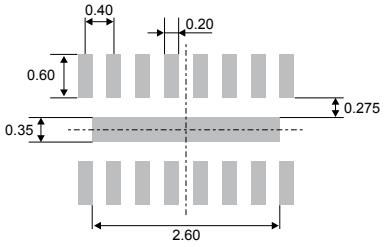


Figure 10. Marking

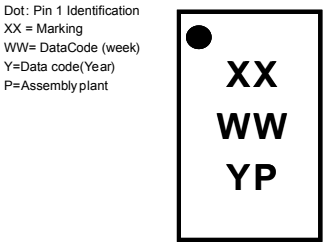
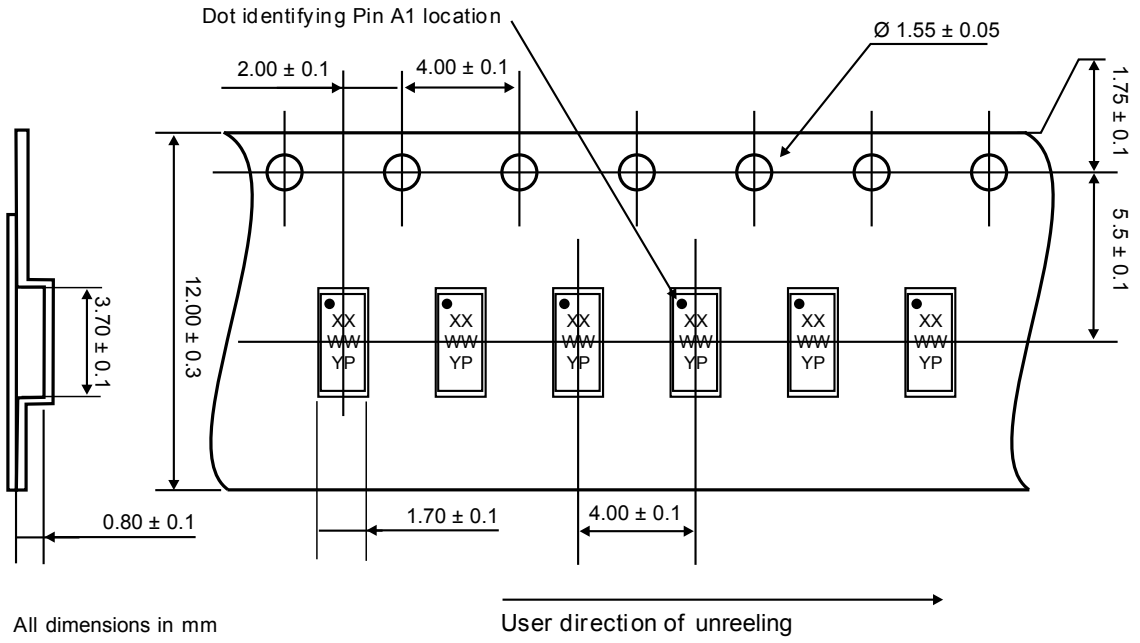


Figure 11. Tape and reel outline



Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L + W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 12. Recommended stencil window position

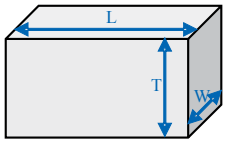
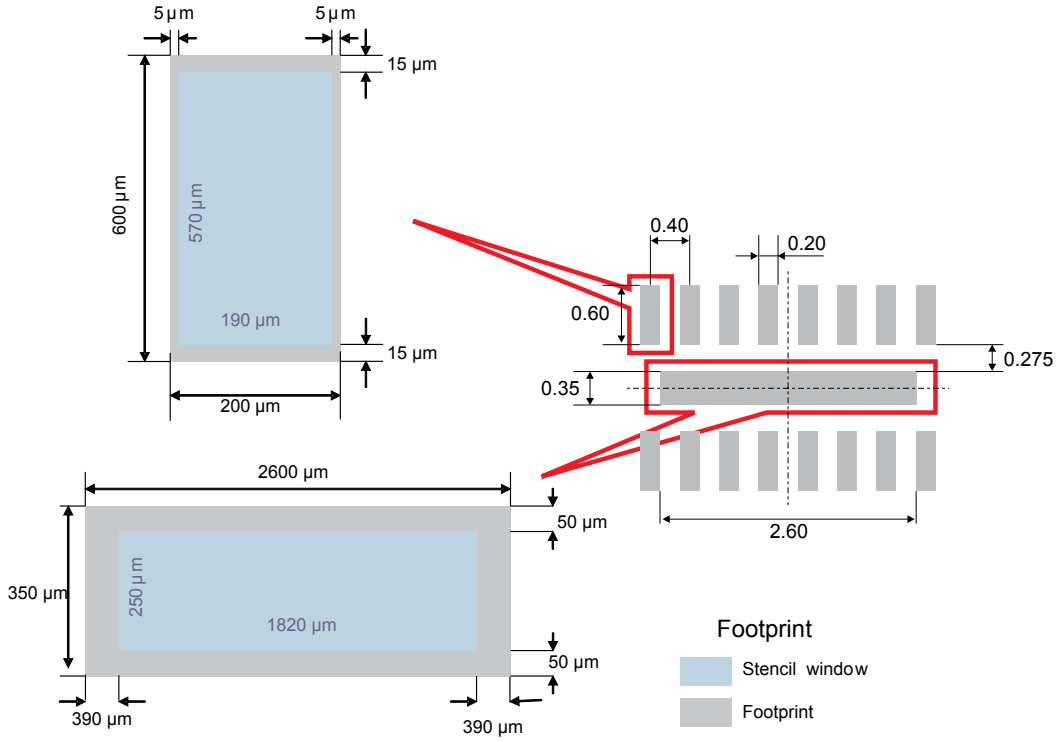


Figure 13. **Recommended stencil opening dimensions**



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3 Placement

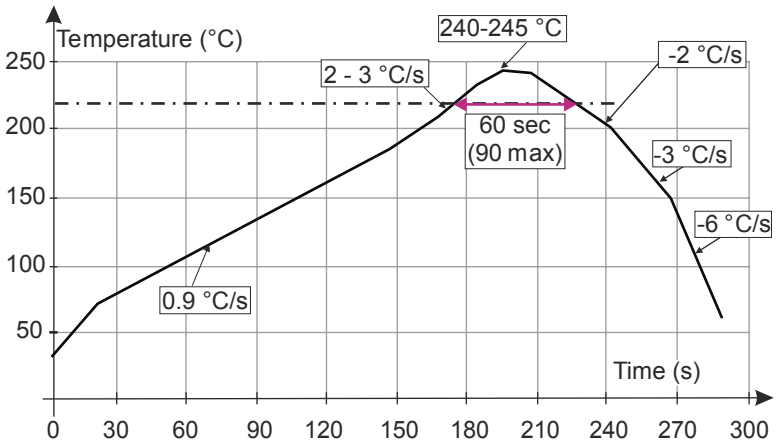
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 14. **ST ECOPACK® recommended soldering reflow profile for PCB mounting**



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 4. Ordering information

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF08-1005M16	H8[1]	QFN	7.9 mg	3000	Tape and reel (7”)

1. *The marking can be rotated by 90° to differentiate assembly location*

Revision history

Table 5. Document revision history

Date	Version	Changes
24-Oct-2006	1	Initial release.
04-Feb-2008	2	Reformatted to current standards. Updated ECOPACK statement. Added Section 4: Recommendation on PCB assembly.
08-Feb-2018	3	Updated Table 1. Absolute maximum ratings (T_{amb} = 25 °C).