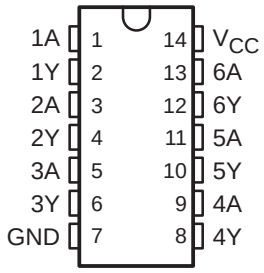
- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Greater Noise Immunity Than Standard Inverters**
- **Operates With Much Slower Than Standard Input Rise and Fall Slew Rates**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  **− Fanout to 15 F Devices**
- **SCR Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

**E OR M PACKAGE**
**(TOP VIEW)**




## description/ordering information

The CD74AC14 contains six independent inverters. This device performs the Boolean function $Y = \overline{A}$.

Each circuit functions as an independent inverter, but because of the Schmitt action, the inverters have different input threshold levels for positive-going ($V_{T+}$) and negative-going ($V_{T-}$) signals.

**ORDERING INFORMATION**

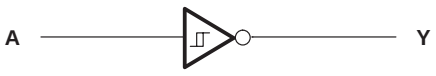
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −55°C to 125°C | PDIP − E | Tube | CD74AC14E | CD74AC14E |
| | SOIC − M | Tube | CD74AC14M | AC14M |
| | | Tape and reel | CD74AC14M96 | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic diagram, each inverter (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 6 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package . . . . . 80°C/W
M package . . . . . 86°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | $T_A$ = 25°C | | −55°C to 125°C | | −40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.5 V to 5.5 V | | −24 | | −24 | | −24 | mA |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 4.5 V to 5.5 V | | 24 | | 24 | | 24 | mA |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | −55°C to 125°C | | −40°C to 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going threshold | | | 5 V | 2.6 | 3.4 | 2.6 | 3.4 | 2.6 | 3.4 | V |
| $V_{T-}$ Negative-going threshold | | | 5 V | 1.6 | 2.4 | 1.6 | 2.4 | 1.6 | 2.4 | V |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | | 5 V | 0.5 | | 0.5 | | 0.5 | | V |
| $V_{OH}$ | $V_I = V_{T+}$ | $I_{OH}$ = −50 µA | 1.5 V | 1.4 | | 1.4 | | 1.4 | | V |
| | | | 3 V | 2.9 | | 2.9 | | 2.9 | | |
| | | | 4.5 V | 4.4 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = −4 mA | 3 V | 2.58 | | 2.4 | | 2.48 | | |
| | | $I_{OH}$ = −24 mA | 4.5 V | 3.94 | | 3.7 | | 3.8 | | |
| | | $I_{OH}$ = −50 mA† | 5.5 V | | | 3.85 | | | | |
| | | $I_{OH}$ = −75 mA† | 5.5 V | | | | | 3.85 | | |
| $V_{OL}$ | $V_I = V_{T-}$ | $I_{OL}$ = 50 µA | 1.5 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12 mA | 3 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.5 | | 0.44 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | 1.65 | | | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 4 | | 80 | | 40 | µA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

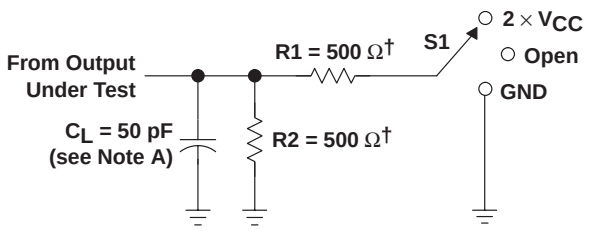
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | −55°C TO 125°C | | −40°C TO 85°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 2.6 | 10.5 | 2.7 | 9.5 | ns |
| $t_{PHL}$ | | | 2.6 | 10.5 | 2.7 | 9.5 | |

## operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 45 | pF |

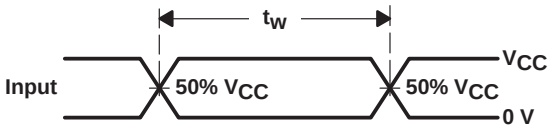
## PARAMETER MEASUREMENT INFORMATION



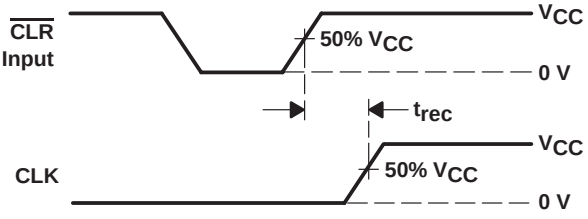

† When $V_{CC}$ = 1.5 V, R1 = R2 = 1 kΩ

**LOAD CIRCUIT**

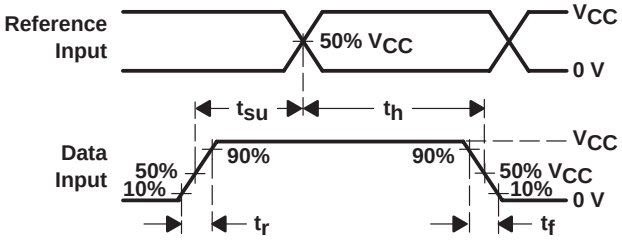
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



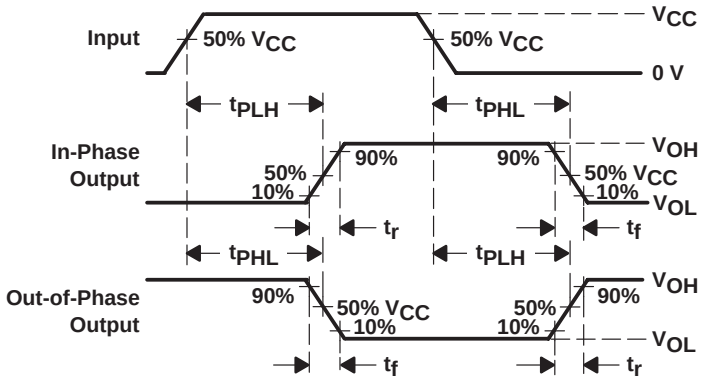

**VOLTAGE WAVEFORMS**
**PULSE DURATION**



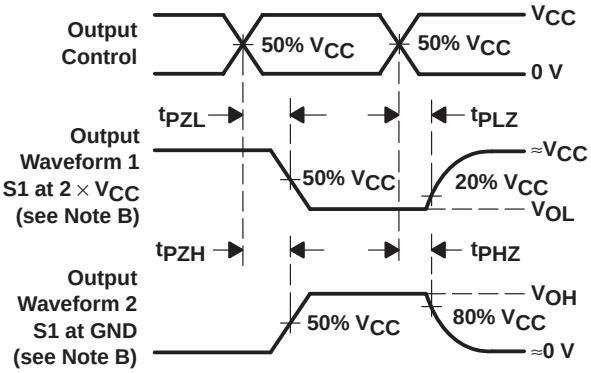

**VOLTAGE WAVEFORMS**
**RECOVERY TIME**




**VOLTAGE WAVEFORMS**
**SETUP AND HOLD AND INPUT RISE AND FALL TIMES**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**




**VOLTAGE WAVEFORMS**
**OUTPUT ENABLE AND DISABLE TIMES**

NOTES: A. $C_L$ includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns. Phase relationships between waveforms are arbitrary.
D. For clock inputs, $f_{max}$ is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
G. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
H. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC14E | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC14E | Samples |
| CD74AC14EE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC14E | Samples |
| CD74AC14M | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC14M | Samples |
| CD74AC14M96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC14M | Samples |
| CD74AC14M96E4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC14M | Samples |
| CD74AC14M96G4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC14M | Samples |
| CD74AC14MG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC14M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

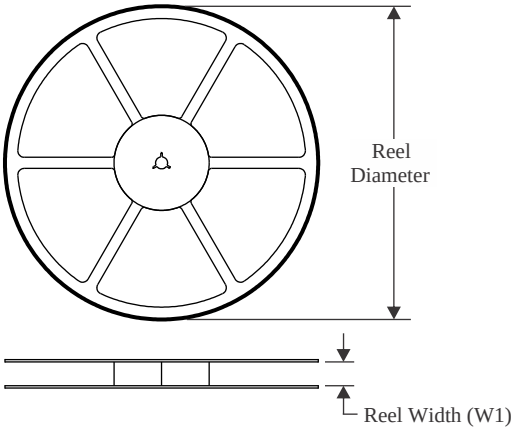
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

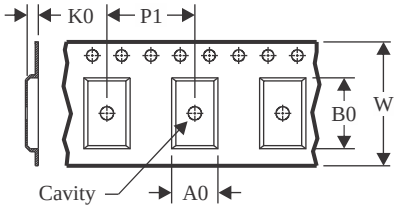
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

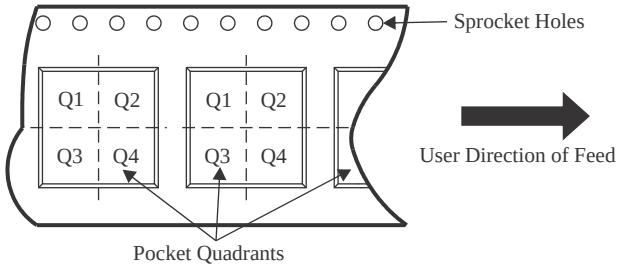



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

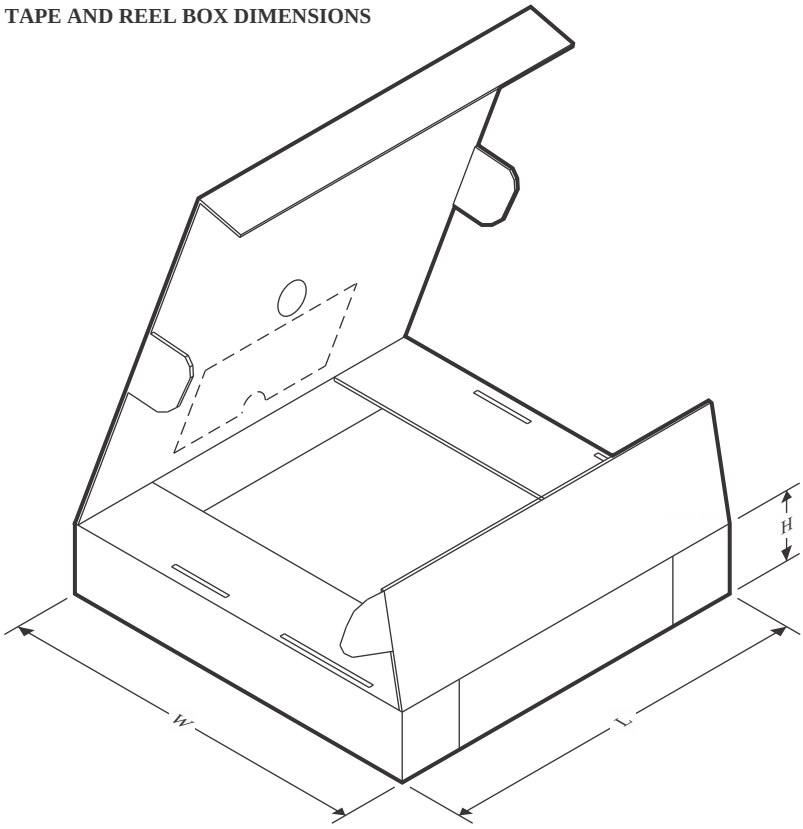
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC14M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

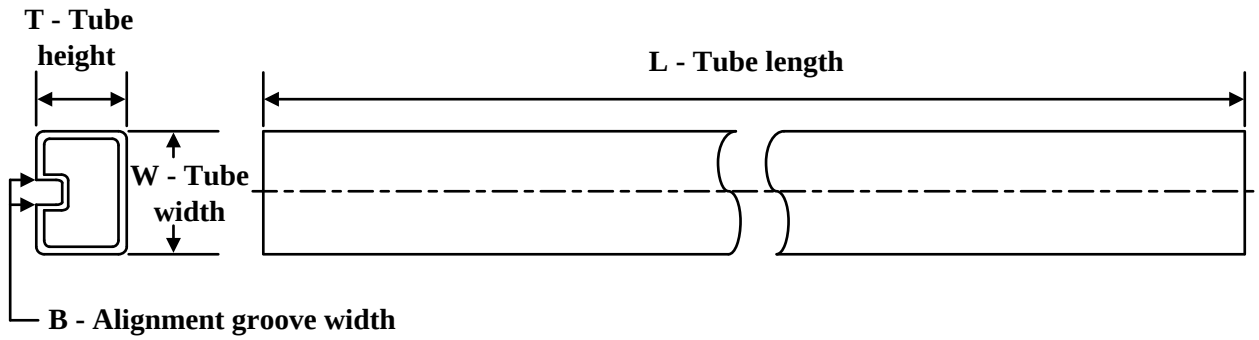
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC14M96 | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

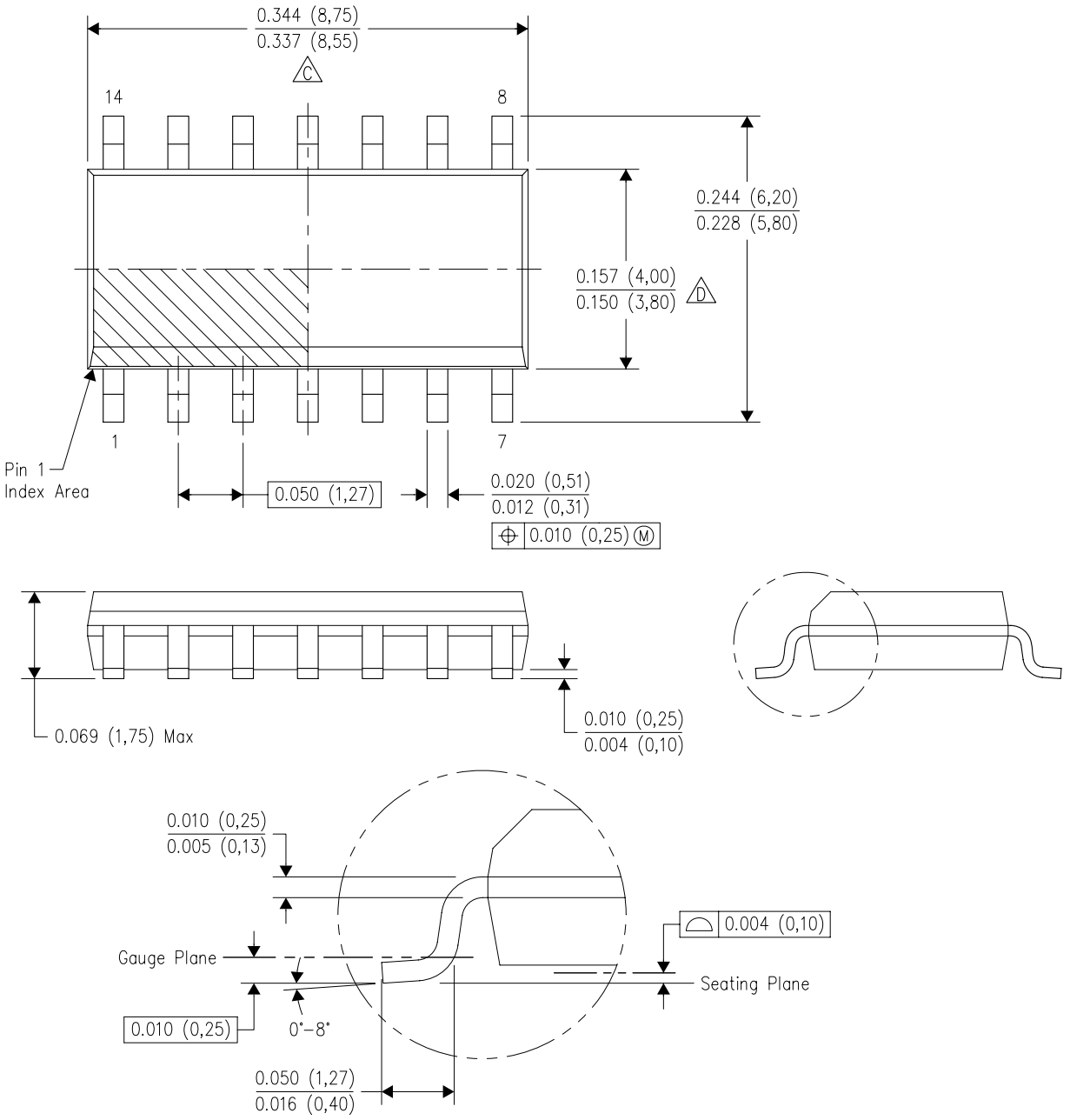
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74AC14E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC14E | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC14EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC14EE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC14M | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| CD74AC14MG4 | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |

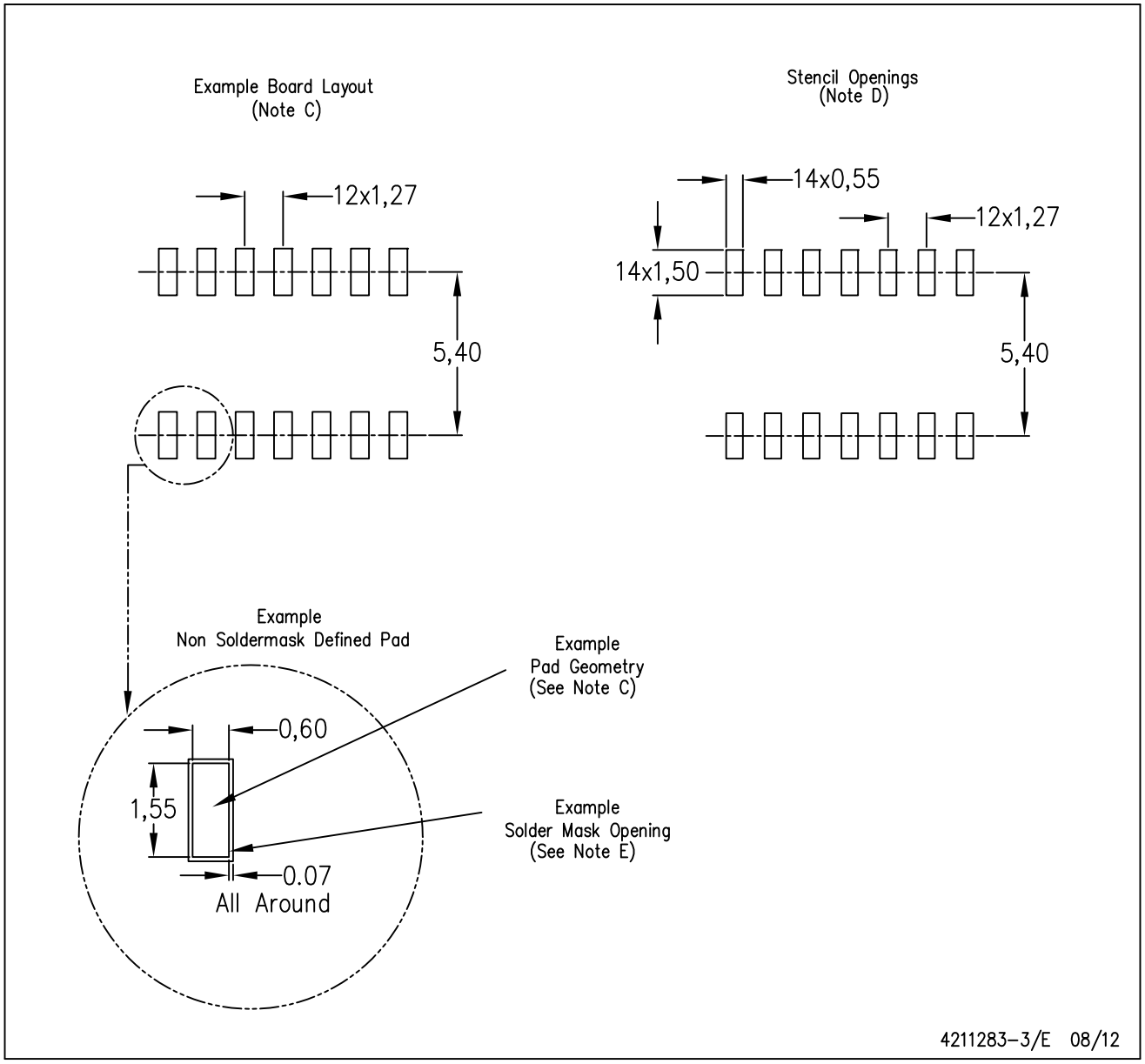
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

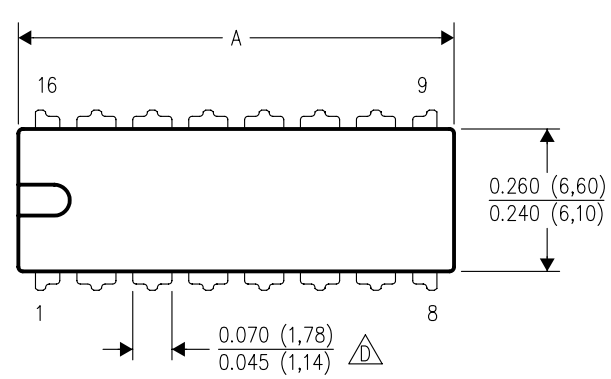



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

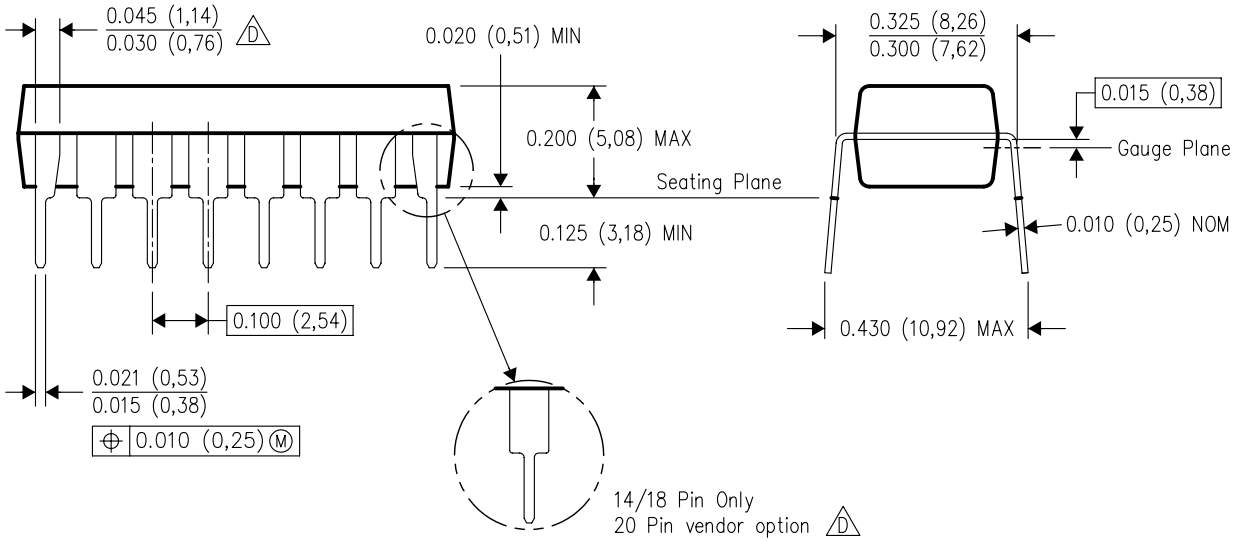
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265