MAX 7000AE, MAX 7000B, & MAX 3000A Devices

December 2005, ver. 2.0 Errata Sheet

Introduction

This errata sheet provides updated information on MAX® 7000AE, MAX 7000B, and MAX 3000A devices, addresses known device issues, and includes workarounds for those issues. Refer to Table 1.

Table 1. MAX 7000AE, MAX 7000B, & MAX 3000A Device Family Issues

Issue	Affected Devices
Specific power sequence situations involving slow rise times for V_{CCIO} or I/O pin voltage can cause I/O source/sink current greater than 300 µA during power-up. *(1) (2)*	MAX 7000B
Fast V_{CCINT} rise times may lead to I/O pin transients during power-up. *(1) (2)*	MAX 7000AE MAX 3000A MAX 7000B

Notes to Table 1:

(1) MAX 9000, MAX 7000, MAX 7000E, MAX 7000S, MAX 7000A (MAX 7128A and MAX 7256A) devices are not hot-socket capable devices and, therefore, have an undefined I/O state during power-up.

(2) Altera is offering permanent recommendations and workarounds for this issue.

MAX 7000B I/O Current During Power Sequencing

Altera has identified that specific power sequence situations involving slow rise times on V_{CCIO} or I/O pin voltage may cause MAX 7000B I/O pins to source/sink current before V_{CCINT} is ramped. These conditions can violate the hot-socketing definition which indicates that these pins should be tri-stated during power-up and should not source/sink more than 300 µA of current per pin. There are two different power sequence situations where I/O pins may source or sink current greater than 300 µA. Table 2 describes the two power sequence issues and their possible workarounds.

Table 2. MAX 7000B I/O Current During Power Sequencing Issues

Power Sequence Situation	Issue	Workarounds *(2)*
V_{CCIO} is ramped before V_{CCINT} *and* V_{CCIO} rise time is slower than 10 ms.	All I/O pins will drive high (source current of up to 45 mA) until V_{CCINT} ramps. *(1)*	1. Ramp V_{CCINT} before V_{CCIO} ramps *or* 2. Decrease V_{CCIO} rise time to faster than 10 ms
V_{CCINT} and V_{CCIO} are grounded *and* a particular I/O pin voltage rises from 0 to 3.3V slower than 10 ms.	That particular I/O pin will sink up to 24 mA, pulling the I/O pin voltage down, until V_{CCINT} or V_{CCIO} ramps.	1. Ramp V_{CCINT} or V_{CCIO} before I/O pin voltage ramps *or* 2. Decrease I/O pin voltage rise time to faster than 10 ms.

Notes to Table 2:

(1) The device's I/O source current does not pose any reliability issues unless it is maintained for an extended period of time.

(2) If the source/sink current is not a concern in the system during power-up, no action is necessary.

I/O Transients During Fast V_{ccint} Rise

Altera has identified that fast V_{CCINT} rise times can lead to pulses on I/O pins during the power-up period on MAX® 7000AE, MAX 3000A, and MAX 7000B devices. This condition can violate the hot-socketing definition that says these pins should be tri-stated during power-up and should not source or sink more than 300 µA of current per pin. There are two different pulses resulting from fast V_{CCINT} rise times, a low pulse transient on any I/O pin, and a separate pulse transient on combinatorial output pins.

Table 3 shows the issues and the MAX devices they affect.

Table 3. MAX I/O Transient During Fast V_{CCINT} Issues	
Issue	**Affected Device Families**
Combinatorial Output Pin Pulse Transient : A low or high pulse can occur on pins programmed to be combinatorial outputs in the design *(1)*	MAX 7000AE *(2)* MAX 3000A *(2)* MAX 7000B
Low Pulse Transient : occurs on any I/O pin *(1)*	MAX 7000AE MAX 3000A

Notes to Table 3:

(1) MAX 9000, MAX 7000, MAX 7000E, MAX 7000S, MAX 7000A (MAX 7128A and MAX 7256A) devices are not hot-socket capable devices and, therefore, have an undefined I/O state during power-up.

(2) Low or high pulse depends on whether the output pin macrocell uses its XOR gate as an inverter.

Table 4 shows the fast rise times that can lead to either transient pulse issue in MAX 7000AE and MAX 3000A devices.

Table 4. Rise Times for Transient Pulses in MAX 7000AE and MAX 3000A	
Device	**V_{CCINT} Rise Time**
EPM7512AE EPM3512A	<1.0 ms
EPM7256AE EPM3256A	<1.0 ms
EPM7128AE EPM3128A	<500 µs
EPM7064AE EPM3064A	<250 µs
EPM7032AE EPM3032A	<125 µs

Table 5 shows the rise times which can lead to the combinatorial output pin pulse transient in MAX 7000B devices.

Table 5. Rise Times for Combinatorial Output Pulse Transient in MAX 7000B	
Device	**V_{CCINT} Rise Time**
EPM7512B	<120 µs
EPM7256B	<120 µs
EPM7128B	<60 µs

EPM7064B	<30 µs
EPM7032B	<30 µs

Combinatorial Transient

This high or low transient can occur on pins configured as combinatorial outputs in the programmed design. Other pin types in the design and dedicated inputs are not affected. This one-time pulse during V_{CCINT} power-up can affect MAX 7000AE, MAX 3000A, and MAX 7000B devices. Fast V_{CCINT} rise times can lead to a timing lag between output pin output enable (OE) and logic array release when transitioning into user mode. The OE signal releases output pins before the logic array is released and temporarily drives output pins with a high or low signal from the logic array.

The one-time pulse is shorter than 20 µs and begins at ~1.8V in the V_{CCINT} rise profile. The V_{OH} of the pulse depends on the level of V_{CCIO} supply. If V_{CCIO} is ramping, then the output pulse will only drive as high as the value of V_{CCIO}. If the pulse occurs, the current source/sink of the device's I/O does not pose any reliability issues. If the short transient pulse is not a concern in the system during power-up, no action is necessary.

For MAX 7000AE and MAX 3000A devices, the pulse polarity, high or low, depends on whether the macrocell's XOR gate driving the combinatorial output pin is inverting or non-inverting. An inverting XOR gate will produce a low pulse; a non-inverting XOR gate will produce a high pulse. This can be determined from the report file equation in the MAX+PLUS® II or the Quartus® II software. The MAX+PLUS II and Quartus II equations for inverting and non-inverting macrocell output are shown below:

MAX+PLUS II Report File:

- If the macrocell output equation shows a (`node_A $ VCC`), the XOR is inverting and a pulse to the output pin is low.
- If the macrocell output equation shows (`node_A $ GND`) or a (`node_A $ node_B`), the XOR is non-inverting and a pulse to the output pin is high.

Quartus II Report File:

- If the macrocell output equation shows `A1L5 =!(A1L5_or_out)`, the XOR is inverting and a pulse to the output pin is low.
- If the macrocell output equation shows `A1L5 = (A1L5_or_out)`, the XOR is non-inverting and a pulse to the output pin is high.

Workaround

If an output pin driving a single low or high pulse during power-up in MAX 7000AE, MAX 3000A, and MAX 7000B devices is an issue for your system, there are a few possible workarounds.

- For MAX 7000AE and MAX 3000A devices, if the high pulse is a problem for your system, check the report file equations to see if any pertinent combinatorial outputs use the macrocell XOR as non-inverting. If the XOR feeding the output is inverting, the pulse will be low instead of high. If you can use reverse logic on this signal, insert an additional inverter before the output pin in the design file. If you cannot use reverse logic, you can use two inverters (macrocells) in series to ensure the output pin is driven by an inverted XOR gate.

- For MAX 7000AE, MAX 3000A, and MAX 7000B devices, modify the design file to register the output pins in question. The combinatorial output pulse transient will only occur on a combinatorial output, not on registered outputs.

- For MAX 7000AE or MAX 3000A devices with a V_{CCINT} rise time faster than the times shown in Table 4, a MAX 7000B device can be used as an alternative since its rise times shown in Table 5 are much faster. MAX 7000B devices use a 2.5-V V_{CCINT} supply and are pin compatible with MAX 7000AE devices.

- Use a V_{CCINT} supply with rise time slower than number shown in Table 4 for MAX 7000AE and MAX 3000A devices or Table 5 for MAX 7000B devices.

Low Pulse Transient

This low pulse transient can occur on any I/O pin (not including dedicated inputs) early in V_{CCINT} power-up. This affects MAX 7000AE and MAX 3000A devices and does not affect 7000B devices. The MAX 7000AE and MAX 3000A V_{CCINT} rise times faster than those shown in Table 4 cause internal nodes (which should be at GND) to charge up, turning on pass gates in the programmable interconnect array (PIA). This short pass gate turn-on period pulls the I/O to ground.

The low pulse is shorter than 500 µs and occurs at ~0.8-V in the V_{CCINT} rise profile. The current source/sink of the devices I/O pins if the pulse occurs does not pose any reliability issues. If the short transient low pulse is not a concern in the system during power-up, no action is necessary.

Workaround

If an output pin driving a low going pulse during power-up in MAX 7000AE and MAX 3000A devices is an issue for your system, there are a few possible workarounds.

- Usually a low going pulse is only an issue for a device on the board that is expecting a pull-up value. The MAX device pulse may pull down the pulled-up signal either partially or totally depending on how fast the V_{CCINT} ramp rate is with respect to the numbers in Table 4. A stronger pull-up resistor can be used to maintain the high value. The pull-up should be chosen such that no more than 24 mA is sunk by a MAX device I/O pin.

- For V_{CCINT} rise time faster than the times shown in Table 4, a MAX 7000B device can be used as an alternative since its rise times shown in Table 5 are much faster. MAX 7000B device use a 2.5-V V_{CCINT} supply and are pin compatible with MAX 7000AE devices.

- Use a V_{CCINT} supply with rise time slower than number shown in Table 4 for MAX 7000AE, MAX 3000A devices.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com