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APPLICATION NOTE 302

DS2141, DS21Q41, DS21Q43 8-MHz System Clock Operation

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Abstract: The application note describes how to design a backplane of 8.192MHz that simultaneously connects to any four framers of the following: DS21Q41 quad T1 framer, DS21Q43 E1 framer, DS2141 T1 controller, DS2151 T1 single chip transceiver (SCT), and DS2153 E1 SCT.

The DS2141, DS21Q41, DS21Q43, DS2151 and DS2153 PCM signals can interface to an 8 MHz system backplane. Typically this application is used to multiplex four 2.048 MHz PCM streams onto a single 8 MHz PCM stream. To accomplish this the elastic stores are enabled and placed in the 2.048 MHz SYSCLK mode. **Figure 1** describes a timing scheme in which a single RSYNC is generated for all four framers. Each framer in turn is driven with an 8.192 MHz clock burst of 8 cycles. Each clock burst causes the elastic store to output 1 DS0. This results in a Byte Interleaved 8.192 MHz PCM stream.

DS21Q41/DS21Q43 OR DS2141/DS2151/DS2153

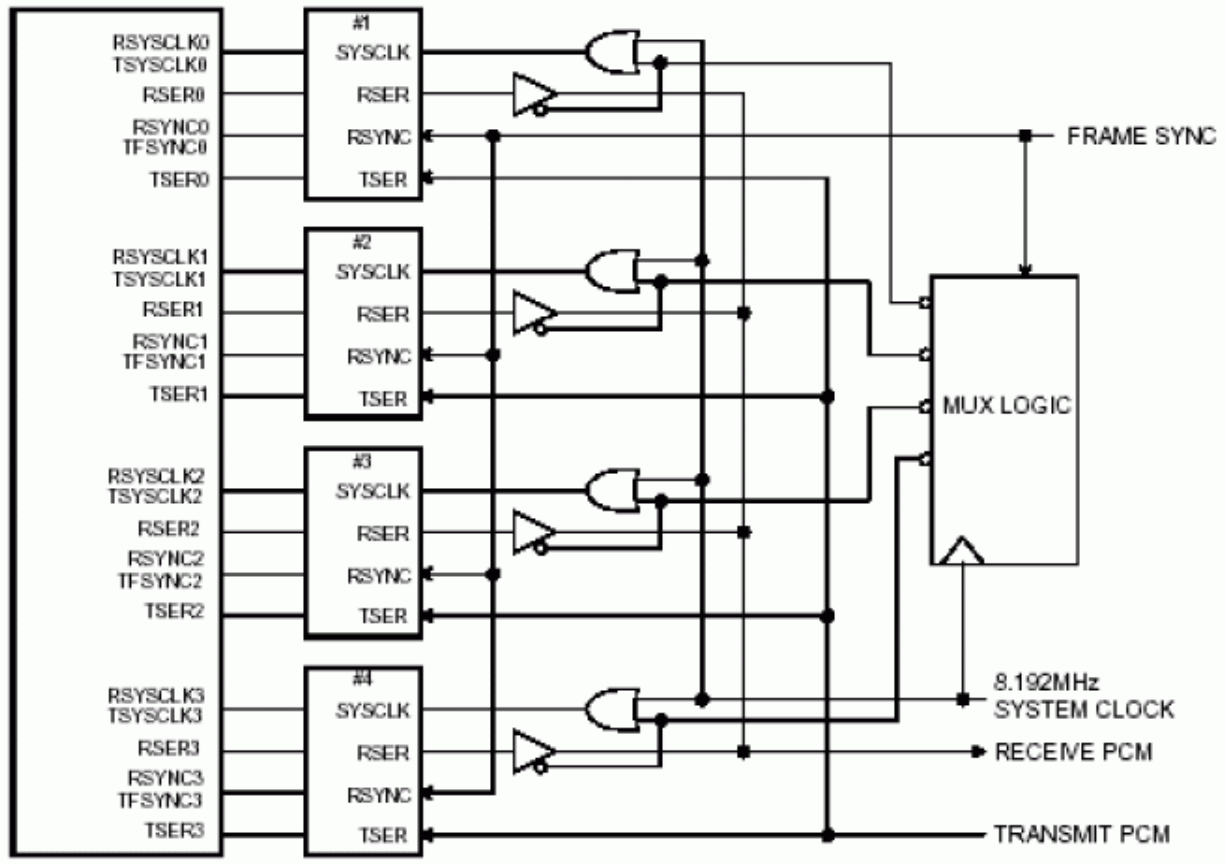


Figure 1. Quad multiplexed frames.

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