60V, 4A Synchronous Step-Down Regulator with Rail-to-Rail Programmable Output

FEATURES

- **Wide V_{IN} Range: 3.1V to 60V**
- **Wide V_{OUT} Range: 0V to (V_{IN} – 0.5V)**
- **Single Resistor V_{OUT} Programming**
- **Integrated 110mΩ Top N-Channel/50mΩ Bottom N-Channel MOSFETs**
- **95% Efficiency with 12V_{IN} and 5V_{OUT}**
- **Regulated I_Q: 440µA, Shutdown I_Q: 18µA**
- **Accurate Current Monitoring (±4%) without Sense Resistor**
- **Accurate Resistor Programmable Frequency (300kHz to 3MHz) with ±50% Frequency Sync Range**
- **Accurate Programmable Output Current**
- **Input Voltage Regulation for MPPT Applications**
- ±0.8% Output Voltage Accuracy
- Peak Current Mode Operation
- Programmable Wire Drop Compensation
- Burst Mode® Operation, Forced Continuous Mode
- Internal Compensation and Programmable Soft-Start
- Overtemperature Protection
- Available in Thermally Enhanced 28-Lead (4mm × 5mm) QFN and TSSOP Packages

APPLICATIONS

- Industrial Applications
- Automotive Applications

DESCRIPTION

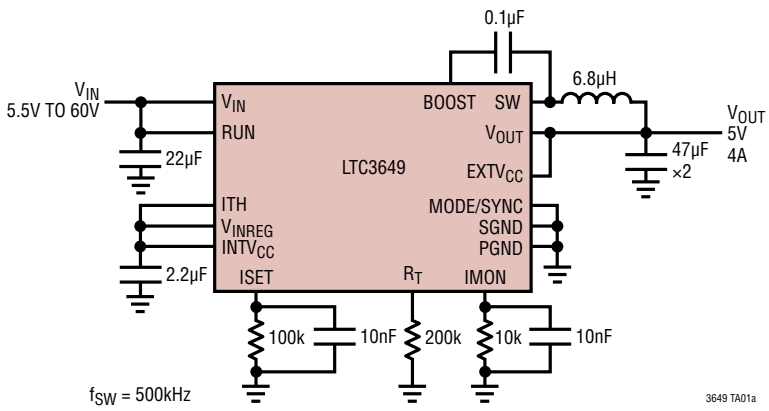
The LTC®3649 is a high efficiency 60V, 4A synchronous monolithic step-down regulator. The regulator features a single resistor programmable output voltage, internal compensation and high efficiencies over a wide V_{OUT} range.

The step-down regulator operates from an input voltage range of 3.1V to 60V and provides an adjustable rail-to-rail output range from (V_{IN} – 0.5V) to ground while delivering up to 4A of output current. The switching frequency is also adjusted with an external resistor. A user-selectable mode input is provided to allow the user to trade off ripple noise for efficiency at light loads; Burst Mode operation provides the highest efficiency at light loads, while forced continuous mode provides low output ripple. The MODE/SYNC pin can also be used to allow the user to synchronize the switching frequency to an external clock.

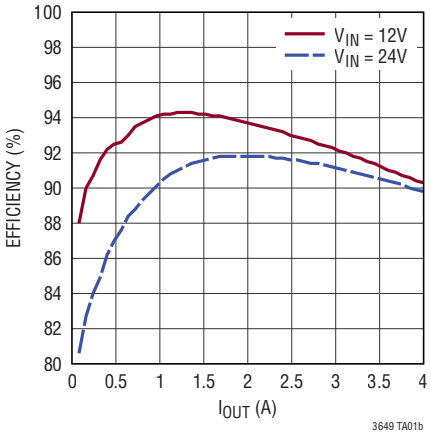
The LTC3649 operates with a peak current mode architecture that allows for fast transient response with inherent cycle-to-cycle current limit protection. It also features programmable output current limit, current monitoring and input voltage regulation.

TYPICAL APPLICATION

24V to 5V_{OUT} Burst Mode Operation



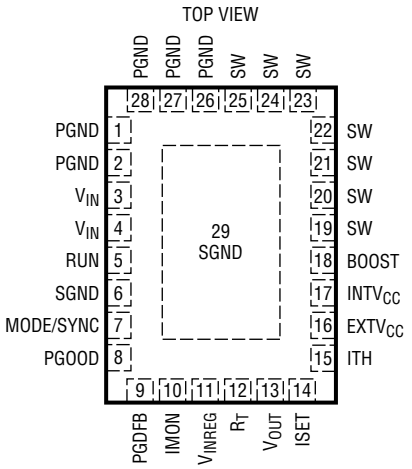
Efficiency with V_{OUT} = 5V



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

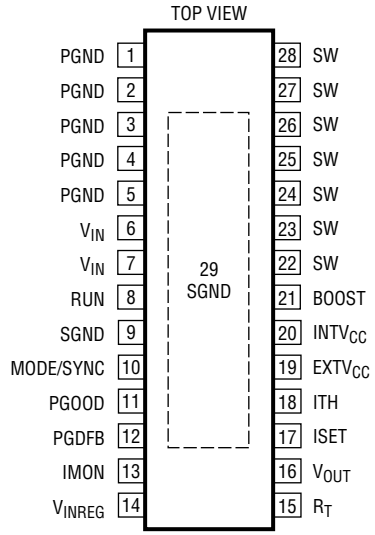
V_{IN} Voltage (Note 3) ..... 64V to –0.3V
ISET, OUT Voltage ..... 64V to –0.3V
RUN Voltage ..... 64V to –0.3V
MODE/SYNC Voltage ..... 6V to –0.3V
PGDFB, R_T ..... $INTV_{CC}$ +0.3V to –0.3V
$EXTV_{CC}$ Voltage ..... 28V to –0.3V
IMON, PGOOD Voltage ..... 4V to –0.3V
V_{INREG}, ITH Voltage ..... 4V to –0.3V
Operating Junction
Temperature Range (Notes 5, 7) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3.4°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 30°C/W, θ_{JC} = 5°C to 10°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3649#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3649EUFD#PBF	LTC3649EUFD#TRPBF	3649	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3649IUFD#PBF	LTC3649IUFD#TRPBF	3649	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3649EFE#PBF	LTC3649EFE#TRPBF	LTC3649	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3649IFE#PBF	LTC3649IFE#TRPBF	LTC3649	28-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C. (Note 5) V_{IN} = 24V, V_{EXTVCC} = 0V unless otherwise noted. (Notes 5, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Operating Voltage Range			3.1		60	V
V_{OUT}	Output Operating Voltage Range	(Note 4)		0.05		V_{IN}	V
I_{VIN}	Input Quiescent Current	Shutdown Mode; V_{RUN} = 0V			18	30	µA
		Burst Mode Operation			440	600	µA
		FC Mode (Note 6)			1.4	2.5	mA
I_{ISET}	Reference Current	V_{ISET} = 3.3V		49.6	50	50.4	µA
			●	49.4	50	50.6	µA
$\Delta V_{OUT(LOAD+LINE)}$	Output Voltage Load + Line Regulation		●		0.1	0.5	%
$V_{EA(OFFSET)}$	Error Amp Input Offset	V_{ISET} = 3.3V		–5		5	mV
g_m (EA)	Error Amplifier Transconductance	V_{ITH} = 0.7V, V_{OUT} = 3.3V		400	550	700	µS
I_{LSW}	Topside NMOS Switch Leakage				0.1	1	µA
R_{SW-GND}	SW Resistance to GND			0.5	1	1.5	MΩ
$R_{DS(ON)}$	Topside NMOS On-Resistance				110		mΩ
	Bottom Side NMOS On-Resistance				50		mΩ
D_{MAX}	Maximum Duty Cycle	V_{ISET} = V_{IN} (Note 4)			95		%
$t_{ON(MIN)}$	Minimum On-Time				60		ns
V_{RUN}	RUN Input Rising		●	1.08	1.2	1.32	V
	RUN Hysteresis				120		mV
I_{RUN}	RUN Input Current	V_{RUN} = 12V			0	10	nA
$V_{MODE/SYNC}$	Burst Mode Operation					0.4	V
	FC Mode			1.2			V
$I_{MODE/SYNC}$	MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 0V		–8	–5		µA
I_{LIM}	Peak Current Limit			5.7	6	6.3	A
			●	5.4	6	6.6	A
V_{UVLO}	V_{INTVCC} Undervoltage Lockout	V_{IN} Rising	●	2.4	2.65	2.9	V
$V_{UVLO(HYS)}$	V_{INTVCC} Undervoltage Lockout Hysteresis				200		mV
V_{OVLO}	V_{IN} Overvoltage Lockout Rising			64	68		V
$V_{OVLO(HYS)}$	V_{IN} Overvoltage Lockout Hysteresis				2	4	V
f_{OSC}	Oscillator Frequency	R_T = 100kΩ	●	0.92	1.00	1.08	MHz
f_{SYNC}	SYNC Capture Range	% of Programmed Frequency		50		150	%
V_{INTVCC}	V_{INTVCC} LDO Output Voltage			3.25	3.45	3.65	V
		V_{IN} > 5.0V, V_{EXTVCC} > 3.2V		2.85	3.0	3.15	V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage			3.1	3.15	3.2	V
			●	3.25			V
R_{VOUT}	V_{OUT} Resistance to GND	V_{OUT} = 5V		80	100	120	kΩ
I_{PGDFB}	PGDFB Leakage Current	V_{PGDFB} = 0.6V			0	100	nA
OV_{PGDFB}	Output Overvoltage PGOOD Upper Threshold	PGFB Rising		0.63	0.645	0.66	V
UV_{PGDFB}	Output Undervoltage PGOOD Lower Threshold	PGFB Falling		0.54	0.555	0.57	V
ΔV_{PGDFB}	PGOOD Hysteresis	PGFB Returning			10		mV
R_{PGOOD}	PGOOD Pull-Down Resistance				550		Ω
$I_{PGOOD(LEAK)}$	PGOOD Leakage Current	V_{PGOOD} = 3.3V				100	nA
t_{PGOOD}	PGOOD Delay	PGOOD Low to High			16		Switch Cycles
		PGOOD High to Low			64		Switch Cycles
A_{IMON}	I_{OUT}/I_{IMON}	Ratio of Output Current to I_{IMON}		38.5	40	41.5	k
		Current	●	36	40	44	k
I_{IMON}	IMON Pin Current	I_{OUT} = 4A		96	100	104	µA
			●	90	100	110	µA
V_{IMON}	Regulated I_{MON} Voltage Under Output Current Regulation		●	1.94	2.0	2.06	V
V_{VINREG}	Input Voltage Regulation Voltage		●	1.85	2.0	2.15	V
I_{VINREG}	V_{INREG} Leakage Current	V_{VINREG} = 3.3V			0	0.1	µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referred to V_{SGND}/V_{PGND}.

Note 3: Transient absolute maximum voltages should not be applied for more than 4% of the switching duty cycle.

Note 4: V_{OUT} can be programmed to V_{IN} if the ISET pin is driven to that voltage. If a resistor is used to program V_{ISET}, the current into the ISET pin will decrease as V_{ISET} approaches V_{IN}. Refer to the ISET current vs V_{ISET} graph as an example and reference. Furthermore, during high I_{OUT} and high duty cycle operation, V_{OUT} may be limited by the voltage drop across the top switch. Refer to the High Duty Cycle/Dropout Operation section for more details.

Note 5: The LTC3649 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3649E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3649I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

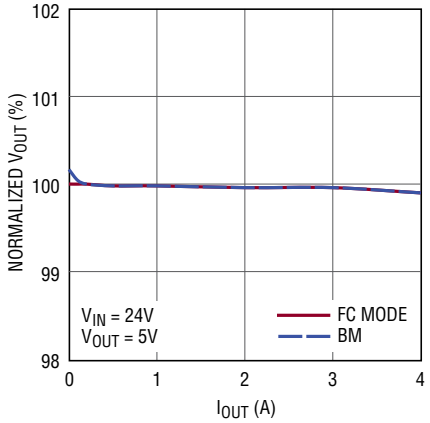
Note 6: The quiescent current in FC mode does not include switching loss of the power FETs.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

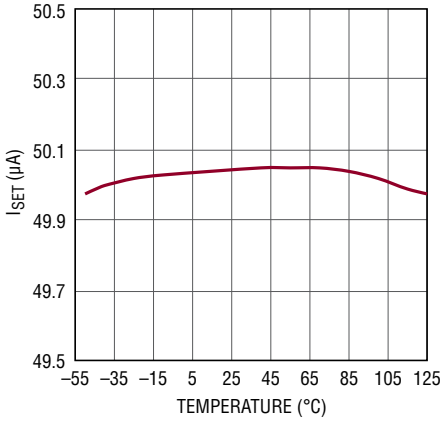
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

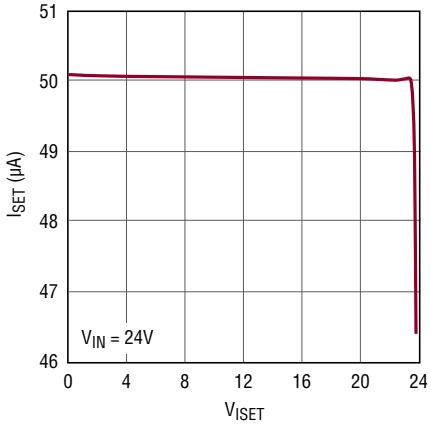
Load Regulation



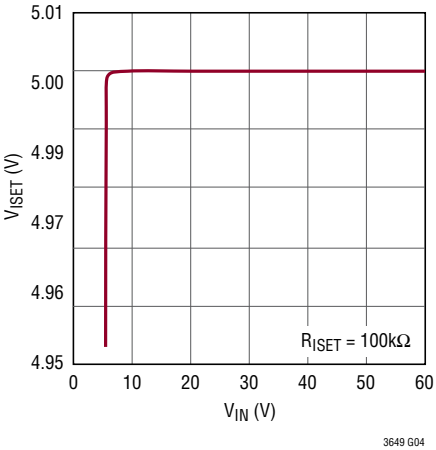
ISET Current vs Temperature



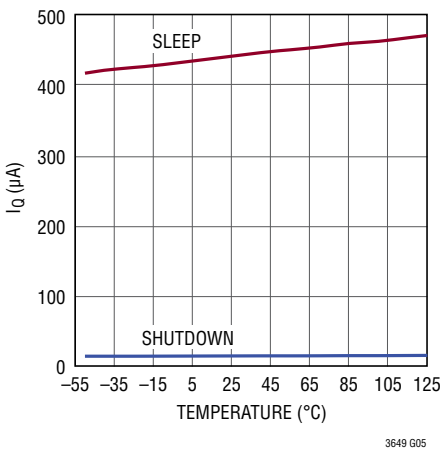
ISET Current vs V_{ISET}



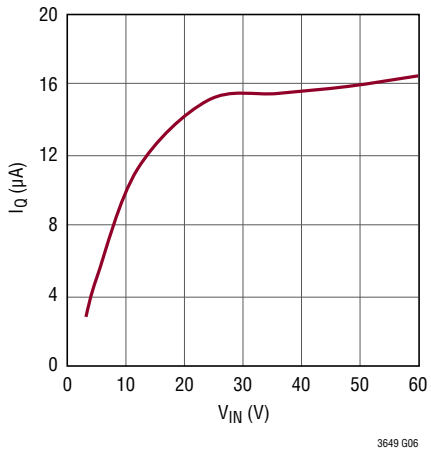
ISET Voltage Line Regulation



Quiescent Current vs Temperature

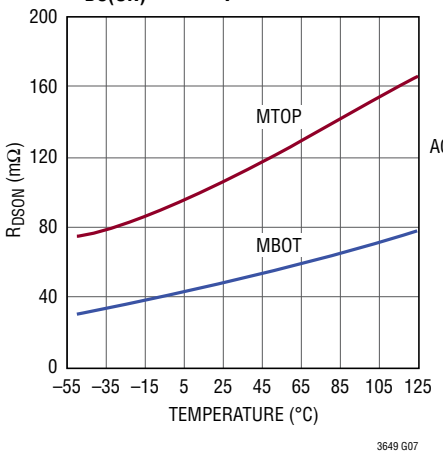


Shutdown Current vs V_{IN}

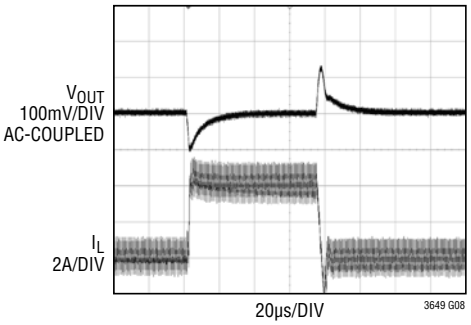


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs Temperature

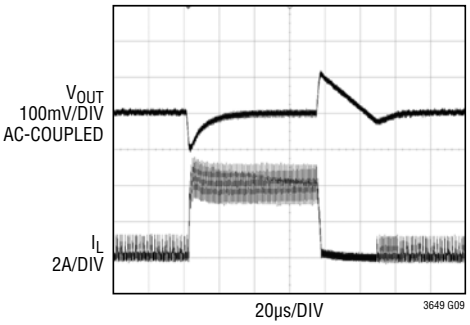


Transient Response, CCM



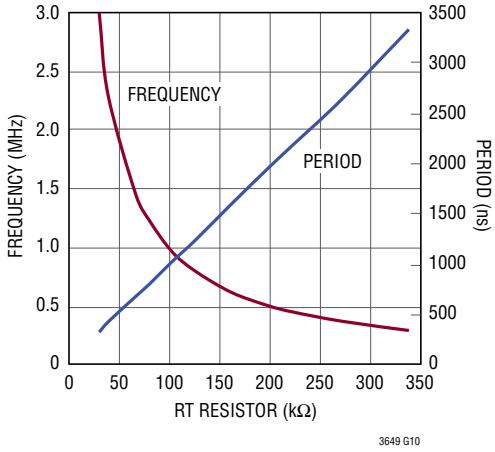
V_{IN} = 24V, V_{OUT} = 5V
I_{OUT} = 0A TO 4A, L = 2.2µH, f_{SW} = 1MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
FC MODE, C_{OUT} = 2× 47µF

Transient Response, Burst Mode

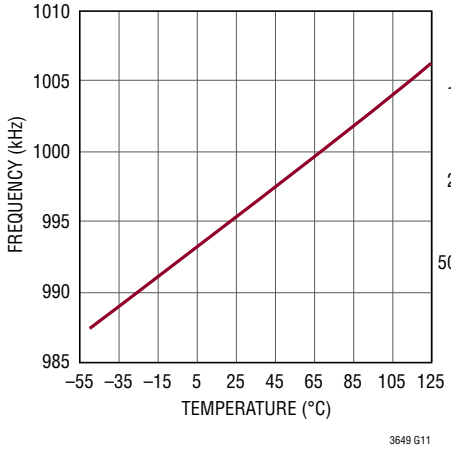


V_{IN} = 24V, V_{OUT} = 5V
I_{OUT} = 0.2A TO 4A, L = 2.2µH, f_{SW} = 1MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
BURST MODE, C_{OUT} = 2× 47µF

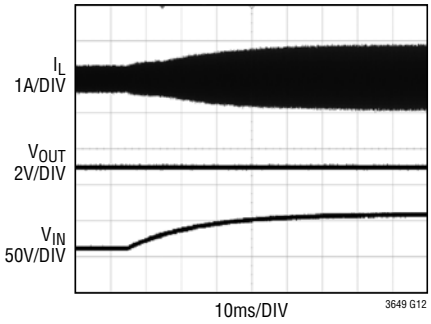
Switching Frequency/Period vs R_T



Switching Frequency vs Temperature

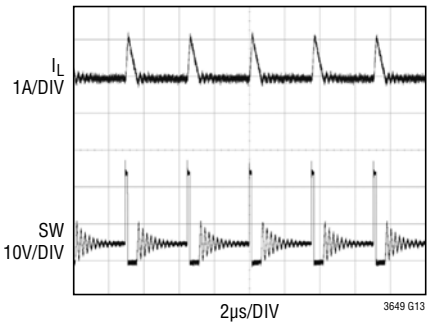


Output Regulation with V_{IN} Slew



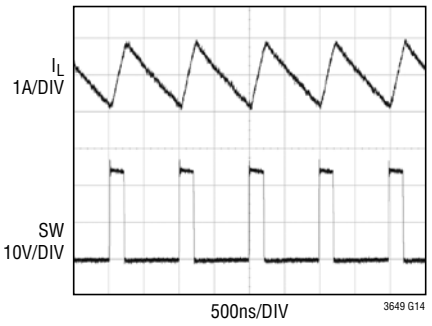
V_{IN} = 12V TO 60V, V_{OUT} = 5V
I_{OUT} = 0A, L = 2.2µH, f_{SW} = 2.25MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
FC MODE, C_{OUT} = 2× 47µF

Burst Mode Operation



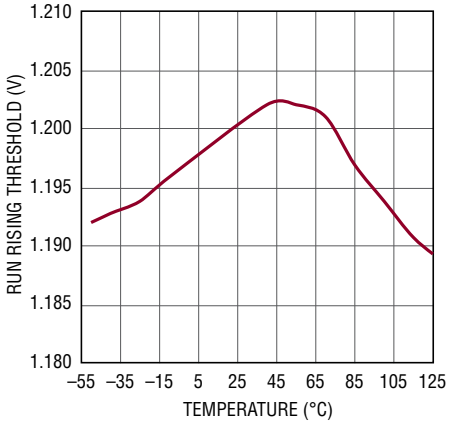
V_{IN} = 24V, V_{OUT} = 5V
I_{OUT} = 100mA, L = 2.2µH, f_{SW} = 1MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
BURST MODE, C_{OUT} = 2× 47µF

Continuous Conduction Mode Operation



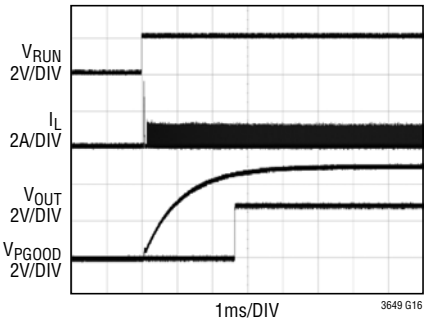
V_{IN} = 24V, V_{OUT} = 5V
I_{OUT} = 0A, L = 2.2µH, f_{SW} = 1MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
FC MODE, C_{OUT} = 2× 47µF

Run Rising Threshold vs Temperature



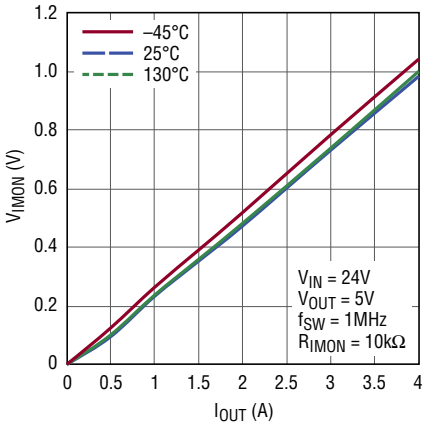
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-up Waveform

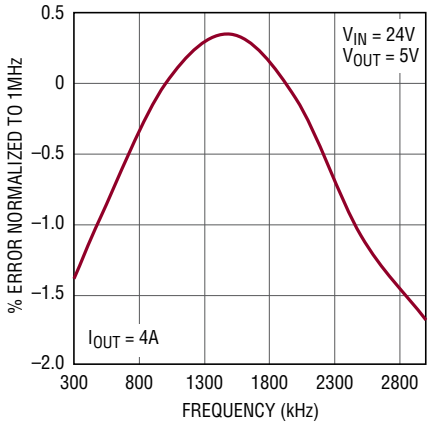


V_{IN} = 24V, R_{ISET} = 100kΩ
R_{LOAD} = 120Ω, L = 2.2µH, f_{SW} = 1MHz
R_{ITH} = 4kΩ, C_{ITH} = 2.2nF, C_{ITHP} = 47pF
BURST MODE, C_{OUT} = 2× 47µF

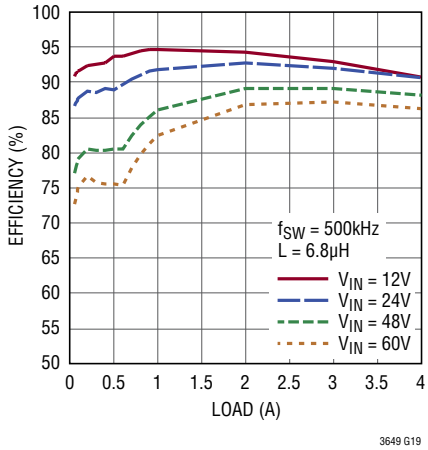
V_{IMON} vs Load (Temperature)



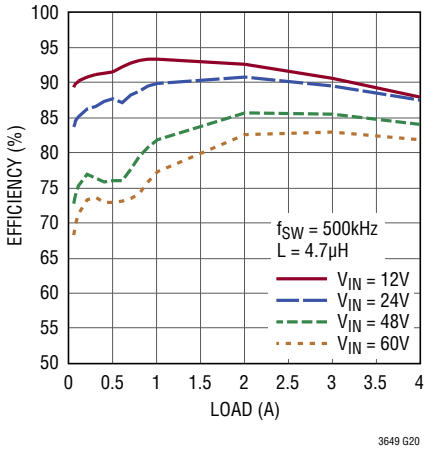
V_{IMON} Error vs Frequency



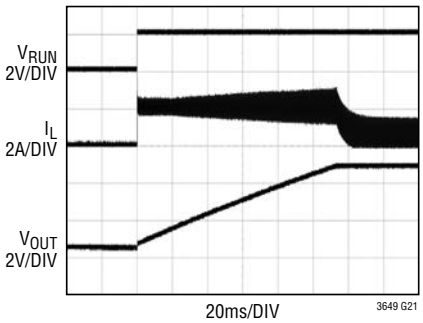
Efficiency vs Load Current at $5V_{OUT}$



Efficiency vs Load Current at $3.3V_{OUT}$

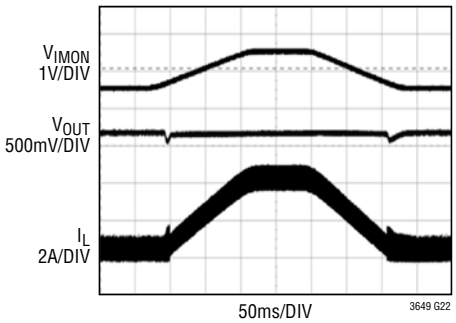


Output Capacitor Charging with Fixed Average Current Limit



V_{IN} = 24V, R_{ISET} = 100kΩ
R_{LOAD} = 10Ω, L = 2.2µH R_{ITH} = 4kΩ,
C_{ITH} = 2.2nF, C_{ITHP} = 47pF, R_{IMON} = 40kΩ,
C_{IMON} = 0.47nF, C_{OUT} = 2× 47µF + 36mF

Load Step with Cable Drop Compensation



CABLE DROP RESISTANCE OF 200mΩ

PIN FUNCTIONS (QFN/TSSOP)

PGND (Pins 1, 2, 26-28/Pins 1-5): Ground Pins for Power Switch.

V_{IN} (Pin 3, 4/Pins 6, 7): Input Supply Pin of the Step-Down Regulator.

RUN (Pin 5/Pin 8): Logic Controlled RUN Input. Do not leave this pin floating. Place a resistor divider from V_{IN} to GND for an accurate V_{IN} undervoltage threshold.

SGND (Pins 6, 29/Pins 9, 29): Signal Ground Pin of the Step-Down Regulator. The exposed pad must be soldered to PCB ground for electrical connection and rated thermal performance.

MODE/SYNC (Pin 7/Pin 10): Mode Select and Oscillator Synchronization Input of the Step-Down Regulator. Leave MODE/SYNC floating for forced continuous mode operation or tie MODE/SYNC to GND for Burst Mode operation. Furthermore, connecting MODE/SYNC to an external clock will synchronize the internal oscillator to the external clock signal and put the part in forced continuous mode.

PGOOD (Pin 8/Pin 11): V_{OUT} Within Regulation Indicator. PGOOD is pulled to GND when V_{PGFB} is more than 0.645V or less than 0.555V.

PGDFB (Pin 9/Pin 12): Power Good Feedback. Place a resistor divider from V_{OUT} to GND to detect power good level.

IMON (Pin 10/Pin 13): Output Current Monitoring Pin. The current coming out of this pin is equal to 1/40,000 of the average output current.

V_{INREG} (Pin 11/Pin 14): Input Voltage Regulation Sense Input. Place a resistor divider from V_{IN} to GND to program the level of input voltage regulation.

R_T (Pin 12/Pin 15): Oscillator Frequency Programming Pin. Connect an external resistor between 333.3k to 33.3k from R_T to GND to program the frequency from 300kHz to 3MHz respectively. Since the synchronization range is limited to ±50% of the set frequency, be sure that either the external clock is within this range or R_T is set to accommodate the external clock for proper frequency lock.

V_{OUT} (Pin 13/Pin 16): Output Voltage Error Amplifier Input Pin. Connect to the output of the LTC3649 voltage regulator.

ISET (Pin 14/Pin 17): Accurate 50µA Bias Current and Positive Input to the Error Amplifier. Connect an external resistor from this pin to SGND to program the output voltage. Connecting an external capacitor from ISET to ground will soft start the output voltage by reducing current inrush during start-up.

ITH (Pin 15/Pin 18): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage. Tying this pin to $INTV_{CC}$ activates internal compensation.

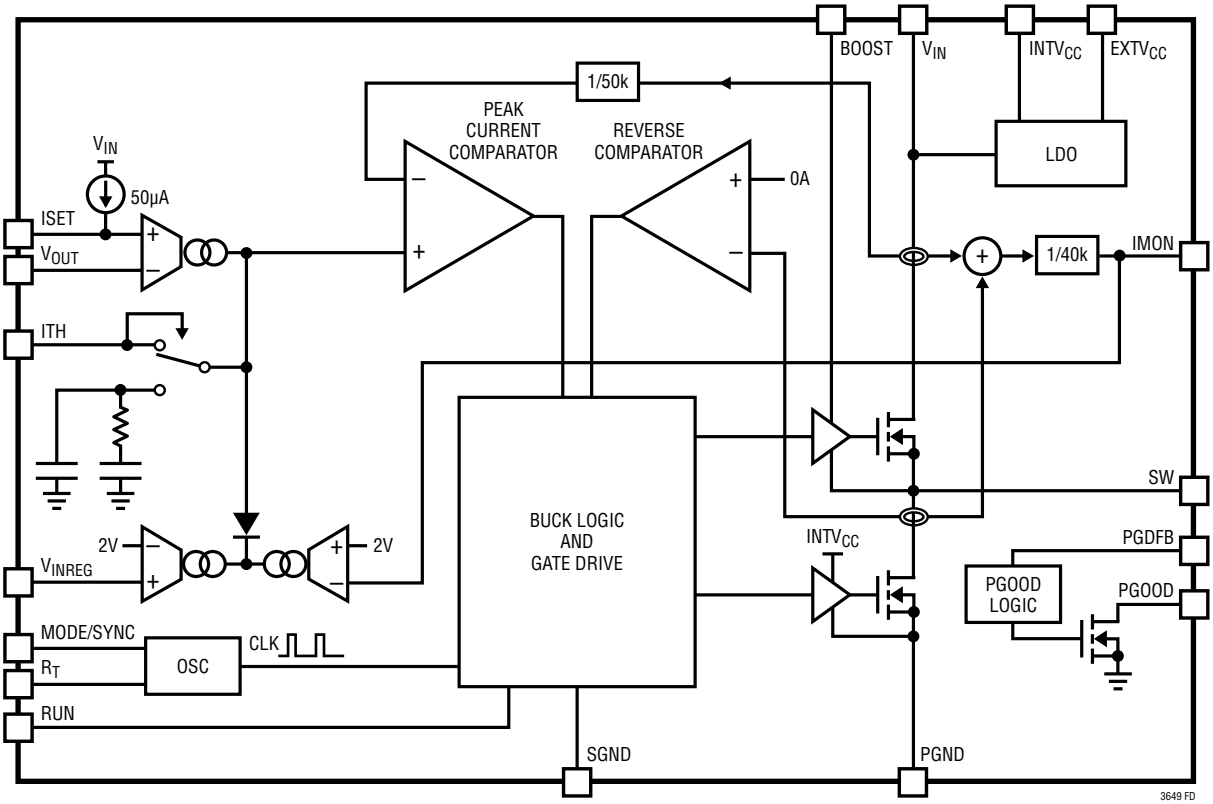
$EXTV_{CC}$ (Pin 16/ Pin 19): External Power Input to the Internal Regulator. The internal regulator will draw current from $EXTV_{CC}$ instead of V_{IN} when $EXTV_{CC}$ is tied to a voltage higher than 3.2V and V_{IN} is above 5V. For output voltages at or above 3.3V and less than 28V, this pin can be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT}, locally bypass with at least a 1µF to GND.

$INTV_{CC}$ (Pin 17/Pin 20): Low Dropout Regulator. Locally bypass with at least 2.2µF to GND.

BOOST (Pin 18/Pin 21): Boosted Floating Driver Supply for Internal Top Power MOSFET. Place a 0.1µF bootstrap capacitor between BOOST and SW.

SW (Pins 19-25/Pins 22-28): Switch Node Connection to the Inductor of the Step-Down Regulator.

FUNCTIONAL DIAGRAM



OPERATION

The LTC3649 is a current mode monolithic step-down regulator. The accurate 50µA bias current on the I_{SET} pin allows the user to program the output voltage in a unity-gain buffer fashion with just one external resistor from the I_{SET} pin to GND (R_{SET}). The output voltage is set such that:

$$V_{OUT} = 50\mu A \bullet R_{SET}$$

The LTC3649 operates through a wide V_{IN} range, and its frequency can be programmed to a wide range with the R_T resistor. To suit a variety of applications, the MODE/SYNC pin allows the user to trade off output ripple for efficiency.

Main Control Loop

In normal operation, the internal top power MOSFET is turned on at the beginning of a clock pulse. The inductor current is allowed to ramp up to a peak level. Once that level is reached, the top power switch is turned off and the bottom switch is turned on until the next clock cycle. The peak inductor current is determined by sensing the voltage drop across the SW and V_{IN} nodes of the top power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor peak current. The error amplifier, EA, adjusts this ITH voltage by comparing the V_{OUT} voltage with the voltage on ISET. If the load current increases, it causes a drop in V_{OUT} relative to V_{ISET}. This causes the ITH voltage to rise until the average inductor current matches that of the load current.

OPERATION

Low Current Operation

Burst Mode operation can be selected by connecting the MODE/SYNC pin to GND. In this mode, the LTC3649 will automatically transition from continuous mode operation to Burst Mode operation when the load current is low. A reverse current comparator looks at the voltage across SW to GND and turns off the bottom power MOSFET when that voltage difference approaches zero. This prevents the inductor current from going negative. An internal burst clamp is set to be approximately 1A, which means that in Burst Mode operation, the peak inductor current will never go below 1A regardless of what the ITH voltage demands the peak current to be. As a result, when the load is low enough, V_{OUT} will rise relative to V_{ISET} because the average programmed inductor current is above the load current, thus driving V_{ITH} low. Once the ITH voltage is driven below an internal threshold (~400mV), the switching regulator will enter its sleep mode and wait for V_{OUT} to drop and V_{ITH} to rise above the threshold before it starts to switch again. During sleep mode, the quiescent current of the part is reduced to less than 400µA to conserve input power. The LTC3649 is designed to operate with single burst pulse behavior to minimize output voltage ripple while keeping the efficiency high at light loads. Lastly, if at any point the top power MOSFET is on for roughly 8 consecutive clock cycles, the part will turn on the bottom power MOSFET for a brief duration such that the BOOST capacitor can be replenished.

Forced Continuous Mode Operation

Floating the MODE/SYNC pin defaults the LTC3649 into forced continuous mode operation. In this mode, the part switches continuously regardless of load current, and the inductor peak current is allowed to decrease to approximately –1A to allow for negative average current.

High Duty Cycle/Dropout Operation

As the input voltage decreases towards the desired output voltage, the duty cycle will increase towards 100%. However, given the architecture, there are two restrictions that prevent the LTC3649 from operating in full dropout mode.

The first restriction is due to how the ISET voltage is programmed. If a resistor is placed between ISET and GND to set the output voltage, the 50µA of current out of the ISET pin is only guaranteed to be accurate when V_{ISET} is more than 500mV below V_{IN}. As the input voltage drops below that 500mV threshold, the ISET current will decrease, thus limiting the programmed voltage. Typically, V_{ISET} will never get within 300mV of V_{IN}. Since V_{ISET} programs V_{OUT}, this limitation essentially enforces a maximum duty cycle for the switcher. This limitation can be overcome if an accurate external supply is used to drive the ISET pin directly.

The second limitation against full dropout operation is the requirement for the BOOST to SW capacitor to refresh. When the top power MOSFET is on for multiple clock cycles during dropout operation, the BOOST to SW capacitor slowly gets depleted by the internal circuitry of the chip. When the bottom switch does not turn on for at least 80ns for 8 periods, it is forced to turn on in order to guarantee sufficient voltage on the bootstrap capacitor. During a refresh, the bottom switch will only turn on for roughly 30% of the period to limit inductor ripple, thus limiting output voltage ripple.

Output Current Monitoring and Regulation

The LTC3649 has the ability to accurately sense the average inductor current without the use of an external sense resistor. The IMON pin output current is 1/40000th scale of the inductor current. Placing a resistor from IMON to GND allows the voltage on that node to be equal to:

$$V_{IMON} = \frac{R_{IMON} \bullet I_L}{40000}$$

Since the IMON current mirrors the inductor current, it is necessary to place a capacitor from IMON to GND to filter the voltage on the node. The choice of this capacitor is discussed below.

In addition to simply sensing the inductor current, the LTC3649 can also be programmed to regulate the average output current limit. The regulator will limit the peak inductor current if it senses that the voltage on IMON has exceeded 2V. As a result, the programmed average inductor current depends on the size of R_{IMON} such that:

$$I_{LAVG} = \frac{2V \bullet 40000}{R_{IMON}}$$

OPERATION

If current monitoring is needed but current limiting is not, simply pick an R_{IMON} resistor small enough such that V_{IMON} will never approach 2V. A 10k resistor along with a 10nF capacitor is typically a good RC pair to use in this case.

If current limiting is useful for the application, it is important to carefully pick the value of the capacitor from IMON to GND, C_{IMON}. If C_{IMON} is picked to be too large, then the switching regulator will be slow to react to a large output transients, and the average inductor current will rise above the programmed level until the loop can react. If C_{IMON} is picked to be too small, then the loop can become unstable. Typically, an RC time constant that is at least 10 times slower than the switching frequency is a good place to start.

$$C_{IMON} \bullet R_{IMON} \geq \frac{10}{2\pi \bullet f_{SW}} = \frac{1.59}{f_{SW}}$$

Cable Drop Compensation

In certain applications, the point of load will be separated from the switching regulator with a significant amount of wire resistance. Thus, the voltage at the point of load, V_{POL}, will be reduced from V_{OUT} near the regulator by the resistance of the trace/wire multiplied by the current. In those applications, it is useful to adjust for the V_{OUT} regulation point depending on the average output current to maintain an accurate V_{POL}.

The IMON feature of the LTC3649 along with its single resistor output voltage programmability allows this feature to be implemented with the following configuration shown in Figure 1.

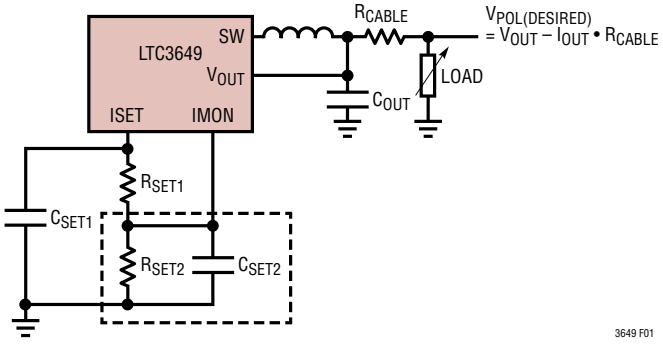


Figure 1. Cable Drop Compensation Application

The general idea behind this setup is that once the inductor current rises, the current out of the IMON pin will rise proportionally. As a result, the ISET voltage will increase, thus increasing the regulated output voltage. This rise of V_{OUT} offsets the voltage drop across the cable, R_{CABLE}, thus keeping V_{POL} constant.

R_{SET2} should be sized to account for the amount of cable resistance:

$$R_{SET2} = 40000 \bullet R_{CABLE}$$

Furthermore, in order to regulate V_{POL} at the desired voltage:

$$(R_{SET1} + R_{SET2}) \bullet 50\mu A = V_{POL(DESIRED)}$$

C_{SET1} is still required if soft-start is desired for the application, and C_{SET2} is required to filter out the AC ripple noise of the inductor current. Once again, typically C_{SET2} and R_{SET2} should be sized to have a RC time constant 10 times slower than the switching frequency.

Input Voltage Regulation

In certain applications, the input supply to the power regulator can exhibit fairly high output impedance. As a result, when the regulator is running at heavy loads, V_{IN} might droop more than desired. The input voltage regulation loop allows the application to be programmed to decrease the peak inductor current level, and consequently the input current draw, when it senses that the input voltage has dropped below a programmed threshold. This threshold is programmed by connecting a resistor divider from V_{IN} to GND with its intermediate node fed back to V_{INREG}. With this setup, if V_{VINREG} ever falls below 2V, the regulator will decrease the output current level in order to maintain a 2V level at the pin. If this feature is not required, tie the V_{INREG} pin to $INTV_{CC}$ to prevent this control loop from interfering with normal operation.

Another useful application for the input voltage regulation loop is for momentary hold up supplies. Suppose an input supply is suddenly removed from the application, V_{IN} will immediately start to drop until it reaches the programmed input voltage regulation point. When this happens and CCM operation is selected, the regulator will actually take charge from the output capacitor and boost charge back to

OPERATION

the input to hold the input voltage at the regulated point. The regulator will continue to perform this operation until the output capacitor has dissipated so much energy that it can no longer hold up the input voltage. This momentary input voltage holdup proves to be a handy tool for certain applications.

$INTV_{CC}$ Regulator

The LTC3649 has two onboard internal low dropout (LDO) regulators that power the drivers and internal bias circuitry. Regardless of which one is in operation, the $INTV_{CC}$ must be bypassed to GND with a minimum of 2.2µF ceramic capacitor. Good bypassing is necessary to supply the high transient current required by the power MOSFET gate drivers.

The first LDO is powered from V_{IN}, and the $INTV_{CC}$ voltage is regulated to 3.3V. The power dissipated across this LDO would thus equal to $(V_{IN} – 3.3) • I_{INTVCC}$. For a typical 1MHz application running in CCM, the current drawn from $INTV_{CC}$ by the chip is roughly 20mA. Thus, if the input voltage is high, the power loss and heat rise due to this LDO is significant.

To combat this issue, a separate LDO exists that is powered from $EXTV_{CC}$. As long as the input voltage is above 5V and the $EXTV_{CC}$ voltage is above 3.2V, this LDO will take over and regulate the $INTV_{CC}$ voltage to 3.1V. In applications where the output voltage is programmed to 3.3V or above, it is recommended that the V_{OUT} (<28V) pin be directly tied to the $EXTV_{CC}$ pin. Otherwise, if a separate lower voltage rail exists on board that can supply $INTV_{CC}$ current, then attaching that supply to $EXTV_{CC}$ will also suffice provided that a 1µF ceramic bypass capacitor is placed from the $EXTV_{CC}$ pin to GND physically close to the chip. Both examples should significantly reduce the power loss through the LDO.

V_{IN} Undervoltage Programming

LTC3649 offers an accurate RUN threshold to start the regulator. As a result, a resistor divider from IN to GND can be placed with the intermediate node fed back to RUN to set an accurate V_{IN} undervoltage threshold. As the input voltage rises, the RUN voltage will increase above the V_{RUN} rising threshold (1.2V), and the regulator will turn on. Similarly, once on, if the input voltage decreases below the V_{RUN} falling threshold (1.1V), the regulator will turn off.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3649 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 70V, the regulator suspends operation by shutting off both power MOSFETs and discharges the ISET pin voltage to ground. Once V_{IN} drops below the V_{OVLO} threshold, the regulator resumes normal switching operation.

Programming Switching Frequency

Connecting a resistor from the R_T pin to GND programs the switching frequency from 300kHz to 3MHz according to the following formula:

$$f\,(kHz) = \frac{10^5}{R_T(k\Omega)}$$

Do not float the R_T pin.

The internal phase-locked loop has a synchronization range of ±50% around its programmed frequency. Therefore, during external clock synchronization, the proper R_T value should be selected such that the external clock frequency is within this 50% range of the R_T programmed frequency.

Output Voltage Tracking and Soft-Start

The LTC3649 allows the user to program its output voltage ramp rate by means of the ISET pin. Since V_{OUT} servos its voltage to that of V_{ISET}, placing an external capacitor C_{SET} from the ISET pin to GND will program the ramp-up rate of the ISET pin and thus the V_{OUT} voltage.

$$V_{OUT}(t) = I_{ISET} • R_{SET} \left[1 - e^{\frac{1}{R_{SET} • C_{SET}} t}\right]$$

From 0% to 90% V_{OUT}:

$$t_{SS} \cong -R_{SET} • C_{SET} • \ln(1 - 0.9)$$

$$t_{SS} \cong 2.3 • R_{SET} • C_{SET}$$

OPERATION

The soft-start time t_{SS} (from 0% to 90% of V_{OUT}) is 2.3 times the time constant (R_{SET}•C_{SET}). The ISET pin can also be driven by an external supply capable of sinking 50µA.

When starting up into a pre-biased V_{OUT}, the LTC3649 will stay in Burst Mode operation and keep the power switches off until the voltage on ISET has ramped up to be equal to V_{OUT}, at which point the switcher will begin switching and V_{OUT} will ramp up with ISET.

Output Power Good

When the LTC3649's output voltage is within the 7.5% window of the regulation point, which is divided down as a V_{PGDFB} voltage in the range of 0.555V to 0.645V, the output voltage is in regulation and the PGOOD pin is pulled high with an external resistor connected to $INTV_{CC}$ or another voltage rail. Otherwise, an internal open-drain pull-down device will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3649's PGOOD falling edge includes a blanking delay of approximately 64 clock cycles.

Internal/External ITH Compensation

For ease of use, the user can simplify the loop compensation by tying the ITH pin to $INTV_{CC}$ to enable internal compensation. Because the internal compensation is required to provide a stable output voltage for a wide range of switching frequencies, it is designed to have a loop response that is typically much slower than optimal. This thus becomes a trade-off between simplicity and OPTI-LOOP® optimization, where ITH components are external and are selected to optimize the loop transient response with minimum output capacitance.

Minimum On-Time Considerations

Due to the architecture of the LTC3649, a minimum on-time restriction is imposed such that the top power MOSFET can have enough time to turn on and accurately determine if it has reached its peak current level before shutting off. The typical minimum on-time of the regulator is 60ns. Thus, given an application with varying input and output voltage ranges, the frequency must be designed to be slow enough to ensure the minimum on-time restriction is not violated.

$$\text{Freq (kHz)} \leq \frac{V_{OUT(MIN)}}{60 \bullet 10^{-6} \bullet V_{IN(MAX)}}$$

In the rare cases where the minimum on-time restriction is violated, the frequency of the LTC3649 will automatically and gradually fold back down to one-fifth of its programmed switching frequency to allow the output to remain in regulation. This feature is designed for applications where the input voltage only experiences momentary spikes in voltage. In such applications, the frequency does not have to be programmed so slow to account for those momentary spikes, thus significantly saving component size and cost.

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Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large input voltage droops from occurring, a low effective series resistance (ESR) input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the ESR that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When only a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, use X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} = 3 \frac{\Delta I_{OUT}}{f \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is

APPLICATIONS INFORMATION

very low. A 10µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as physically close to the V_{IN} pin as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Lower ripple current reduces core losses in the inductor and reduces output voltage ripple. However, at extremes, low ripple causes inductor current sensing issues. Highest efficiency operation is obtained at low frequency with reasonably small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple current does not exceed specified inductor saturation current ratings, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Table 1. Inductor Selection Table

INDUCTOR	INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)	MANUFACTURER
XAL8080 Series	4.7	8.89	17.4	8.6 × 8.1	8.0	Coilcraft www.coilcraft.com
	6.8	13.20	14.0	8.6 × 8.1	8.0	
	10.0	21.00	10.9	8.6 × 8.1	8.0	
XAL1010 Series	3.3	3.70	27.4	11.3 × 10	10.0	
	4.7	5.20	25.4	11.3 × 10	10.0	
	5.6	6.30	23.6	11.3 × 10	10.0	
	6.8	8.10	21.8	11.3 × 10	10.0	
	8.2	11.70	18.3	11.3 × 10	10.0	
	10.0	13.40	17.5	11.3 × 10	10.0	
FDV0840 Series	2.1	10.40	10.6	9.1 × 8.4	4.0	Toko www.toko.com
	3.9	18.80	8.4	9.1 × 8.4	4.0	
	4.9	24.60	6.9	9.1 × 8.4	4.0	
	6.9	31.70	6.1	9.1 × 8.4	4.0	
IHLP-4040DZ-A1 Series	2.2	8.20	25.6	11.5 × 10.3	4.0	Vishay www.vishay.com
	3.3	13.70	18.6	11.5 × 10.3	4.0	
	4.7	15.00	17.0	11.5 × 10.3	4.0	
	5.6	17.60	16.0	11.5 × 10.3	4.0	
	6.8	21.20	13.5	11.5 × 10.3	4.0	
	10.0	33.20	12.0	11.5 × 10.3	4.0	
WE-HCI 1050 Series	2.4	3.50	17.0	10.6 × 10.6	5.0	Wurth Elektronik www.we-online.com
	3.3	5.90	15.0	10.6 × 10.6	5.0	
	4.2	7.10	14.0	10.6 × 10.6	5.0	
	5.5	10.30	12.0	10.6 × 10.6	5.0	
	6.5	12.50	10.0	10.6 × 10.6	5.0	
	7.8	13.60	9.5	10.6 × 10.6	5.0	
	10.0	16.30	8.5	10.6 × 10.6	5.0	

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Once the value for L is known, the type of inductor must be selected. Core loss is very dependent on the material, frequency and inductance selected. Higher inductance reduces ripple. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite materials have very low core losses and are preferred at high switching frequencies, so design goals can minimize copper loss and preventing saturation. However, ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK and Wurth Elektronik. Refer to Table 1 for more details.

Checking Transient Response

The OPTI-LOOP external compensation allows the transient response to be optimized for a wide range of loads and output capacitors via the ITH pin. This allows for optimization of the control loop behavior and provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects these closed-loop responses. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external component network shown in the Figure 2 circuit will provide an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested value) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

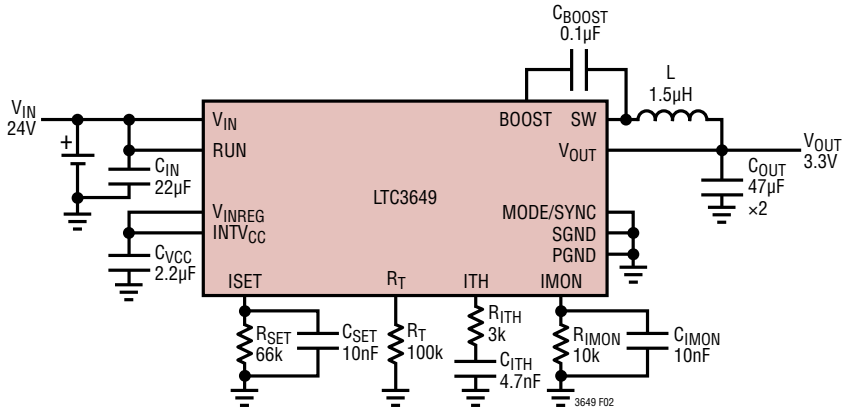

Figure 2. 24V to 3.3V, 1MHz Buck Regulator with Output Current Monitoring

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The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in most critical frequency ranges of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-start operation.

Input Disconnect/Input Short Considerations

If at any point the input supply is removed with the output voltage still held high through its capacitor, power will be drawn from the output capacitor to power the chip, until the output voltage drops below the minimum V_{IN} requirements of the chip.

However, if the V_{IN} pin is grounded while the output is held high, regardless of the RUN state, parasitic body diodes inside the LTC3649 will pull current from the output through the SW pin. Depending on the size of the output capacitor and the resistivity of the short, high currents may flow through the internal body diode, and cause damage to the part. If a V_{IN} discharge is possible, preventative measures should be taken to prevent current flow through the internal body diode. Simple solutions would be placing a Schottky diode in series with the supply (Figure 3), or placing a Schottky diode from V_{OUT} to V_{IN} (Figure 4).

Output Short Considerations

In an event where the output of the LTC3649 is shorted to GND through a low resistance, high inductance trace/wire, it is likely for the output voltage to momentarily drop below GND. In a typical application where the output is tied directly to the V_{OUT} pin, it would violate the ABSMAX specification of the pin and potentially cause damage to the IC. To prevent damage in this case, connect a 100Ω resistor between the output and the V_{OUT} pin.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual power losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (P1 + P2 + P3 + \ldots)$$

where P1, P2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3649 circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

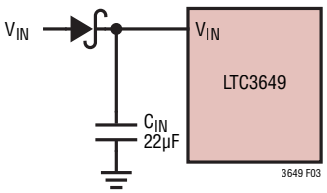


Figure 3. Schottky Diode in Series with the Supply

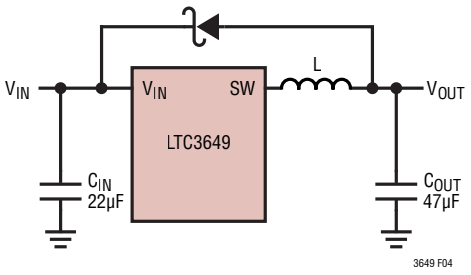


Figure 4. Schottky Diode from V_{OUT} to V_{IN}

APPLICATIONS INFORMATION

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(D) + (R_{DS(ON)BOT})(1 - D)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}{}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from IN to ground. The resulting dQ/dt is a current out of IN that is typically much larger than the DC control bias current. In continuous mode:

   $$I_{GATECHG} = f(Q_T + Q_B)$$

   where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

   $$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN}$$

   The gate charge loss is a function of current through the $INTV_{CC}$ pin as well as frequency. Thus, their effects will be more pronounced in application with high LDO supply voltages (either $EXTV_{CC}$ or V_{IN}) and higher frequencies.

3. Other "hidden" losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3649 internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Thermal Conditions

In a majority of applications, the LTC3649 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN and FE packages. However, in applications where the LTC3649 is running at high ambient temperature, high V_{IN}, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 180°C, both power switches will be turned off until the temperature drops by 15°C.

To avoid the LTC3649 from exceeding the maximum junction temperature, some thermal analysis must be done. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

As an example, consider the case when the LTC3649 is used in applications where V_{IN} = 24V, I_{OUT} = 4A, f = 1MHz, and V_{OUT} = 3.3V. The equivalent power MOSFET resistance R_{SW} is:

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{V_{OUT}}{V_{IN}} + R_{DS(ON)BOT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 110m\Omega \bullet \frac{3.3V}{24V} + 50m\Omega \bullet \left(1 - \frac{3.3V}{24V}\right)$$

$$= 58.25m\Omega$$

In the case where the $EXTV_{CC}$ pin is connected to the OUT pin, the V_{IN} current will be minimal as most of the current used to bias up internal circuitry and gate drive will come directly from $EXTV_{CC}$. Typically for a 1MHz application, the current drawn from $EXTV_{CC}$ will be 20mA.

Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}{}^2 \bullet R_{SW} + V_{EXTVCC} \bullet I_{EXTVCC}$$

$$= 16A^2 \bullet 58.25m\Omega + 3.3V \bullet 20mA$$

$$= 998mW$$

APPLICATIONS INFORMATION

The FE28 package junction-to-ambient thermal resistance, θ_{JA}, is around 30°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 0.998W \bullet 30°C/W + 25°C = 54.94°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 10% at 54.94°C yields a new junction temperature of 60°C. If the application calls for a higher ambient temperature and/or higher switching frequency, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

If $EXTV_{CC}$ is not connected to V_{OUT}, the IC current will come from V_{IN}. In this case, the total power dissipation will be:

$$P_D = 16A^2 \bullet 58.25m\Omega + 24V \bullet 20mA = 1.41W$$

This will result in an extra 400mW of power dissipation.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3649 (refer to Figure 5). Check the following in your layout:

1. Do the capacitors C_{IN} connect to the V_{IN} and GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Solder the exposed pad (Pin 29) on the bottom of the package to the GND plane. Connect this GND plane to other layers with thermal vias to help dissipate heat from the LTC3649.
4. The ground terminal of the ISET resistor must be connected to the other quiet signal GND and together connected to the power GND on only one point. The ISET resistor should be placed and routed away from noisy components and traces, such as the SW line, and its trace should be minimized

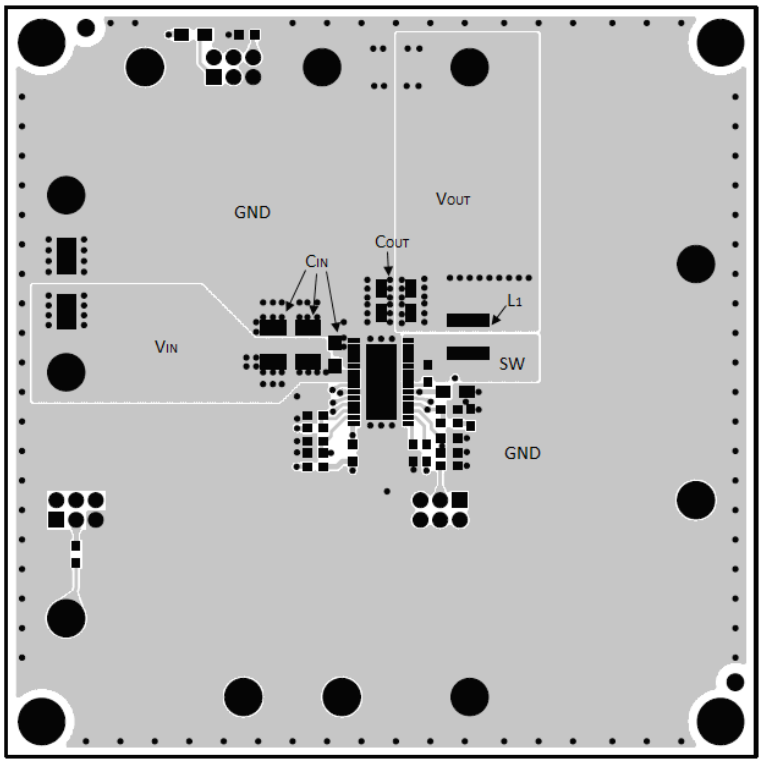


Figure 5. Sample PCB Layout

APPLICATIONS INFORMATION

5. Keep sensitive components away from the SW pin. The ISET resistor, R_T resistor, the compensation components C_{ITH} and R_{ITH}, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.
6. A ground plane is preferred.
7. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

Design Example

As a design example, consider the LTC3649 in an application with the following specifications:

V_{IN} = 24V to 36V

V_{OUT} = 5V

$I_{OUT(MAX)}$ = 4A

$I_{OUT(MIN)}$ = 500mA

f_{SW} = 1MHz

First, the R_{SET} is selected based on:

$$R_{SET} = \frac{V_{OUT}}{50\mu A} = \frac{5V}{50\mu A} = 100k\Omega$$

For best accuracy, 0.5% 100k resistor is selected.

For a typical soft-start time of 2ms (0% to 90% of final V_{OUT} value), the C_{SET} should be:

$2ms = 2.3 \bullet R_{SET} \bullet C_{SET}$

$\Rightarrow C_{SET} = 8.7nF$

A typical 10nF capacitor can be used for C_{SET}.

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized. Select from the characteristic curves the correct R_T resistor for the 1MHz switching frequency. Based on that, R_T should be 100k. Then calculate the inductor value to achieve a current ripple that is about 40% of the maximum load current at maximum V_{IN}:

$$L = \left(\frac{5V}{1MHz \bullet 1.6A}\right)\left(1 - \frac{5V}{36V}\right) = 2.7\mu H$$

C_{OUT} will be selected based on the ESR that is required to satisfy the output ripple requirement and the bulk capacitance needed for loop stability. For this design, two 47µF ceramic capacitors will be used.

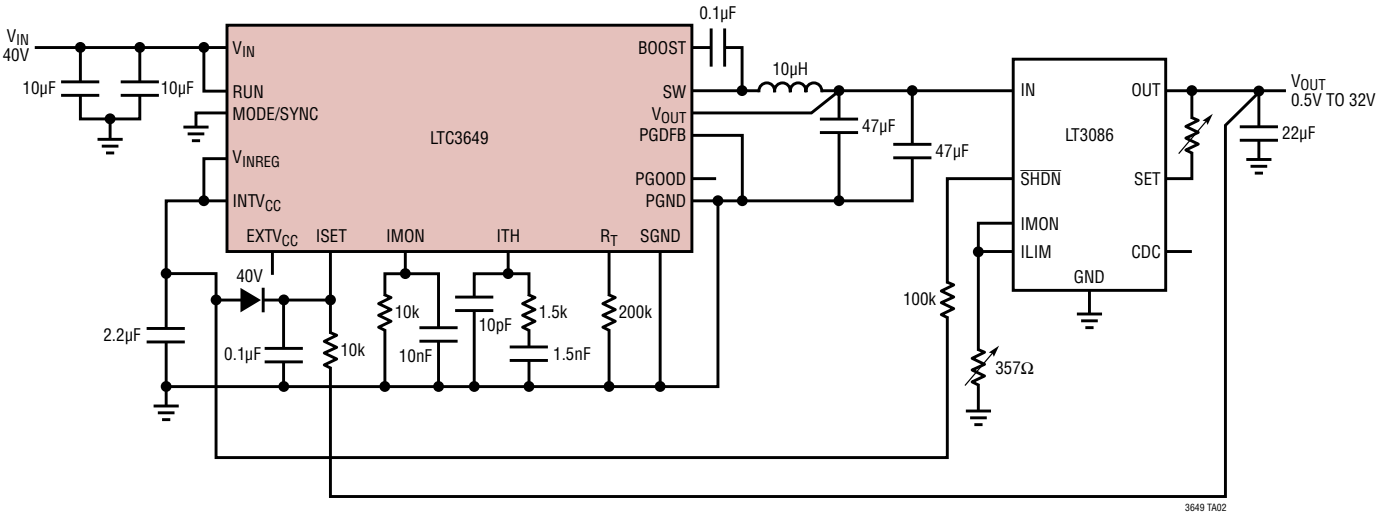
C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 4A\left(\frac{5V}{36V}\right)\left(\frac{36V}{5V} - 1\right)^{1/2} = 1.38A$$

Decoupling the V_{IN} pin with one 22µF ceramic capacitor is adequate for most applications.

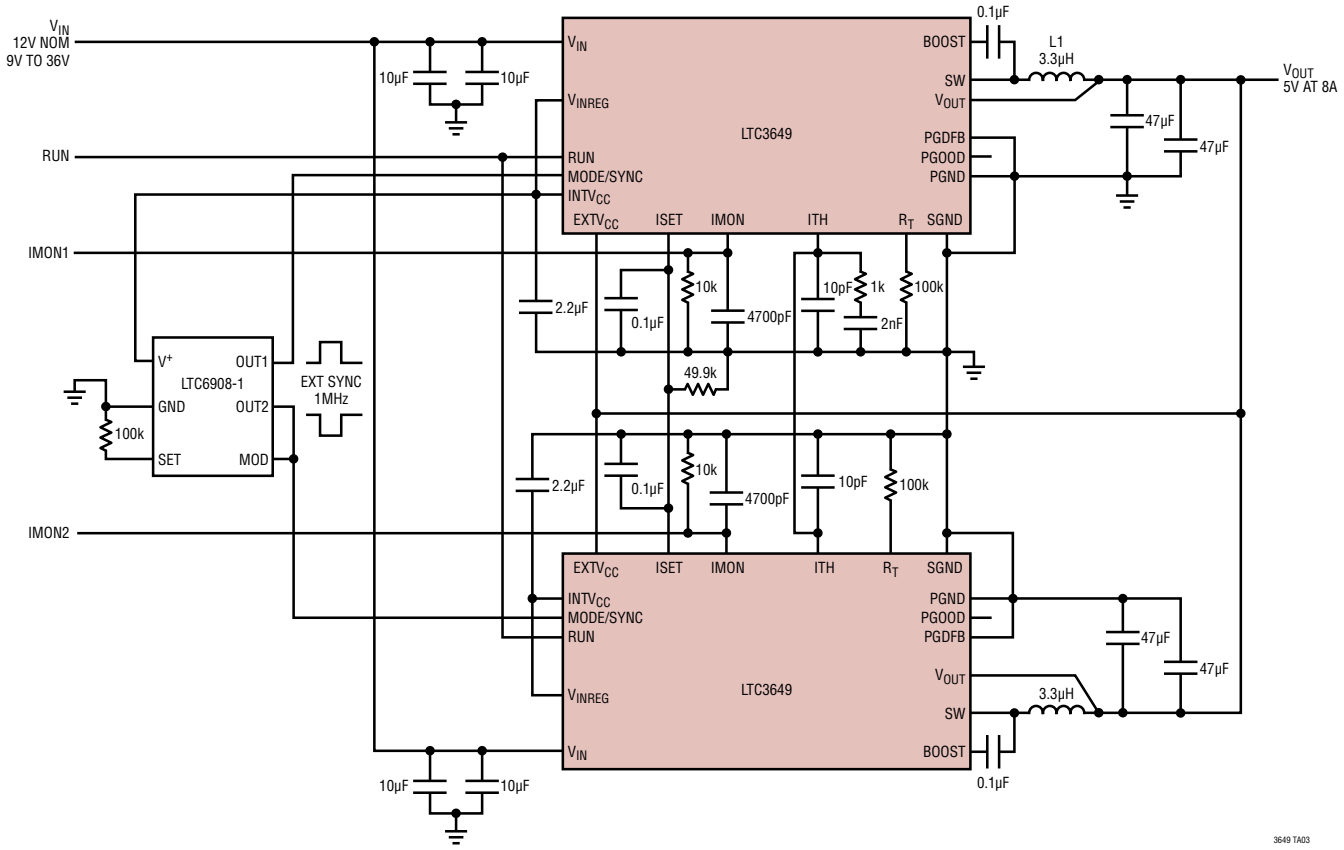
TYPICAL APPLICATIONS

0.5V to 32V, 2.1A Low-Noise High Efficiency Lab Supply



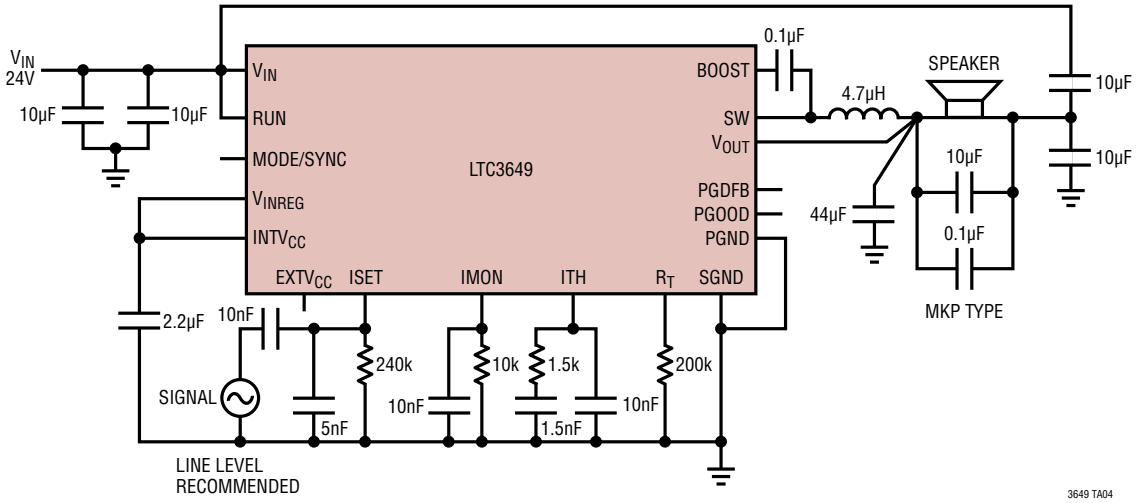
TYPICAL APPLICATIONS

Dual Phase Operation

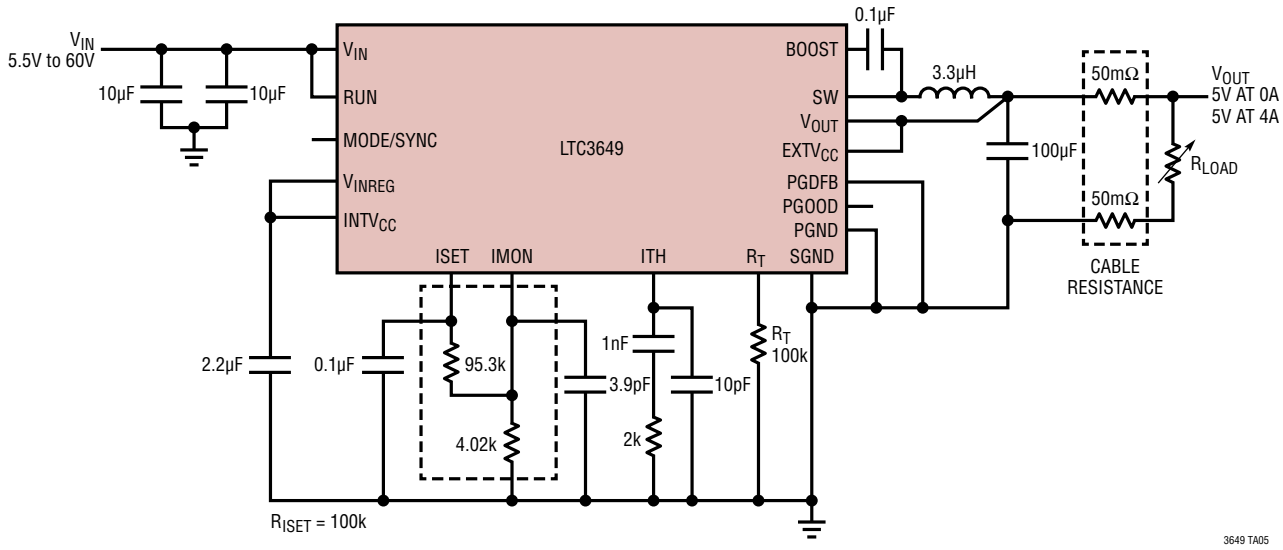


TYPICAL APPLICATIONS

Wide Input Signal Range Audio Driver



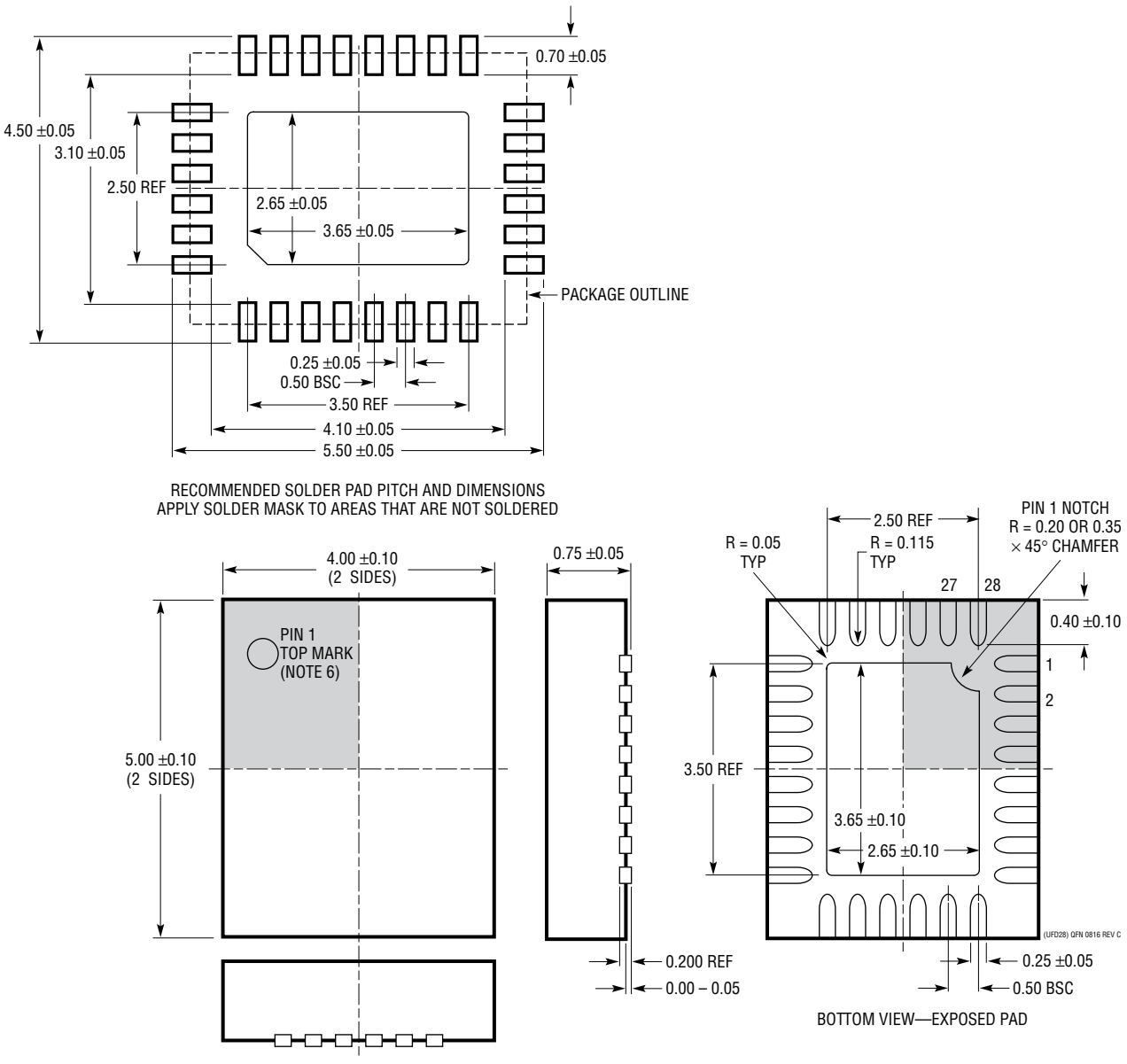
Cable Drop Compensation



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3649#packaging for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev C)

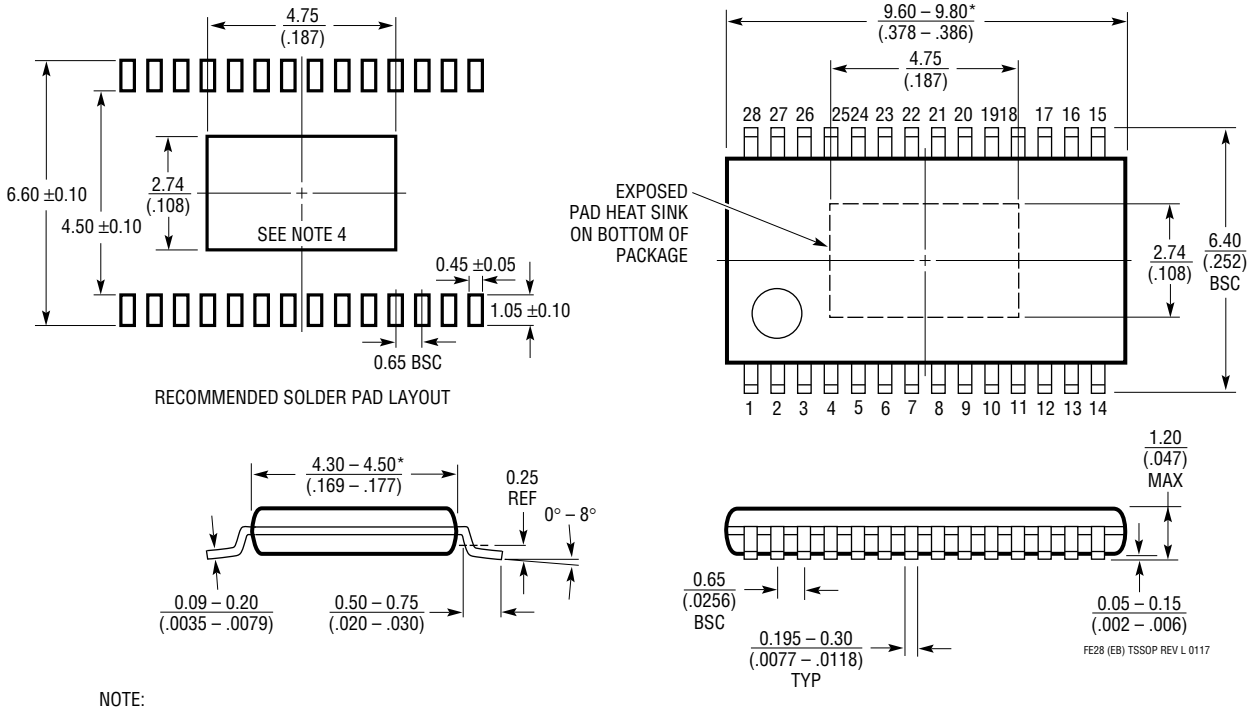


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGHD-3).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3649#packaging for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev L)
Exposed Pad Variation EB



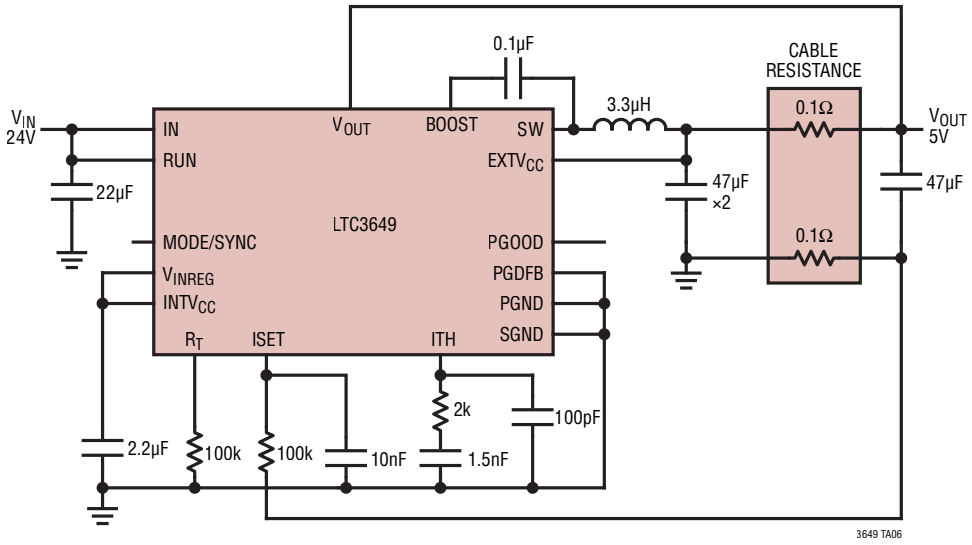
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/16	Clarified shutdown current to 18µA Clarified IMON conditions Clarified Programming Switching Frequency section	1 3 11
B	05/17	Clarified $INTV_{CC}$ capacitor on Typical Applications	21, 22

TYPICAL APPLICATION

5V$_{OUT}$ with Remote Sensing



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3600	15V, 1.5A Synchronous Rail-to-Rail Single Resistor Step-Down Regulator	$V_{IN(MIN)}$ = 4V, $V_{IN(MAX)}$ = 15V, $V_{OUT(MIN)}$ = 0V, MSOP-12, 3mm × 3mm DFN-12
LTC3892/ LTC3892-1	60V, Low I_Q, Dual 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4.5V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, I_Q = 29µA
LTC3891	60V, Low I_Q, Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	PLL Fixed Frequency 50kHz to 900kHz, 4V ≤ V_{IN} ≤ 60V, 0.8V ≤ V_{OUT} ≤ 24V, I_Q = 50µA
LT®8620	65V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E 3mm × 5mm QFN-24
LT8641	65V, 4A, 96% Efficiency, 3MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 3mm × 4mm QFN-18
LT8610A/ LT8610AB	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8610AC	42V, 3.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-16E
LT8611	42V, 2.5A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA and Input/Output Current Limit/Monitor	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, 3mm × 5mm QFN-24
LT8612	42V, 6A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 3.0µA, I_{SD} <1µA, 3mm × 6mm QFN-28
LT8614	42V, 4A, 96% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} <1µA, 3mm × 4mm QFN-18
LT8616	42V, Dual 2.5A + 1.5A, 95% Efficiency, 2.2MHz Synchronous Micropower Step-Down DC/DC Converter with I_Q = 5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 5µA, I_{SD} <1µA, TSSOP-28E, 3mm × 6mm QFN-28

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