TPSM846C23 4.5-V to 15-V Input, 0.35-V to 2-V Output, 35-A PMBus™ Power Module

1 Features

- Complete Integrated PMBus™ Power Solution
- Pin Compatible With TPSM846C24 (non-PMBus)
- Stackable up to 70 A With Current Sharing
- Output Voltage Range 0.35 V to 2 V
- Output Voltage Accuracy as Tight as 0.5%
- 15 mm × 16 mm Footprint (6.4 Max Height)
- 300-kHz to 1-MHz Switching Frequency
- Synchronization to an External Clock
- Differential Remote Sense
- Power-Good Output
- Prebias Output Monotonic Start-Up
- PMBus Telemetry: Current, Voltage, Temperature
- Programmable Protection and Fault Response
- Programmable UVLO, Soft Start/Stop, Delays
- Operating IC Junction Range: –40°C to +125°C
- Operating Ambient Range: –40°C to +105°C
- Enhanced Thermal Performance: 8.7°C/W
- Meets EN55022 Class A Emissions
- Create a Custom Design Using the TPSM846C23 With the WEBENCH® Power Designer

2 Applications

- Compact PCI / PCI Express / PXI Express
- Broadband and Communications Infrastructure
- Automated Test and Medical Equipment
- DSP and FPGA Point-of-Load Applications

3 Description

The TPSM846C23 is a 35-A fixed-frequency, PMBus-compliant, step-down power module, with PMBus commands that allow for the configuration, control, and monitoring of key power regulator functions. The module incorporates the controller, power MOSFETs, inductor, and associated components into a rugged, thermally enhanced, surface-mount package. The user supplies the input and output capacitors along with a few other passive components to set the operating parameters of the module. Two modules can be configured to work in parallel to provide up to a 70-A, two-phase power solution.

The PMBus interface provides for converter configuration of output voltage, UVLO, soft start, soft stop, overcurrent, and thermal shutdown parameters. The interface also provides support for telemetry that can report the actual output voltage, output current, and device temperature. Standard PMBus *warning* and *fault* functions are also supported. The device supports PMBus communication speeds up to 400 kHz and supports a subset of the commands in the PMBus 1.3 specification.

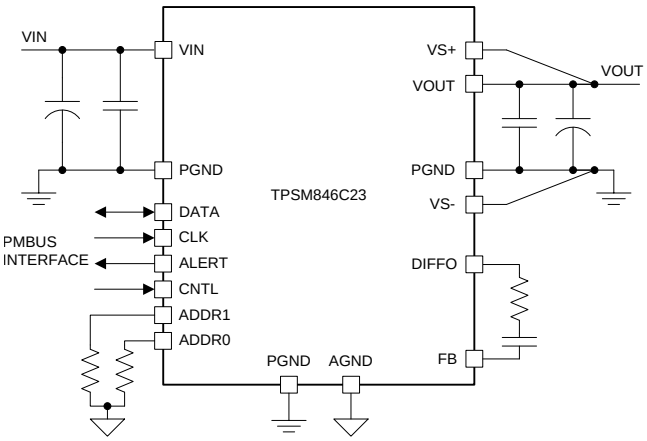
The 15-mm × 16-mm component footprint is easy to solder onto a printed circuit board and allows a compact, point-of-load design.

Device Information(1)

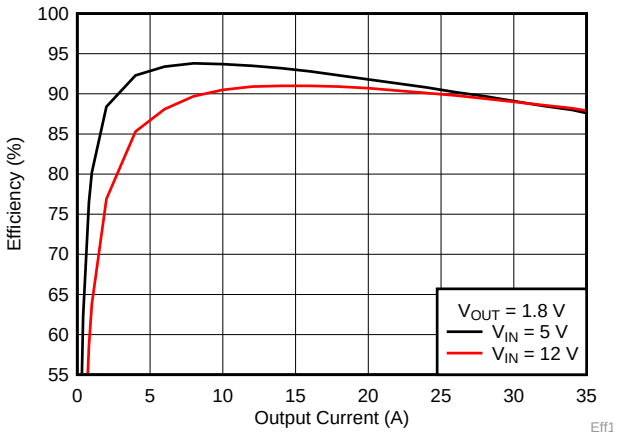
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPSM846C23	MOL (59)	15.00 mm × 16.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2018) to Revision F — **Page**

- Changed HBM ESD from 500 V to 1000 V ... 6

Changes from Revision D (January 2018) to Revision E — **Page**

- Updated PCB Top-side Layout Recommendation figure ... 78

Changes from Revision C (August 2017) to Revision D — **Page**

- first release of production-data data sheet ... 1

Changes from Revision B (March 2017) to Revision C — **Page**

- Datasheet marked as Advanced Information - prototype samples available ... 1
- Changed the maximum height of the device to 6.4 mm ... 1
- Added link to the parallel EVM and user's guide ... 28
- Added the EMI section ... 80

Changes from Revision A (March 2017) to Revision B — **Page**

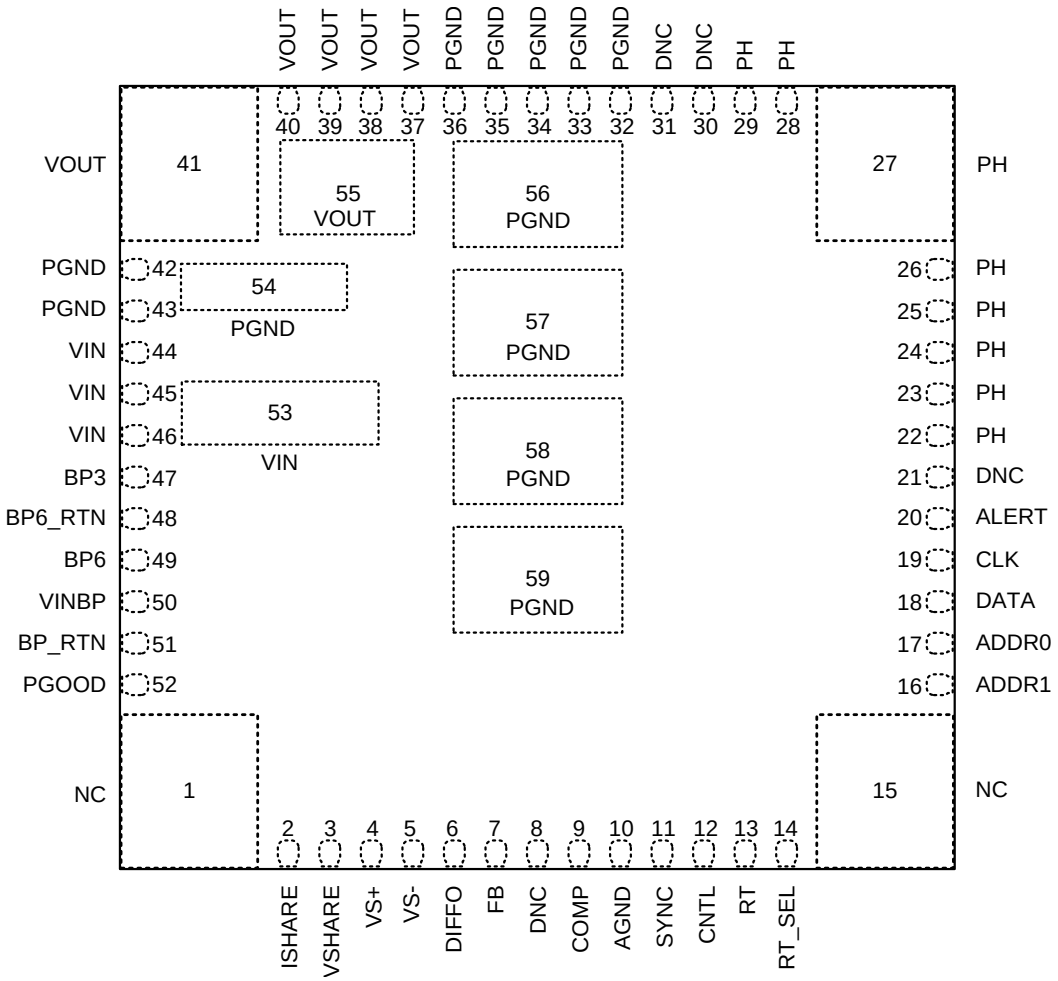
- Added the height of the device in Features ... 1

Changes from Original (March 2017) to Revision A **Page**

- Corrected 3 pin names on the Figure 19 73

5 Pin Configuration and Functions

MOL Package
59-Pin BQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR0	17	I	Connect a resistor from this pin to AGND to set the low-order 3 bits of the desired PMBus address. Do not leave this pin floating. See *PMBus Address*.
ADDR1	16	I	Connect a resistor from this pin to AGND to set the high-order 3 bits of the desired PMBus address. Do not leave this pin floating. See *PMBus Address*.
AGND	10	G	Analog ground for the controller circuitry. This pin is internally connected to PGND.
ALERT	20	O	PMBus ALERT pin. See PMBus specification.
BP_RTN	51	G	Return path for VINBP and BP3. This pin is internally connected to PGND, pad 59.
BP3	47	O	Output of the internal 3.3-V regulator. Bypass this pin with a minimum of 2.2-µF to BP_RTN. Can be used as a pullup termination voltage for PGOOD and PMBus signals.
BP6	49	O	Output of the internal 6.5-V regulator that powers the driver stage of the device. Bypass this pin with a minimum of 2.2-µF to BP6_RTN.
BP6_RTN	48	G	Power ground return path for BP6 bypass capacitor.
CLK	19	I	PMBus CLK pin. See PMBus specification.
CNTL	12	I	PMBus CNTL pin. See PMBus specification.
COMP	9	O	Output of the error amplifier.
DATA	18	I/O	PMBus DATA pin. See PMBus specification.
DIFFO	6	O	Output of the remote sense differential amplifier. This provides remote sensing for output voltage reporting and the voltage control loop.
DNC	8, 21, 30, 31	–	Do Not Connect. Do not connect these pins to AGND, PGND, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
FB	7	I	Feedback pin for the control loop.
ISHARE	2	I	Current sharing signal for parallel operation.
NC	1, 15	–	Not Connected. These pins are internally isolated from any signal and all other pins. Each pin must be soldered to a pad on the PCB. These pins can be left isolated or connected to AGND or PGND.
PGND	32, 33, 34, 35, 36,42, 43, 54, 56, 57, 58, 59	G	Power ground of the device. This is the return current path for the power stage of the device. Connect these pins to the bypass capacitors associated with VIN and VOUT. Connect pads 56, 57, 58, and 59 to the PCB ground planes using multiple vias for optimal thermal performance. All pins should be connected together externally with a copper plane or pour directly under the device.
PGOOD	52	O	Power good indicator. This pin is an open-drain output and will assert low during any fault/warn conditions. See Power Good Indicator section for details. Requires a pullup resistor.
PH	22, 23, 24, 25, 26, 27, 28, 29	O	Phase switch node. Do not connect any external components to these pins or tie them to a pin of another function.
RT	13	I	Frequency-setting resistor. To operate the device at its default switching frequency, do not connect to this pin. To operate at a different switching frequency, connect a resistor from this pin to AGND.
RT_SEL	14	I	RT resistor select. To operate the device at its default switching frequency, connect this pin to AGND. To operate at a different switching frequency, let this pin float.
SYNC	11	I/O	Frequency synchronization pin. In a stand-alone application or as the Master device in a parallel configuration, the SYNC pin is configured as a SYNC-IN pin and power conversion is synchronized to the rising edge of a 50% duty cycle external clock applied to this pin. For a Slave device in a parallel configuration, power conversion is synchronized to the falling edge of the incoming clock.
VIN	44, 45, 46, 53	I	Input switching voltage pins. These pins supply voltage to the power switches of the converter.
VINBP	50	I	Input power to the controller circuitry. Bypass this pin with a minimum of 1 µF to BP_RTN. This pin is internally connected to VIN.
VOUT	37, 38, 39, 40, 41, 55	O	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external bypass capacitors between these pins and PGND.
VS+	4	I	Positive input of the remote amplifier. Connect this pin to VOUT at the load for best voltage regulation. Do not let this pin float.
VS–	5	I	Negative input of the remote amplifier. Connect this pin to ground at the load for best voltage regulation. Do not let this pin float.
VSHARE	3	I/O	Voltage sharing signal for parallel operation.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input voltage	VIN	–0.3	18	V
	VIN < 2-ms transient		19	
	VIN–PH (VIN TO PH differentially)	–0.3	25	
	ADDR0, ADDR1, FB	–0.3	3.6	
	CLK, DATA	–0.3	5.5	
	VS+, VS–, RT, CNTL, SYNC, PGOOD, ISHARE, RT_SEL	–0.3	7	
	BP6_RTN, BP_RTN, AGND	–0.3	0.3	
Output voltage	PH	–1	25	V
	PH < 100-ns transient	–5	25	
	BP6, COMP, DIFFO, VSHARE	–0.3	7	
	ALERT	–0.3	5.5	
	BP3	–0.3	3.6	
Operating IC junction temperature, T_J		–40	125	°C
Operating ambient temperature, T_A		–40	105	
Storage temperature, T_{stg}		–55	150	°C
Mechanical shock			500	G
Mechanical vibration			10	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Input voltage	VIN	4.5	12	15	V
	SYNC		3.3	6.5	
	PGOOD pull-up voltage		3.3	5.5	
Output voltage	V_{OUT}	0.35		2.0	V
Output current	I_{OUT}	0		35	A
Frequency		300	500	1000	kHz
Temperature	Operating ambient temperature	–40		105	°C
	Operating IC junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPSM846C23 MOL (QFN) 59 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter[3]	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter[4]	4.3	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 100 mm × 100 mm, 6-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Over –40°C to 105°C free-air temperature range, V_{IN} = 12 V, V_{OUT} = 1.2 V, $I_{OUT} = I_{OUT(max)}$, f_{SW} = 500 kHz, C_{IN1} = 4 × 22 µF, 25 V, 1210 ceramic, C_{IN2} = 2 × 330 µF electrolytic bulk, C_{OUT1} = 4 × 47 µF, 6.3 V, 1210 ceramic, C_{OUT2} = 2 × 470 µF, 6.3-V polymer bulk (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage	Over I_{OUT} range	4.5		15	V
I_{VIN}	Input operating current	Non-switching supply current		7.7	12	mA
OUTPUT VOLTAGE (V_{OUT})						
V_{OUT}	Factory default setting	R_{SET} = Not loaded, VOUT_SCALE_LOOP = 1		500		mV
		R_{SET} = 10 kΩ, 1%, VOUT_SCALE_LOOP = 0.5		1		V
	VOUT programmable range[1][2]	R_{SET} = Not loaded, VOUT_SCALE_LOOP = 1.0	0.35		1.65	V
		R_{SET} = 10 kΩ, 1%, VOUT_SCALE_LOOP = 0.5	0.7		2[3]	V
	VOUT programmable step size	R_{SET} = Not loaded, VOUT_SCALE_LOOP = 1		1.953		mV
		R_{SET} = 10 kΩ, 1%, VOUT_SCALE_LOOP = 0.5		3.906		mV
	Setpoint voltage tolerance	R_{SET} = Not loaded, T_J = 25°C, I_{OUT} = 0 A	–1%		1%	
		R_{SET} = 10 kΩ, 1%, T_J = 25°C, I_{OUT} = 0 A[4]	–1.5%		1.5%	
	Temperature variation	0°C < T_J < 85°C, I_{OUT} = 0 A[2]	–0.5%		0.5%	
		–40°C < T_J < 125°C, I_{OUT} = 0 A[2]	–1%		1%	
	Line regulation	4.5 V < V_{IN} < 15 V, I_{OUT} = 0 A		±0.05%		
	Load regulation	Over I_{OUT} range, using remote sense		±0.2%		
	Output voltage ripple	20-MHz bandwidth		13		mV
OUTPUT CURRENT						
I_{OUT}	Output current	Natural Convection. See SOA graph for derating.	0		35	A
I_{OCF}	Overcurrent fault threshold	Factory default setting		42		A
		Programmable range	5		52	
I_{OCWF}	Overcurrent warning threshold	Factory default setting		37		A
		Programmable range	4		50	
$I_{OCF(acc)}$	Overcurrent fault accuracy	I_{OUT} ≥ 20 A	–15%		15%	
$I_{SH(acc)}$	Output current share accuracy	(I_{OUT1} – I_{OUT2}) ÷ I_{TOTAL}, I_{OUT} ≥ 20 A per module[5]	–15%		15%	
		(I_{OUTx} – I_{TOTAL}) ÷ 2, I_{OUT} < 20 A per module[5]	–3%		3%	

(1) Output voltage is set by the VOUT_COMMAND PMBus command.
(2) Specified by design. Not production tested.
(3) While the PMBus permits setting the output voltage higher than 2 V, this product is not designed to be operated beyond this limit.
(4) The stated limit of the set-point tolerance includes the tolernace of both the internal voltage reference and the internal adjustment resistor. The overall output voltage tolerance will be affected by the tolerance of the external R_{SET} resistor.
(5) Specified by correlation. Not production tested.

Electrical Characteristics (continued)

Over –40°C to 105°C free-air temperature range, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = $I_{OUT(max)}$, f_{SW} = 500 kHz, C_{IN1} = 4 × 22 µF, 25 V, 1210 ceramic, C_{IN2} = 2 × 330 µF electrolytic bulk, C_{OUT1} = 4 × 47 µF, 6.3 V, 1210 ceramic, C_{OUT2} = 2 × 470 µF, 6.3-V polymer bulk (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER GOOD (PGOOD) AND OVERVOLTAGE / UNDERVOLTAGE THRESHOLD							
$V_{PG(OL)}$	PGOOD output low voltage	V_{IN} = 4 V, V_{OUT} = 0 V, I_{PGOOD} = 5 mA				0.3	V
		V_{IN} = 0 V, I_{PGOOD} = 80 µA				0.8	
$V_{PG(rise)}$	PGOOD threshold V_{OUT} rising	V_{OUT} setting = 1.2 V			95		%V_O
$V_{PG(fall)}$	PGOOD threshold V_{OUT} falling				105		%V_O
V_{OVWARN}	Overvoltage warning threshold				112		%V_O
$V_{OVFAULT}$	Overvoltage fault threshold				117		%V_O
V_{UVWARN}	Undervoltage warning threshold				88		%V_O
$V_{UVFAULT}$	Undervoltage fault threshold				83		%V_O
PERFORMANCE							
Efficiency (6)		V_{IN} = 12 V, I_{OUT} = 25 A	V_{OUT} = 0.8 V		83%		
			V_{OUT} = 1.2 V		87%		
			V_{OUT} = 1.8 V		90%		
		V_{IN} = 5 V, I_{OUT} = 25 A	V_{OUT} = 0.8 V		84%		
			V_{OUT} = 1.2 V		88%		
			V_{OUT} = 1.8 V		91%		
Transient response (6)		10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, C_{OUT} = 1000 µF, RC = 1 kΩ, CC = 1 nF	V_{OUT} over/undershoot		60		mV
			Recovery time		60		µs
		10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, C_{OUT} = 2000 µF, RC = 665 Ω, CC = 1.5 nF	V_{OUT} over/undershoot		40		mV
			Recovery time		60		µs
		10 A / µs load step from 25% to 75% of $I_{OUT(max)}$, C_{OUT} = 4000 µF, RC = 499 Ω, CC = 2.2 nF	V_{OUT} over/undershoot		27		mV
			Recovery time		60		µs
INTERNAL LOAD (BP6, BP3)							
V_{BP6}	BP6 regulator output voltage	7.5V ≤ V_{IN} ≤ 15 V, switching		5.85	6.4	6.95	V
$V_{BP6(DO)}$	Dropout voltage	(V_{VIN} – V_{BP6}), V_{IN} = 4.5 V, switching				400	mV
V_{BP3}	BP3 regulator output voltage	V_{IN} ≥ 4.5 V		3	3.2	3.4	V
CAPACITANCE							
C_{IN}	External input capacitance	ceramic		88			µF
		non-ceramic			660		µF
C_{OUT}	External output capacitance	ceramic (7)		188			µF
		non-ceramic (7)		940		4000 (8)	µF
			ESR (9)			5	mΩ

(6) Specified by design. Not production tested.
(7) The minimum required output capacitance consists of 4 × 47-µF ceramic capacitors and 2 × 470-µF, 10-mΩ ESR (5 mΩ equivalent).
(8) The proper frequency compensation network values are determined by the total amount of output capacitance. (See the *Setting the Compensation Network* section.)
(9) The maximum ESR refers to the combined equivalent ESR of all non-ceramic output capacitors. For example, two 10-mΩ ESR capacitors have a combined equivalent ESR of 5 mΩ.

6.6 Switching Characteristics

Over –40°C to 105°C free-air temperature range, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = I_{OUT} max, f_{SW} = 500 kHz, C_{IN1} = 4 × 22-µF 25-V 1210 ceramic, C_{IN2} = 2 × 330-µF electrolytic bulk, C_{OUT1} = 4 × 47-µF, 6.3-V 1210 ceramic, C_{OUT2} = 2 × 470-µF, 6.3-V polymer bulk (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_{SW}	Switching frequency	Factory default setting. RT_SEL grounded, No R_T resistor	425	500	575	kHz
		R_T = 68.1 kΩ, 1% RT_SEL open	255	300	345	
		R_T = 20.0 kΩ, 1% RT_SEL open	850	1000	1150	
		Adjustment range	300		1000	
PWM						
t_{ON-MIN}	Minimum on time(1)			50	100	ns
$t_{OFF-MIN}$	Minimum off time(1)	f_{SW} = 1MHz		515	560	ns
SYNCHRONIZATION						
$V_{IH(sync)}$	High-level input voltage		2.2			V
$V_{IL(sync)}$	Low-level input voltage				0.8	V
D_{SYNC}	Sync input duty cycle	f_{SW} = 300 kHz to 1 MHz		50%		
f_{SYNC}	Sync frequency range		300		1000	kHz

(1) Specified by design. Not production tested.

6.7 Programmable Characteristics

Over operating free-air temperature range, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFT START (PMBus Programmable)						
TON_RISE	Soft-start time	Factory default setting		3		ms
		Programmable range, 16 discrete settings(1)(2)	0		100	ms
		Accuracy, TON_RISE = 3 ms	–10%		10%	
TON_MAX_ FAULT_LIMIT	Upper limit in time to power up the output	Factory default setting(3)		0		ms
		Programmable range, 16 discrete settings(1)(3)	0		100	ms
		Accuracy(1)	–10%		10%	
TON_DELAY	Turnon delay	Factory default setting		0		ms
		Programmable range, 16 discrete settings (1)	0		100	ms
		Accuracy(1)	–10%		10%	
SOFT STOP (PMBus Programmable)						
TOFF_FALL	Soft-start time	Factory default setting		3		ms
		Programmable range, 16 discrete settings (1)(2)	0		100	ms
		Accuracy, TOFF_FALL= 1 ms	–10%		10%	
TOFF_DELAY	Turnon delay	Factory default setting(2)		0		ms
		Programmable range, 16 discrete settings(1)	0		100	ms
		Accuracy(1)	–10%		10%	
UNDERVOLTAGE LOCKOUT (UVLO) (PMBus Programmable)						
VIN_ON	Input turnon voltage	Factory default setting		4.5		V
		Programmable range, 15 discrete settings (1)	4.25		7.75	V
		Accuracy	–5%		5%	
VIN_OFF	Input turnoff voltage	Factory default setting		4		V
		Programmable range, 15 discrete settings(1)	4		7.5	V
		Accuracy(1)	–10%		10%	
TEMPERATURE SENSE AND THERMAL SHUTDOWN						

(1) Specified by design. Not production tested.
(2) Setting TON_RISE or TOFF_FALL to 0 ms programs the device to bring its output voltage up to the programmed regulation value or down to 0 V as quickly as possible, resulting in an effective TON_RISE and TOFF_FALL time of 1 ms.
(3) Setting TON_MAX_FAULT_LIMIT to 0 disables the TON_MAX_FAULT response.

Programmable Characteristics (continued)

Over operating free-air temperature range, V_{IN} = 12 V, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD}	Junction thermal shutdown temperature(1)			145	160	°C
T_{HYST}	Thermal shutdown hysteresis(1)			25		°C
OT_FAULT _LIMIT	Overtemperature fault limit	Factory default setting		145		°C
		Programmable range(1)	120		165	°C
OT_WARN _LIMIT	Overtemperature warning limit	Factory default setting		120		°C
		Programmable range(1)	100		140	°C
$T_{OT(hys)}$	Overtemperature fault warning hysteresis(1)		15	20	25	°C
MEASUREMENT SYSTEM						
$M_{VOUT(rng)}$	Output voltage measurement range(1)		0		5.8	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy(1)	V_{OUT} = 1.2 V	–2%		2%	
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution(1)			2^{-9}		V
$M_{IOUT(mg)}$	Output current measurement range(1)		0		52	A
$M_{IOUT(acc)}$	Output current measurement accuracy	$I_{OUT} \geq$ 20 A	–15%		15%	
		3 A ≤ I_{OUT} ≤ 20 A	–3		3	A
$M_{IOUT(lsb)}$	Output current measurement bit resolution(1)			62.5		mA
$M_{TSNS(mg)}$	Internal temperature sense range(1)		–40		165	°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy(1)	–40°C ≤ T_J ≤ 165°C	–5		5	°C
$M_{TSNS(lsb)}$	Internal temperature sense bit resolution(1)			1		°C
PMBus INTERFACE						
$V_{IH(PMBUS)}$	Logic-high voltage on CLK, DATA, CNTL		1.35			V
$V_{IL(PMBUS)}$	Logic-low voltage on CLK, DATA, CNTL				0.8	V
$V_{hysCNTL}$	Hysteresis on CNTL			170		mV
$I_{IH(PMBUS)}$	Input high-level current into CLK, DATA		–10		10	µA
$I_{IL(PMBUS)}$	Input low-level current into CLK, DATA		–10		10	µA
I_{CNTL}	CNTL pin pullup current		5		10	µA
$V_{OL(PMBUS)}$	Output low-level voltage on DATA, ALERT	V_{IN} > 4.5 V, $I_{OL(PMBUS)}$ = 4 mA			0.4	V
$I_{OH(PMBUS)}$	Output high-level leakage current into DATA, ALERT	Voltage on DATA, ALERT = 5.5 V			10	µA
$I_{OL(PMBUS)}$	Output low-level sinking current into DATA, ALERT	Voltage on DATA, ALERT< 0.4 V	4			mA
f_{PMBUS}	PMBus operating frequency	Slave mode	10		400	kHz

6.8 Typical Characteristics (V_{IN} = 12 V)

V_{IN} = 12 V, T_A = 25°C, f_{SW} = 500 kHz (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).

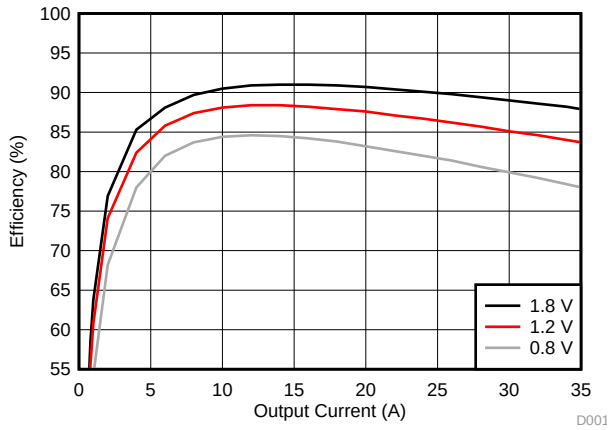


Figure 1. Efficiency vs Output Current

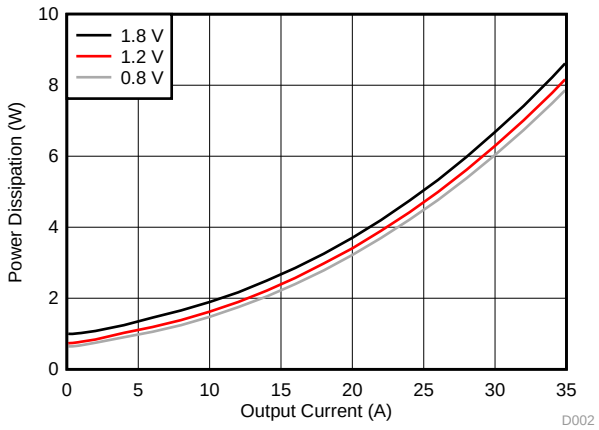


Figure 2. Power Dissipation vs Output Current

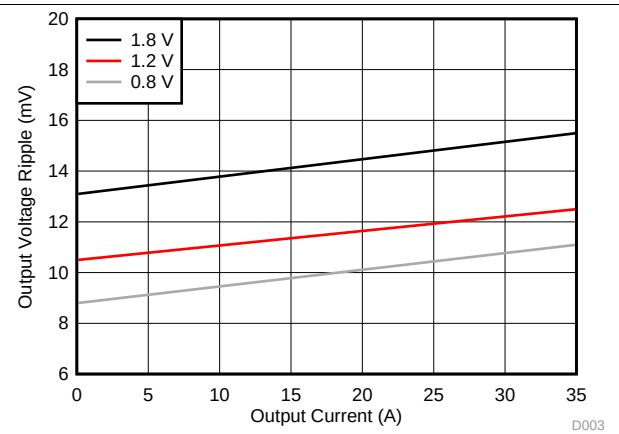


Figure 3. Voltage Ripple vs Output Current

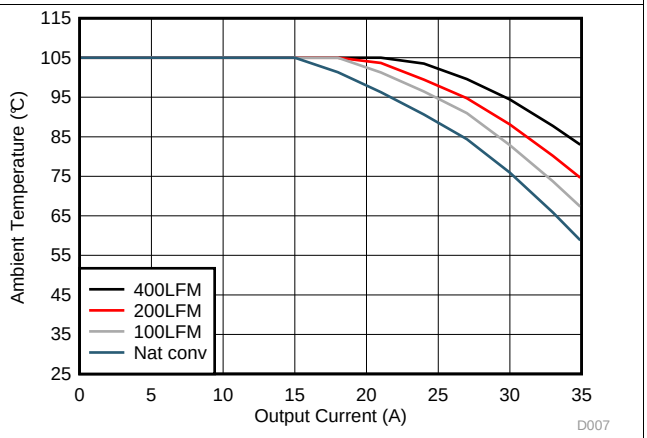


Figure 4. Safe Operating Area

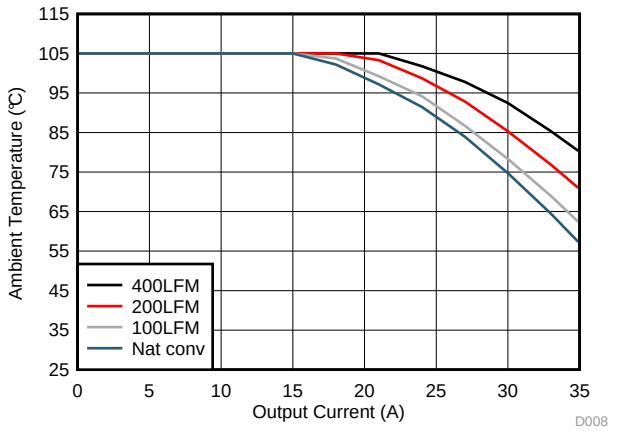


Figure 5. Safe Operating Area

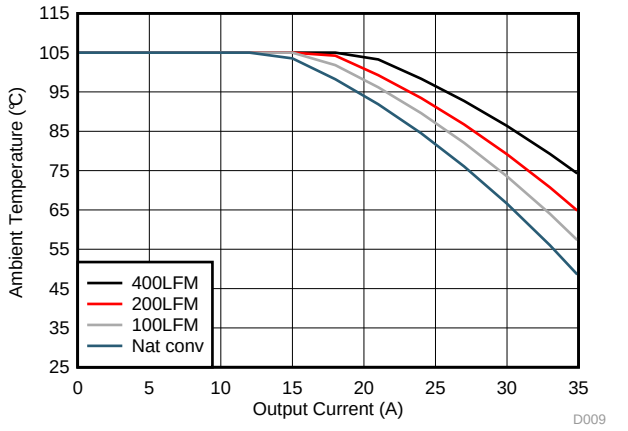
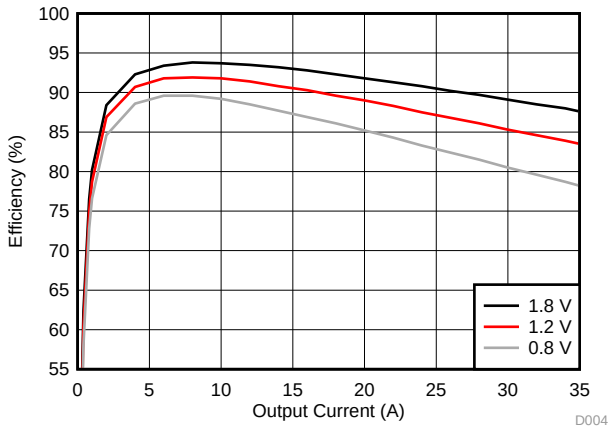


Figure 6. Safe Operating Area

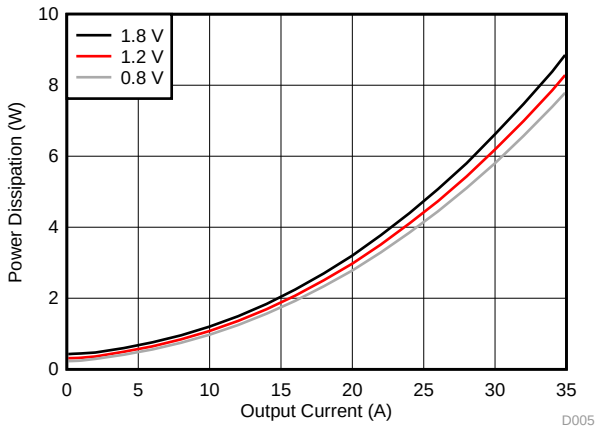
6.9 Typical Characteristics (V_{IN} = 5 V)

V_{IN} = 5 V, T_A = 25°C, f_{SW} = 500 kHz (unless otherwise specified). Safe operating area curves were measured using a Texas Instruments evaluation module (EVM).



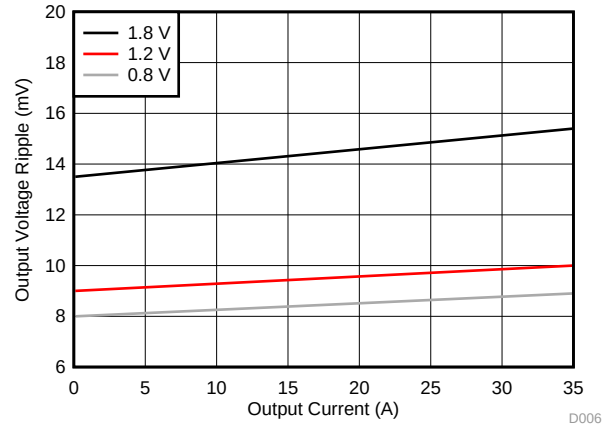
V_{IN} = 5 V f_{SW} = 500 kHz

Figure 7. Efficiency vs Output Current



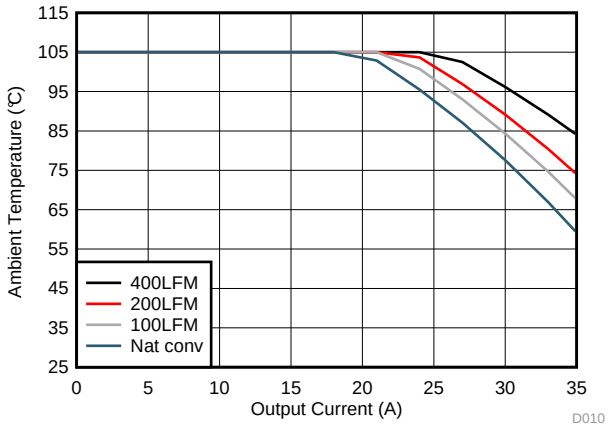
V_{IN} = 5 V f_{SW} = 500 kHz

Figure 8. Power Dissipation vs Output Current



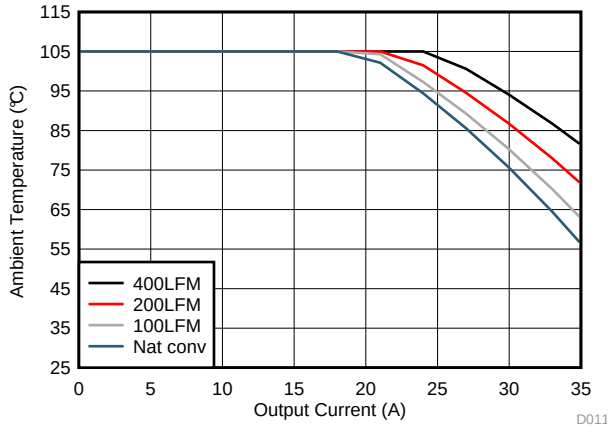
V_{IN} = 5 V f_{SW} = 500 kHz

Figure 9. Voltage Ripple vs Output Current



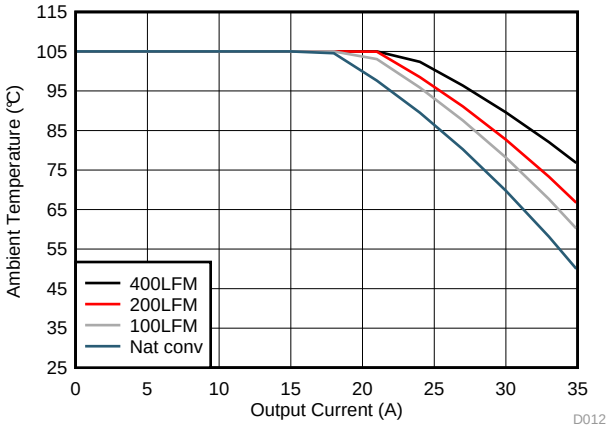
V_{IN} = 5 V V_{OUT} = 0.8 V f_{SW} = 500 kHz

Figure 10. Safe Operating Area



V_{IN} = 5 V V_{OUT} = 1.2 V f_{SW} = 500 kHz

Figure 11. Safe Operating Area



V_{IN} = 5 V V_{OUT} = 1.8 V f_{SW} = 500 kHz

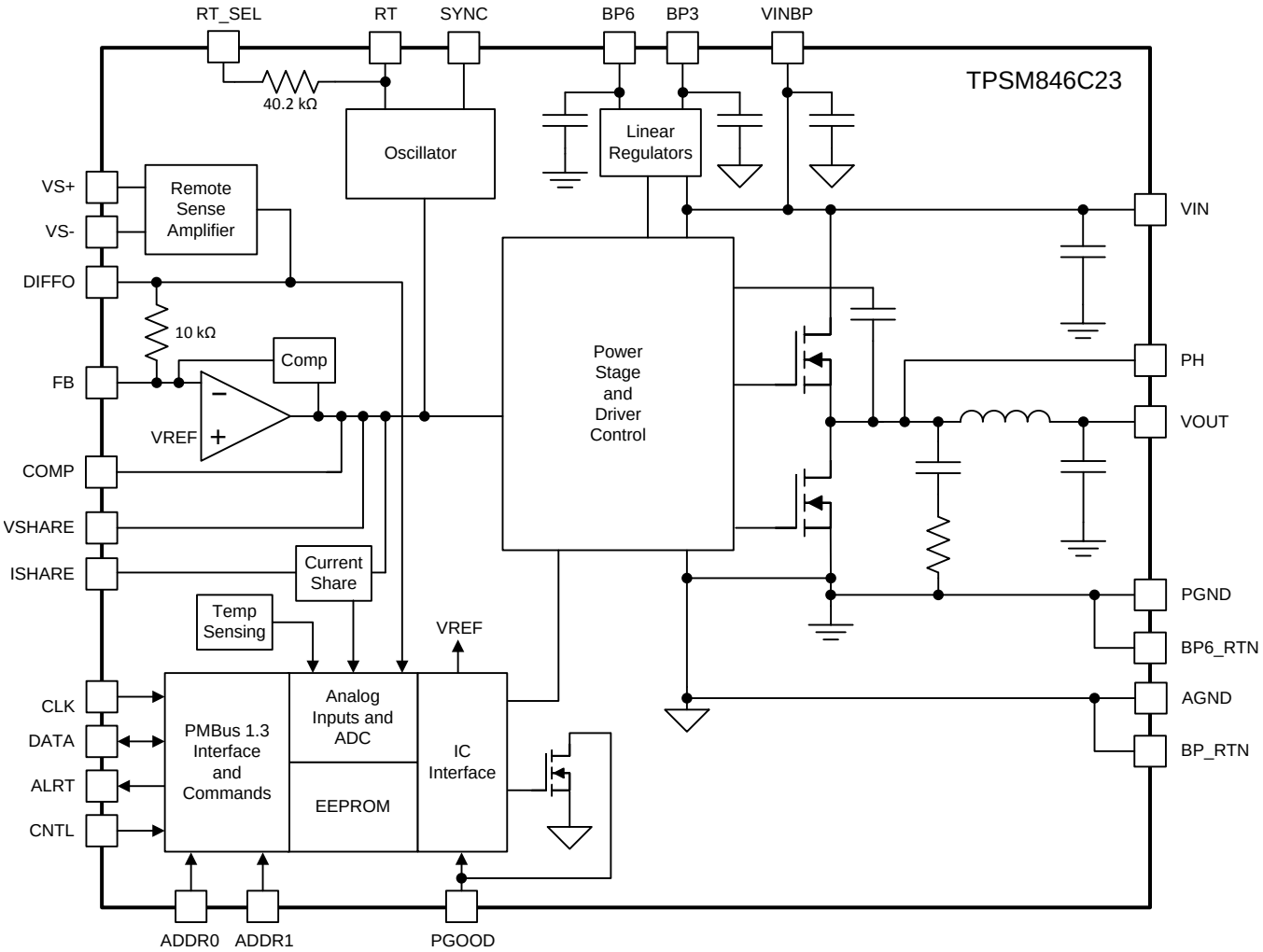
Figure 12. Safe Operating Area

7 Detailed Description

7.1 Overview

The TPSM846C23 device is a PMBus-1.3-compliant, 35-A, high-performance, synchronous buck-power module, enabling high-power density and minimal PCB area. This device implement the industry-standard fixed switching frequency, voltage-mode control with input feed-forward topology that responds instantly to input voltage change. This device can be synchronized to the external clock to eliminate beat noise and reduce EMI and EMC. Monotonic prebias capability eliminates concerns about damaging sensitive loads. Two TPSM846C23 devices can be paralleled together to provide up to 70-A load. Current sensing for overcurrent protection, current reporting, and current sharing between two devices are implemented by sampling a small portion of the power-stage current, which provides accurate information independent of the device temperature. The integrated PMBus interface capability provides precise current monitoring, voltage monitoring, and internal die-temperature monitoring, as well as many user-programmable configuration options including adaptive voltage scaling (AVS) function through standard VOUT_COMMAND on the PMBus.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PMBus

7.3.1.1 PMBus General Description

Timing and electrical characteristics of the PMBus interface specification can be found in the *PMB Power Management Protocol Specification, Part 1, revision 1.3* available at http://pmbus.org. The TPSM846C23 device supports both the 100-kHz and 400-kHz bus timing requirements. The devices do not stretch pulses when communicating with the master device.

Communication over the PMBus interface can support the packet error checking (PEC) scheme if desired. If the master supplies clock (CLK pin) pulses for the PEC byte, PEC is used. If the CLK pulses are not present before a STOP, the PEC is not used.

The devices support a subset of the commands in the PMBus 1.3 Power Management Protocol Specification. See *Supported PMBus Commands* for more information

The devices contain nonvolatile memory that stores configuration settings and scale factors. However, the device does not automatically save the settings programmed into this nonvolatile memory. The STORE_DEFAULT_ALL (11h) or STORE_USER_ALL (15h) command must be used to commit the current settings to nonvolatile memory as device defaults. The settings that are capable of being stored in nonvolatile memory are noted in the detailed command descriptions.

7.3.1.2 PMBus Address

The PMBus specification requires that each device connected to the PMBus have a unique address on the bus. The TPSM846C23 device has 64 possible addresses (0 through 63 in decimal) that can be assigned by connecting resistors from the ADDR0 and ADDR1 pins to AGND. The address is set in the form of two octal digits (0 to 7), one digit for each pin. ADDR1 is the high order digit, and ADDR0 is the low-order digit. These address selection resistors must be 1% tolerance or better. Using resistors other than the recommended values can result in devices responding to adjacent addresses. The PMBus address, in decimal, is given by the following expression:

PMBus Address = 8 × ADDR1(level) + ADDR0(level)

The E96 series resistors with no worse than 1% tolerance suggested for each digit value are shown in Table 1.

Table 1. Required Address Resistors

LEVEL	RESISTOR VALUE (kΩ)
0	7.15
1	14
2	22.6
3	34.8
4	51.1
5	78.7
6	121
7	187

The TPSM846C23 device also detects values that are out of range on the ADDR0 and ADDR1 pins. If the device detects that either pin has an out-of-range resistance connected to it, the device continues to respond to PMBus interface commands, but does so at address 127 decimal, which is outside of the possible programmed addresses. It is possible, but not recommended, to use the device in this condition, especially if other devices are present on the bus or if another device could possibly occupy the 127 decimal address.

Certain addresses in the I^2C address space are reserved for special functions, and it is possible to set the address of the devices to respond to these addresses. The user is responsible for knowing which of these reserved addresses are in use in a system and for setting the address of the devices accordingly so as not to interfere with other system operations. The devices can be set to respond to the global call address or 0. TI recommends not setting the devices to this address unless the user is certain that no other devices respond to this address and that the overall bus is not affected by having such an address present.

7.3.1.3 PMBus Connections

The PMBus interface implemented in the TPSM846C23 device consists of four signal lines: CLK, DATA, ALERT, and CNTL. The electrical specifications for the hardware interface follow the specifications given in System Management Bus (SMBus) specification V2.0. The module supports both the 100-kHz and 400-kHz bus speeds. For 400-kHz operation, observe the high-power DC specifications found in section 3.1.3 of the SMBus specification.

Communication over the PMBus using packet error checking (PEC) is supported but is optional. If the master supplies CLK pulses for the PEC byte, the PEC is used. If CLK pulses are not present before a STOP, the PEC is not used. When data is transmitted over the bus, the lowest order byte is sent first, and the highest order byte is sent last. Within any byte, the most significant bit (MSB) is sent first, and the least significant bit (LSB) is sent last.

The TPSM846C23 supports the SMBALERT response protocol. This protocol is a mechanism by which a slave (the TPSM846C23) can alert the bus master, via the ALERT pin, that it must communicate. The master processes this event and simultaneously accesses all slaves on the bus (that support the protocol) through the alert response address. Only the slave that caused the alert acknowledges this request. The host performs a modified receive byte operation to get the slave address. At this point, the master can use the PMBus status commands to query the slave that caused the alert. For more information on the SMBus alert protocol, see the SMBus specification.

The CNTL signal is an input signal on the PMBus. It can be used to turn the power-conversion function of the module on and off in conjunction with commands received over the bus. It can be configured as an active high or active low signal through the ON_OFF_CONFIG command. The CNTL signal is programmed at the factory to be an active high signal; that is, the CNTL pin must be pulled high for power conversion to occur. The customer can change this configuration if desired.

For more information, see the *PMBus Interface* section of the *Programmable Characteristics* table.

7.3.1.4 Supported PMBus Commands

The commands listed in Table 2 are implemented as described to conform to the PMBus 1.3 specification. Table 2 also lists the default for the bit behavior and register values.

Table 2. Supported PMBus Commands and Default Values

CMD CODE	PMBus 1.3 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
01h	OPERATION	Can be configured through ON_OFF_CONFIG to be used to turn the output on and off with or without input from the CTRL pin.	OPERATION is not used to enable regulation	00h	No
02h	ON_OFF_CONFIG	Configures the combination of CNTL pin input and OPERATION command for turning output on and off.	CNTL only. Active High	16h	Yes
03h	CLEAR_FAULTS	Clears all fault status registers to 0x00 and releases SMBALERT.	Write-only	n/a	No
10h	WRITE_PROTECT	Used to control writing to the volatile operating memory (PMBus and restore from EEPROM).	Allow writes to all registers	00h	Yes
11h	STORE_DEFAULT_ALL	Stores all current storable register settings into EEPROM as new defaults.	Write-only	n/a	No
12h	RESTORE_DEFAULT_ALL	Restores all storable register settings from EEPROM.	Write-only	n/a	No
15h	STORE_USER_ALL	Stores all current storable register settings into EEPROM as new defaults.	Write-only	n/a	No
16h	RESTORE_USER_ALL	Restores all storable register settings from EEPROM.	Write-only	n/a	No
19h	CAPABILITY	Provides a way for a host system to determine key PMBus capabilities of the device.	Read-only. PMBus v1.3, 400 kHz, PEC and SMBus Alert Response Protocol supported	B0h	No
1Bh	SMBALERT_MASK	Mask Warn or Fault status bits	Mask PGOOD only	n/a	Yes
20h	VOUT_MODE	Read-only output mode indicator.	Fixed at 2^{-9} (1.953 mV/count)	17h	No
21h	VOUT_COMMAND	Default regulation setpoint	500 mV	0100h	Yes

Table 2. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.3 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
24h	VOUT_MAX	Sets the maximum output voltage. VOUT_MAX imposes a higher bound to any attempted V_{OUT} setting.	If VOUT_SCALE_LOOP = 1: VOUT_MAX restores to 1.65 V	034Dh	No
			If VOUT_SCALE_LOOP = 0.5: VOUT_MAX restores to 3.3 V	069Ah	
			If VOUT_SCALE_LOOP = 0.25: VOUT_MAX restores to 6 V	0C00h	
27h	VOUT_TRANSITION_RATE	Sets the rate at which the output should change voltage.	1 mV/us	D03Ch	No
29h	VOUT_SCALE_LOOP	Sets output sense scaling ratio for main control loop.	1	F004h	Yes
2Bh	VOUT_MIN	Sets the minimum output voltage. VOUT_MIN imposes a lower bound to any attempted V_{OUT} setting.	If VOUT_SCALE_LOOP = 1: VOUT_MIN restores to 0.35 V	00B3h	No
			If VOUT_SCALE_LOOP = 0.5: VOUT_MIN restores to 0.7 V	0166h	
			If VOUT_SCALE_LOOP = 0.25: VOUT_MIN restores to 1.4 V	02CCh	
35h	VIN_ON	Sets value of input voltage at which the device must start power conversion.	4.5 V	F012h	Yes
36h	VIN_OFF	Sets value of input voltage at which the device must stop power conversion.	4 V	F010h	Yes
39h	IOUT_CAL_OFFSET	Can be set to null out offsets in the current sensing circuit.	0.0000 A	E000h	Yes
41h	VOUT_OV_FAULT_RESPONSE	Sets output overvoltage fault response.	Restart	BFh	Yes
45h	VOUT_UV_FAULT_RESPONSE	Sets output undervoltage fault response.	Ignore	3Fh	Yes
46h	IOUT_OC_FAULT_LIMIT	Sets the limit value of the output current that causes an overcurrent fault condition.	42 A	F854h	Yes
47h	IOUT_OC_FAULT_RESPONSE	Sets response to output overcurrent faults to latch-off, hiccup mode or ignore.	Hiccup/Restart	FFh	Yes
4Ah	IOUT_OC_WARN_LIMIT	Sets the limit value of the output current that causes an overcurrent warning condition.	37 A (87.5% of OCF)	F84Ah	No
4Fh	OT_FAULT_LIMIT	Sets the limit value of the sensed temperature that causes an overtemperature fault condition.	145°C	0091h	Yes
50h	OT_FAULT_RESPONSE	Sets response to over temperature faults to latch-off, hiccup mode or ignore.	Hiccup/Restart	BFh	Yes
51h	OT_WARN_LIMIT	Sets the limit value of the sensed temperature that causes an overtemperature warning condition.	120°C (OTF – 25°C)	0078h	No
60h	TON_DELAY	Sets the turnon delay.	0 ms	0000h	Yes
61h	TON_RISE	Sets the time from when the output starts to rise until the voltage has entered the regulation band.	3 ms	0003h	Yes
62h	TON_MAX_FAULT_LIMIT	Sets an UPPER limit, in milliseconds, that the unit can attempt to power up the output without reaching the output undervoltage fault limit. The time begins counting as the device enters the soft-start period.	Disabled	0000h	No
63h	TON_MAX_FAULT_RESPONSE	Sets the soft-start timeout fault response.	Restart	BFh	Yes
64h	TOFF_DELAY	Sets the turnoff delay.	0 ms	0000h	Yes
65h	TOFF_FALL	Sets the soft stop fall time.	3 ms	0003h	Yes
78h	STATUS_BYTE	Returns one byte summarizing the most critical faults.		Current status	No
79h	STATUS_WORD	Returns two bytes summarizing fault and warning conditions.		Current status	No
7Ah	STATUS_VOUT	Returns one byte detailing if an output fault or warning has occurred.		Current status	No
7Bh	STATUS_IOUT	Returns one byte detailing if an overcurrent fault or warning has occurred.		Current status	No
7Ch	STATUS_INPUT	Returns one byte of information relating to the status of the converter's input related faults.		Current status	No

Table 2. Supported PMBus Commands and Default Values (continued)

CMD CODE	PMBus 1.3 COMMAND NAME	PMBus COMMAND DESCRIPTION	DEFAULT BEHAVIOR	DEFAULT REGISTER VALUE	NVM
7Dh	STATUS_TEMPERATURE	Returns one byte detailing if a sensed temperature fault or warning has occurred.		Current status	No
7Eh	STATUS_CML	Returns one byte containing PMBus serial communication faults.		Current status	No
80h	STATUS_MFR_SPECIFIC	Returns one byte detailing if internal overtemperature or address detection fault has occurred.		Current status	No
8Bh	READ_VOUT	Returns the output voltage in volts.	Read only	Current status	No
8Ch	READ_IOUT	Returns the output current in amps.	Read only	Current status	No
8Dh	READ_TEMPERATURE_1	Returns the sensed die temperature in degrees Celsius.	Read-only	Current status	No
98h	PMBUS_REVISION	Returns PMBus revision to which the device is compliant.	PMBus 1.3	33h	No
ADh	IC_DEVICE_ID	This read-only block read command returns a single word (16 bits) with the unique device code identifier for each device for which this device can be configured. The BYTE_COUNT field in the block read command is 2 (indicating 2 bytes follow): low byte first, then high byte.	TPS546C23	4623h	No
AEh	IC_DEVICE_REV	This read-only block read command returns a single word (16 bits) with the unique device revision identifier. The BYTE_COUNT field in the block read command is 2 (indicating 2 bytes follow): low byte first, then high byte.	Read only	0001h	No
D0h	MFR_SPECIFIC_00	User scratch pad.		0000h	Yes
D4h	VREF_TRIM (MFR_SPECIFIC_04) (D4h)	Applies a fixed offset voltage to the error amplifier reference voltage (EA_REF).	Fixed offset of 0 mV	0000h	Yes
D5h	STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h)	Increases the value of the reference voltage by shifting the reference higher.	If RSMHI_VAL = 0: STEP_VREF_MARGIN_HIGH will restore to 17.6 mV	0009h	No
			If RSMHI_VAL = 1: STEP_VREF_MARGIN_HIGH will restore to 29.3 mV	000Fh	
D6h	STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h)	Decreases the value of the reference voltage by shifting the reference lower.	If RSMLO_VAL = 0: STEP_VREF_MARGIN_LOW will restore to –17.6 mV	FFF7h	No
			If RSMLO_VAL = 1: STEP_VREF_MARGIN_LOW will restore to –29.3 mV	FFF1h	
D7h	PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)	Sets the PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) Limits as a percentage of nominal.	–17% for UV Fault, –12% for UV Warning, +12% for OV Warning, +17% for OV Fault	00h	Yes
E5h	OPTIONS (MFR_SPECIFIC_21)	Sets user-selectable options.	See detailed command description	1084h	Yes
F0h	MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32)	Sets miscellaneous user-selectable options.	See detailed command description	0193h	Yes

7.3.2 Minimum Capacitance Requirements

For proper operation, the minimum required input capacitance network consists of four 22-µF (or two 47-µF) ceramic capacitors plus a 330-µF bulk capacitor. See capacitors C1 thru C5 in Figure 13. Place the ceramic capacitors as close as possible to the VIN pins. Connect the ground return path of the capacitors to PGND pins 42, 43, 54, and 59 of the TPSM846C23.

The minimum required output capacitance network consists of four 47-µF (or two 100µF) ceramic capacitors plus two 470-µF, low-ESR polymer capacitors. See capacitors C10 thru C15 in Figure 13. The combined ESR of the polymer capacitors must not be greater than 5 mΩ. Place the ceramic capacitors as close as possible to the VOUT and PGND pins of the module. This minimum network insures good transient response and minimal ripple amplitude. The total amount of output capacitance determines the values of the frequency compensation network. For more details see *Setting the Compensation Network*.

Additionally, the analog power path (VINBP) requires its own bypass network consisting of a 10-nF ceramic capacitor (C8 in Figure 13) and 1-µF ceramic capacitor (C7 in Figure 13) connected directly across pins 50 and 51 of the module. For proper operation, the two internal power supply rails of the module must also be bypassed. The 6.5-V rail (BP6) requires a 4.7-µF ceramic capacitor (C6 in Figure 13) placed across pins 48 and 49 of the module with short, direct traces. The 3.3-V rail (BP3) requires a 2.2-µF ceramic capacitor (C9 in Figure 13) placed very close to pins 47 and 51.

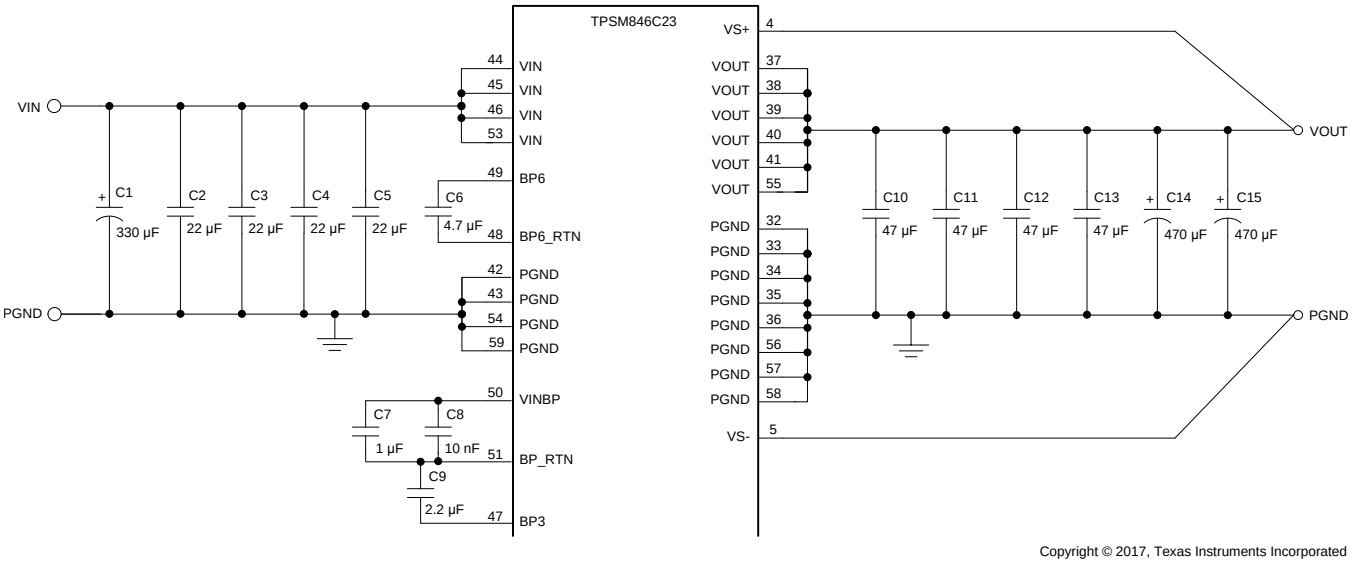


Figure 13. Required Capacitor Schematic

7.3.3 Setting the Compensation Network

The TPSM846C23 requires an external series resistor and capacitor compensation network to be connected between the DIFFO pin (pin 6) and the FB pin (pin 7). These are R_{COMP} and C_{COMP} in Figure 14. The value of these components is determined by the total amount of output capacitance and the switching frequency. Only ceramic and low-ESR, polymer-type capacitors are recommended. These parts should be placed as close as possible to the module and away from noisy signal traces. Suggested values for R_{COMP} and C_{COMP} for some typical values of output capacitance are given in Table 3. Determine final values by testing system stability using standard power supply evaluation techniques.

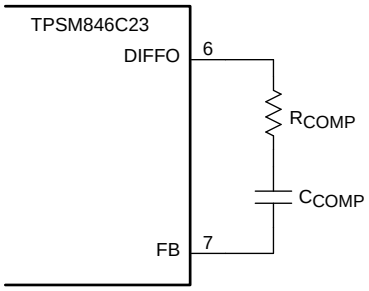


Figure 14. Compensation Components

Table 3. Recommended Compensation Components

TOTAL C_{OUT} (µF)		SWITCHING FREQUENCY						TYPICAL C_{OUT}	
		300 - 400 kHz		400 - 600 kHz		600 - 1000 kHz			
MIN	MAX	R_{COMP}	C_{COMP}	R_{COMP}	C_{COMP}	R_{COMP}	C_{COMP}	Ceramic	Polymer
1000	1500	1.0 kΩ	1000 pF	665 Ω	1500 pF	499 Ω	2200 pF	4 x 47 µF	2 x 470 µF
1500	3000	665 Ω	1500 pF	499 Ω	2200 pF	249 Ω	4700 pF	4 x 47 µF	4 x 470 µF
3000	5000	499 Ω	2200 pF	249 Ω	4700 pF	124 Ω	6800 pF	4 x 47 µF	4 x 1000 µF

7.3.4 Transient Response

The TPSM846C23 is designed to have an exceptional output voltage transient response to output current load steps. Table 4 shows the voltage deviation for several transient conditions.

Table 4. Output Voltage Transient Response

C_{IN} = 4 × 22-µF Ceramic, 2 × 330-µF Electrolytic							
V_{OUT} (V)	V_{IN} (V)	f_{SW} (kHz)	R_{COMP}	C_{COMP}	C_{OUT}		VOLTAGE (1) DEVIATION (mV)
					Ceramic	NON-CERAMIC (2)	
0.6	5	500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	33
		500	249 Ω	4700 pF	4× 47 µF	4× 1000 µF	22
	12	500	249 Ω	4700 pF	4× 47 µF	4× 470 µF	24
		750	124 Ω	6800 pF	4× 47 µF	4× 1000 µF	18
0.8	5	500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	37
		750	124 Ω	6800 pF	4× 47 µF	4× 1000 µF	19
	12	500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	33
		500	249 Ω	4700 pF	4× 47 µF	4× 1000 µF	20
1.0	5	500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	48
		500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	38
		500	249 Ω	4700 pF	4× 47 µF	4× 1000 µF	26
	12	500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	41
		500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	32
		750	499 Ω	2200 pF	4× 47 µF	2× 470 µF	26
1.2	5	500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	38
		750	499 Ω	2200 pF	4× 47 µF	2× 470 µF	34
	12	500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	39
		500	499 Ω	2200 pF	4× 47 µF	4× 470 µF	35
2.0	5	300	1.0 kΩ	1000 pF	4× 47 µF	2× 470 µF	50
		500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	38
	12	300	1.0 kΩ	1000 pF	4× 47 µF	2× 470 µF	57
		500	665 Ω	1500 pF	4× 47 µF	2× 470 µF	42

(1) 50% load step at 2.5 A/µs.
(2) The combined equivalent ESR of all non-ceramic output capacitance must be ≤ 5 mΩ.

7.3.5 Setting the Output Voltage via PMBus

The output voltage of the TPSM846C23 is designed to be set via the PMBus using the VOUT_COMMAND (21h). The output voltage is also dependant on the value of VOUT_SCALE_LOOP (29h) and the presence of a resistor, R_{SET}, from the FB pin (pin 7) to AGND. Table 5 illustrates the possible combinations. The module is programmed at the factory for a VOUT_SCALE_LOOP value of 1 and a VOUT_COMMAND value of 256 (100h), which produces an output voltage of 0.500 V.

Table 5. VOUT_SCALE_LOOP and Output Voltage Range

VOUT_SCALE_LOOP	R_{SET} VALUE	OUTPUT VOLTAGE RANGE (V)		VOUT_COMMAND DATA VALID RANGE	
		MIN	MAX	MIN (Hex)	MAX (Hex)
1	Not required	0.35	1.65	179 (0B3h)	845 (34Dh)
0.5	10 kΩ, 1%	0.7	2 (1)	358 (166h)	1024 (400h)

(1) The TPSM846C23 is designed to be operated with output voltages no higher than 2 V.

The output voltage is set by writing a value with the PMBus VOUT_COMMAND (21h). The VOUT_COMMAND value can be calculated using Equation 1, (round to the nearest integer value), and then converted to a 16 bit hexadecimal value. Using the Write Word protocol, write the hexadecimal word to the device using the VOUT_COMMAND.

$$\text{VOUT\_COMMAND value} = (\text{desired } V_{OUT} \times 512) \quad (1)$$

The value written using the VOUT_COMMAND is held in RAM and remains until it is re-written with a new value or if power is removed. If power is removed and then reapplied, the output voltage and the value in the VOUT_COMMAND register are restored to the value stored in the non-volatile memory of the device. To save the VOUT_COMMAND value to non-volatile memory and make it the new default value, issue the STORE_DEFAULT_ALL command.

For output voltages ≤ 1.65 V, R_{SET} is not required. If an output voltage greater than 1.65 V is required, a 10-kΩ R_{SET} resistor must be populated. See Figure 15 for the proper connection of R_{SET}.

This device is electrically and thermally characterized up to a maximum of 2-V output, and a maximum of 70-W output power. Operation at higher output voltages may be possible, provided the maximum output power and other internal parameters are not exceeded. Higher output voltages require derating to the output current and may require higher switching frequencies. Consult the TI factory applications engineers for support.

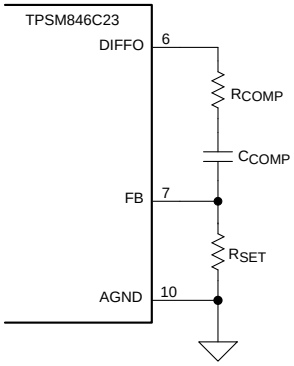


Figure 15. R_{SET} Resistor

7.3.6 Setting the Output Voltage Without PMBus

It is possible to operate the module without the need for a PMBus interface. To set the output voltage, the adjustment method requires a resistor, R_{SET}, connected between the FB pin and AGND as shown in Figure 15. To calculate the correct R_{SET} value, the default value of VOUT_COMMAND must be known. The factory default value of VOUT_COMMAND is 256 (100h), which produces an output voltage of 0.500 V if the R_{SET} resistor is not populated. Equation 2 can be used to calculate the R_{SET} value for a given output voltage, V_{OUT}. Additionally, the R_{SET} value can be selected from Table 6.

Do not set the output voltage higher than 2 V.

$$R_{SET} = \frac{10}{\left(\frac{(V_{OUT} \times 512)}{256} - 1\right)} (k\Omega) \quad (2)$$

Table 6. Standard R_{SET} Resistor Values

V_{OUT} (V)	R_{SET} (kΩ)	V_{OUT} (V)	R_{SET} (kΩ)
0.5	open	1.3	6.19
0.6	49.9	1.4	5.49
0.7	24.9	1.5	4.99
0.8	16.5	1.6	4.53
0.9	12.4	1.7	4.12
1	10	1.8	3.83
1.1	8.25	1.9	3.57
1.2	7.15	2	3.32

7.3.7 Differential Remote Sense

The TPSM846C23 device implements a differential remote-sense amplifier to provide excellent load regulation by cancelling IR-drop in high-current applications. The VS+ and VS– pins must be Kelvin-connected to the output capacitor bank directly at the load and routed back to the device as a tightly coupled differential pair. Ensure that these traces are isolated from fast switching signals and high current paths on the final PCB layout, as these can add differential-mode noise.

7.3.8 Voltage Reference

A reference digital-to-analog converter (DAC) with a 350-mV to 1650-mV range and 2^{-9}-V (1.953 mV) resolution connects to the noninverting input of the error amplifier. The tight tolerance on the reference voltage allows the user to design power supply with very-high DC accuracy.

7.3.9 Switching Frequency and Synchronization

7.3.9.1 Setting the Switching Frequency

The TPSM846C23 is set to a default switching frequency of 500 kHz. To operate the TPSM846C23 at the default switching frequency, connect the RT_SEL pin (pin 14) to AGND, and leave the RT pin (pin 13) open. To change the switching frequency, leave the RT_SEL pin open and connect a resistor from the RT pin (R_{RT}) to AGND. Use Equation 3 to calculate the R_{RT} resistor value.

$$R_{RT} = \frac{18290 + (120 \times V_{IN})}{f_{SW}\,(kHZ)} (k\Omega) \quad (3)$$

The TPSM846C23 devices are designed to operate from 300 kHz to 1 MHz.

7.3.9.2 Synchronization

The TPSM846C23 device can synchronize to an external clock that is ±20% of the free-running frequency set by R_{RT}. It is required that the external clock waveform is a square wave with a duty cycle of 50%.

7.3.9.2.1 Stand-Alone Device

The SYNC pin is factory-configured as an input pin. When power is applied, if no external clocking signal is present on the SYNC pin, the device operates at the switching frequency set by the internal or an external timing resistor. If an external clock signal that meets the specification of the Synchronization section of *Switching Characteristics* is applied to the SYNC pin, the device synchronizes to the leading edge of the applied waveform. The rising edge of the PH node lags the rising edge of the clocking waveform by approximately 500 ns. The external clock must be a 50% duty-cycle square wave. The external-clock frequency must be with ±20% of the free-running frequency set by the R_{RT} resistor. It is permissible for the SYNC signal to become active after the module has powered up. If this is done, there is a small disturbance in the output voltage while the module locks to the SYNC clock. If the SYNC signal is lost during operation, the module quickly detects the loss and reverts to switching at the frequency set by the R_{RT} resistor. A disturbance occurs in the output voltage upon loss of SYNC.

7.3.9.2.2 Paralleled Devices

When two TPSM846C23 devices are paralleled, the SYNC pins of the master and the slave must be supplied with a 50% duty-cycle clock signal at the desired switching frequency. The master device locks to the rising edge of the clock; the slave locks to the falling edge. The 50% duty cycle requirement insures the modules operate 180° out of phase to minimize ripple. Both the master and slave module must have an R_{RT} resistor present whose value sets a switching frequency within ±20% of the SYNC clock frequency. See *Parallel Application* for more information when paralleling devices.

7.3.10 Input Undervoltage Lockout (UVLO)

The TPSM846C23 device provides flexible user adjustment of the undervoltage lockout (UVLO) threshold and hysteresis. The minimum V_{IN} voltage required for power conversion is set by the stored VIN_ON (35h) value. The factory default value is 4.5 V. The turnon value can be set from 4.25 V to 7.75 V in 250-mV steps. The turnoff threshold voltage is stored in the VIN_OFF (36h) value. The factory default is 4 V. The value can be set from 4 V to 7.5 V in 250-mV steps. For more information, see Table 2.

7.3.11 Turnon and Turnoff Delay and Sequencing

The TPSM846C23 device provides many sequencing options. Using the ON_OFF_CONFIG command, the device can be configured to start up whenever the input voltage is above the UVLO threshold, to require an additional signal on the CNTL pin, to receive an update to the OPERATION command through the PMBus interface, or a combination of these configurations. When the gating signal as specified by the ON_OFF_CONFIG command is asserted, a programmable turnon delay can be set with the TON_DELAY command to delay the start of power conversion. Similarly, a programmable turnoff delay can be set with the TOFF_DELAY command to delay the stop of power delivery once the gating signal is deasserted. Delay times are specified in milliseconds (ms), from 0 to 100 ms.

The TPSM846C23, as supplied by the factory, is programmed for zero TOFF_DELAY and 3-ms TOFF_FALL parameters. The power stage discharges the output capacitors when CNTL is de-asserted or under a fault condition. Note that the power stage sinks current as it ramps the output voltage to zero. Once the output voltage is ramped to approximately 200 mV, the power stage will tri-state. This default behavior is set by the ON_OFF_CONFIG command register. The user can set the cpa bit if a controlled soft-stop discharge of the output capacitors is not desired. If this bit is set, the power stage is immediately tri-stated when CNTL is de-asserted or when a fault occurs. The load on the regulator output provides the only means of discharging the output capacitors.

Figure 16 shows control of the start-up and shutdown operations of the device when the device is configured to respond to both the CNTL signal and the OPERATION command. The device can also be configured to independently use either the CNTL signal or the OPERATION command or to convert power when a sufficient input voltage is available.

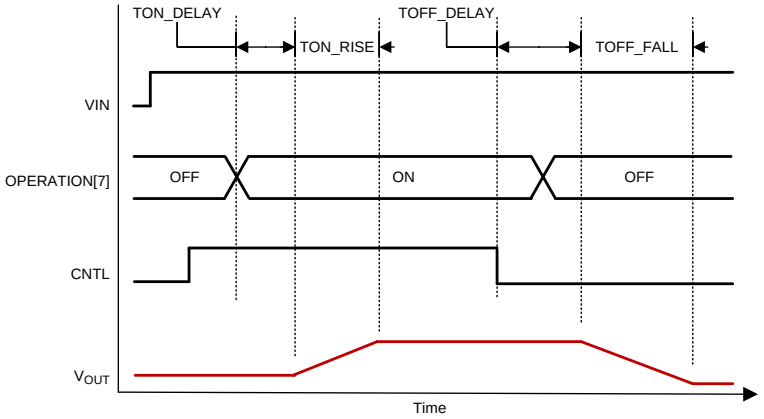


Figure 16. Turnon Controlled by Both Operation(1) and Control (1)

(1) Bit 7 of OPERATION is used to control power conversion.

7.3.12 Soft-Start Time and TON_RISE Command

To control the inrush current required to charge the output capacitor bank during start up, the TPSM846C23 device implements a soft-start time. When the device is enabled, the feedback reference voltage, V_{REF}, ramps from 0 V to the final level at a slew rate defined by the TON_RISE command. The specified rise times are defined by the slew rate required to ramp the reference voltage from 0 V to the final value at each given rise time.

The TPSM846C23 devices support several soft-start times from 1 ms to 100 ms, which are selected by the TON_RISE command.

7.3.13 Soft-Stop Time and TOFF_FALL Command

The TPSM846C23 device implements the TOFF_FALL command to define the time for the output voltage to drop from regulation to 0 as shown in Figure 16. Negative current in the TPSM846C23 device can occur during the TOFF_FALL time to discharge the output voltage. The setting of the TOFF_FALL command to 0 ms causes the TPSM846C23 to bring the output voltage down to 0 as quickly as possible, which results in an effective TOFF_FALL time of 1 ms (fastest time supported). The time is factory-set to 3 ms. This feature can be disabled in the ON_OFF_CONFIG command for the turnoff controlled by the CNTL pin or bit 6 of the OPERATION register if the regulator is turned off by the OPERATION command. If the regulator is turned off by the OPERATION command, both the high-side and low-side FET drivers are turned off immediately, and the output voltage is discharged only by the load.

7.3.14 Prebiased Output Start-Up

The TPSM846C23 device prevents current from being discharged from the output during start-up when a prebiased output condition exists. If the output is prebiased, no PH pulses occur until the internal soft-start voltage rises above the error-amplifier input voltage (FB pin). As soon as the soft-start voltage exceeds the error-amplifier input, and PH pulses start. The device limits synchronous rectification after each PH pulse with a narrow on-time. The on-time of the low-side MOSFET slowly increases on a cycle-by-cycle basis until 128 pulses have been generated and the synchronous rectifier runs fully complementary to the high-side MOSFET. This approach prevents the sinking of current from a prebiased output and ensures the output-voltage start-up and ramp-to-regulation sequences are smooth and monotonic.

If the prebias voltage is close to, or exceeds, the V_{OUT} setpoint voltage, the mandatory 128 switching cycles, as previously described, may induce a non-monotonic dip in the output voltage. The output voltage quickly recovers to the setpoint value once the 128 cycle interval is completed.

The output overvoltage warn is tripped when the FB pin is prebiased to higher than 5% above the regulation level. These devices respond to a prebiased output overvoltage condition immediately upon VIN powered up and when the BP6 regulator voltage is above the BP6 UVLO of 3.73 V (typical).

7.3.15 Power Good (PGOOD) Indicator

PGOOD is an open-drain digital active-high output signal that indicates if the output voltage is within regulation limits. A pullup resistor value between 10 kΩ and 100 kΩ to a voltage source of 5.5 V or less is required. The PGOOD window is defined by OV warning limit and UV warning limit in PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h), which can be programmed through the PMBus interface, as shown in Figure 17. The PGOOD pin pulls low upon any fault condition by default. See Table 7 for the possible sources to pull down the PGOOD pin.

The PGOOD signal can be connected to the CNTL pin of another device to provide additional controlled turnon and turnoff sequencing.

The OVW or PGOOD signal trips when the FB pin is prebiased to higher than 5% above the regulation level. This level of prebias is unusual, and it is beneficial to flag a warning in this situation.

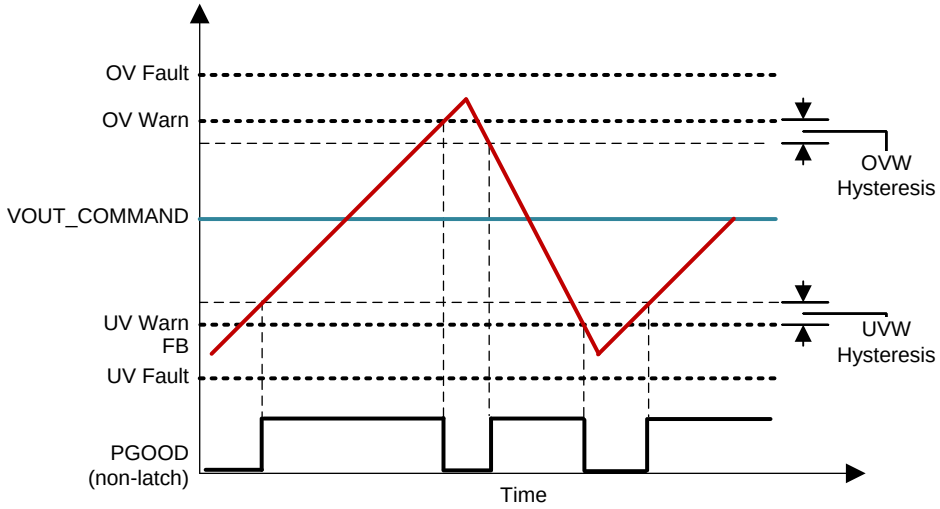


Figure 17. PGOOD Threshold and Hysteresis

NOTE

The presence of a pullup voltage at the PGOOD pin high before the TPSM846C23 device receives input power causes the PGOOD pin to be pulled above a logic-low-voltage level due to the limited pulldown capability in an un-powered condition. If this is not desired, increase the pullup resistance or reduce the external pullup-supply voltage.

7.3.16 Linear Regulators BP3 and BP6

The TPSM846C23 device has two onboard linear regulators to provide suitable power for the internal circuitry of the device. Bypass the BP3 and BP6 pins externally for the converter to function properly. The BP3 pin requires a minimum of 2.2 µF of capacitance connected to BP_RTN. The BP6 pin requires a minimum 4.7µF of capacitance connected to BP6_RTN.

The use of the internal regulators to power other circuits is not recommended because the loads placed on the regulators might adversely affect operation of the controller.

NOTE

Place bypass capacitors as close as possible to the device pins, with a minimum return loop back to ground and the return loop should be kept away from fast switching voltage and main current path. For more information, see the *Layout* section. Poor bypassing can degrade the performance of the regulator.

7.3.17 VREF_TRIM

The nominal output voltage of the converter can also be adjusted by changing the feedback voltage, V_{FB}, using the VREF_TRIM command. The adjustment range is from –64 × 1.953 mV to +63 × 1.953 mV from the nominal FB voltage. This command adjusts the final output voltage of the converter to a high degree of accuracy without relying on high-precision feedback resistors. The resolution of the adjustment is approximately 1.953 mV. The trim value can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

7.3.18 MARGIN

The TPSM846C23 device also allows simple testing of the output-voltage margin, by applying a either a positive or negative offset to the feedback voltage. The STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h) and STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h) commands control the size of the applied high offset or low offset (respectively). The adjustment range is from –64 × 1.953 mV to 31 × 1.953 mV from the nominal feedback voltage. The OPERATION command toggles the converter between the following three states:

- Margin none (no output margining)
- Margin high
- Margin low

Use Equation 4 to calculate the resulted internal-reference voltage.

$$EA\_REF = [(VOUT\_COMMAND \times VOUT\_SCALE\_LOOP) + (VREF\_TRIM + STEP\_VREF\_MARGIN\_HIGH \times OPERATION[5] + STEP\_VREF\_MARGIN\_LOW \times OPERATION[4])] \times 1.953\ mV \quad (4)$$

The total adjustable range of the output voltage, including VOUT_COMMAND, MARGIN, and VREF_TRIM, is limited by the internal reference DAC range of 0.35 V – 1.65 V. For more information on the implementation, see the *Supported PMBus Commands* section.

NOTE

- The VOUT_SCALE_LOOP is limited to only 2 possible options: 1 (default, no bottom resistor required for the divider), or 0.5 (R_{SET}= 10 kΩ).
- When VOUT_SCALE_LOOP is set to 1 (default), no bottom R_{SET} resistor is required. The reference voltage is equal to the output voltage, which allows tighter system DC accuracy by removing the resistor divider tolerance.
- If the divider ratio, R_{SET} / (R_{SET} + R1), does not match the programed VOUT_SCALE_LOOP, the user should be aware that the actual output voltage determined by Equation 2 and Equation 4 may not match the programed VOUT_COMMAND.

7.3.19 Parallel Application

Two TPSM846C23 devices can be paralleled for increased output current up to 70 A. Multiple connections must be made between the paralleled devices and the component selection is slightly different than for a stand-alone TPSM846C23 device. Figure 18 shows a typical schematic for two TPSM846C23 devices in parallel. Parallel operation can be evaluated using the TPSM846C23DEVM-807 evaluation board.

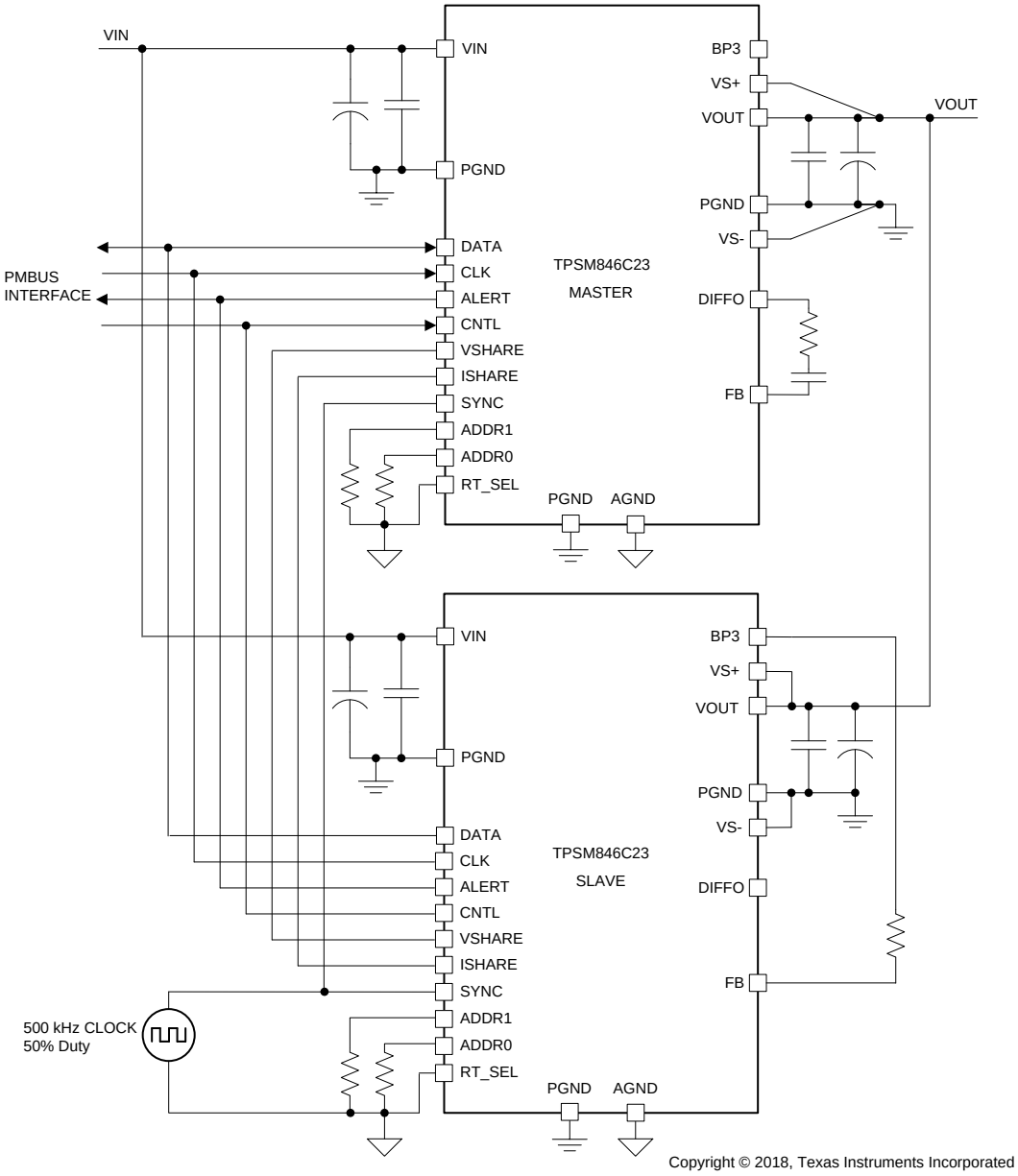


Figure 18. TPSM846C23 Parallel

7.3.20 Parallel Operation

To operate two TPSM846C23 devices in parallel, one of the devices must act as the master and the other act as a slave. To configure one of the devices as the slave device, connect a 1-kΩ resistor between the device FB pin and BP3 pin. Additionally, the SYNC, VSHARE, and ISHARE pins of both devices must be connected as shown in Figure 18. Both devices share the same VSHARE voltage. Essentially, the internal COMP voltage is shared between the two devices by connecting the VSHARE pin of each device together. By connecting the ISHARE pin of each device, the sensed current in each phase is compared, then the error current is added into the internal COMP. The resulting voltage is compared with the PWM ramp to generate the PWM pulse. This current sharing loop maintains the current balance between devices.

In addition to sharing the same internal COMP voltage, the VSHARE pin is also used for fault communication between the loop master and slave devices. The VSHARE pin voltage is pulled low if any device encounters any fault conditions so that the other device sharing VSHARE pin is alerted and stops switching accordingly.

The master and slave devices must be set to two different PMBus addresses. The telemetry data from the master and slave devices must be retrieved seperately.

When configured for parallel operation, the SYNC pins of the master and the slave must be supplied with a 50% duty cycle clock signal at the desired switching frequency. The master device locks to the rising edge of the clock; the slave locks to the falling edge. The 50% duty cycle requirement insures the modules operate 180° out of phase to minimize ripple. Both the master and slave module must have an R_{RT} resistor present whose value sets a switching frequency within ±20% of the SYNC clock frequency.

An optional high-frequency capacitor can be added between the VSHARE pin and ground in noisy systems, but the capacitance must not exceed 10 pF.

If operating conditions result in an on-time pulse width of ≤ 150 ns, jitter may be observed on the master and slave PH pins. The addition of a 10-kΩ resistor in series with the ISHARE connection between the devices helps to reduce, but may not eliminate the jitter.

To evaluate the TPSM846C23 in parallel configuration, an evaluation board is available. Also refer to the *Operating TPSM846C23 in Parallel* user's guide for operation instructions and layout recommendations.

7.3.21 Telemetry

7.3.21.1 Output Current Telemetry

The TPSM846C23 device senses the average output current using an internal sense FET. A sense FET conducts a scaled-down version of the power-stage current. Sampling this current in the middle of the low-side drive signal determines the average output current. This architecture achieves excellent current monitoring and better overcurrent threshold accuracy than the current sensing of a DC-resistance (DCR) inductor with minimal temperature variation and no dependence on power loss in a higher DCR inductor. Use the IOUT_CAL_OFFSET command to improve current sensing and overcurrent accuracy by removing systematic errors related to board layout after assembly. The device continually digitizes the sensed output current, and averages it to reduce measurement noise. The device then places the current value in the read-only register, READ_IOUT, which enables output-current telemetry.

This device cannot report negative (sinking) current. Any negative current is reported as zero amps.

7.3.21.2 Output Voltage Telemetry

The output voltage is sensed at the remote sense amplifier output pin, and the device continually digitizes the sensed output voltage, and averages it to reduce measurement noise. The device then stores the average value in the read-only register, READ_VOUT, which enables output voltage telemetry. Refer to OPTIONS (MFR_SPECIFIC_21) for details of programming output voltage telemetry signal range, averaging and update rate.

7.3.21.3 Junction Temperature Telemetry

The TPSM846C23 device also provides temperature telemetry and programmable internal overtemperature fault or warning thresholds using measurements from an internal temperature sensor. The temperature-sensor circuit applies two bias currents to an internal diode-connected NPN transistor and measures ΔV_{BE} to infer the junction temperature of the sensor. The device then digitizes the result and compares it to the user-configured overtemperature fault and warning thresholds. When an internal overtemperature fault (OTF) is detected, power

conversion stops until the sensed temperature decreases by 20°C. The READ_TEMPERATURE_1 (8Dh) register is continually updated with the digitized temperature measurement, enabling temperature telemetry. The OT_FAULT_LIMIT (4Fh) and OT_WARN_LIMIT (51h) commands set the overtemperature fault and warning thresholds through the PMBus interface. When an overtemperature event is detected, the device sets the appropriate flags in STATUS_TEMPERATURE (7Dh) command and triggers the SMBALERT signal if it is not masked.

7.3.22 Overtemperature Protection

An internal temperature sensor based off the bandgap reference protects the TPSM846C23 device from thermal runaway. The internal thermal shutdown threshold, T_{SD}, is fixed at 145°C (typical), which is different from the user programmable OT_FAULT_LIMIT. When the device senses a temperature above T_{SD}, an otf_bg bit in the STATUS_MFR_SPECIFIC command is flagged, and power conversion stops until the sensed junction temperature decreases by the amount of the thermal shutdown hysteresis, T_{HYST} (20°C typical). The SMBALERT signal is triggered if the signal is not masked.

The device response to an OT_FAULT_LIMIT event can be set to Latch-off, Restart and Ignore in OT_FAULT_RESPONSE. The default response to an over temperature fault is to shut down and then restart. Fixed band gap-detected overtemperature (OT) faults are never ignored. The band gap OT faults always respond in a shutdown and attempted restart once the device cools. Table 7 summarizes the fault-response scheme.

7.3.23 Overcurrent Protection

Both low-side overcurrent and high-side short-circuit protection are implemented. The low-side overcurrent fault and warning thresholds are programmed via PMBus. The low-side MOSFET average current is compared to the set fault threshold. High-side pulses are terminated on a cycle-by-cycle basis whenever the current through the high-side MOSFET exceeds the fixed short circuit threshold.

When either a low-side overcurrent or high-side short-circuit threshold is exceeded in a switching cycle, a counter is incremented. If no overcurrent condition is detected in a switching cycle, the counter is decremented. When the counter counts to three, an overcurrent fault condition is declared, and the output shuts down and restarts after 7 × TON_RISE time or is latched off until re-enabled, or ignored depending on the fault response setting. The behavior of the power stage during the various fault scenarios is shown in Table 7.

7.3.24 Output Overvoltage and Undervoltage Protection

The TPSM846C23 device includes both output overvoltage protection and output undervoltage protection capability by comparing the FB pin voltage to internal selectable pre-set voltages, as defined by the PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h) command.

If the FB pin voltage rises above the output overvoltage-protection threshold, the device terminates normal switching and turns on the low-side MOSFET to discharge the output capacitor and prevent further increases in the output voltage. The device also declares an OV fault, flagging the appropriate status registers, triggering SMBALERT if it is not masked. Then the device enters continuous-restart-hiccup mode or latches off according to the VOUT_OV_FAULT_RESPONSE command. The TPSM846C23 device responds to the output overvoltage condition immediately upon VIN power up and BP6 regulator voltage above its own UVLO of 3.73 V (typical). The VOUT_OV_FAULT_RESPONSE can also be set to ignore the output overvoltage fault and continue without interruption. Under this configuration, the control loop continues to respond and adjust PWM duty cycle to keep output voltage within regulation.

If the FB pin voltage falls below the undervoltage protection level after soft start has completed, the device terminates normal switching and forces both the high-side and low-side MOSFETs off and awaits an external reset or begins a hiccup time-out delay prior to restart, depending on the value of the VOUT_UV_FAULT_RESPONSE command. The device also declares a UV fault by flagging the appropriate status registers and triggering SMBALERT if it is not masked. The VOUT_UV_FAULT_RESPONSE can also be set to ignore the output undervoltage fault and continue without interruption for debug purpose.

Table 7 summarizes the fault-response scheme.

7.3.25 Fault Protection Responses

Table 7 summarizes the various fault protections and associated responses.

NOTE

When configured as parallel operation, the best practice is to have the fault response of the loop master and slave device set as the same to avoid unexpected behavior.

Table 7. Fault Protection Summary

FAULT or WARN	PROGRAMMING	FAULT RESPONSE SETTING	FET BEHAVIOR	ACTIVE DURING TON_RISE	SOURCE OF SMBALERT	SMBALERT MASKABLE	PGOOD
Internal Overtemperature Fault	OT_FAULT_LIMIT (4Fh)	Latch-off	Both FETs off	Yes	Yes	Yes	Low
		Restart	Both FETs off, then restart after cooling down (1)				Low
		Ignore	FETs still controlled by PWM				High
Internal Overtemperature Warn	OT_WARN_LIMIT (51h)	Latch-off or restart on fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore fault					High
Bandgap Overtemperature Fault	Threshold fixed internally	Latch-off	Both FETs off	Yes	Yes	Yes	Low
		Restart	Both FETs off, then restart after cooling down (1)				
		Ignore	Both FETs off, then restart after cooling down (2)				
Low-Side OC Fault	IOUT_OC_FAULT_LIMIT (46h)	Latch-off	3 PWM counts, then both FETs off	Yes	Yes	Yes	Low
		Restart	3 PWM counts, then both FETs off, restart after 7× TON_RISE				Low
		Ignore	FETs still controlled by PWM				High
Low-Side OC Warn	IOUT_OC_WARN_LIMIT	Latch-off or Restart on Fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore Fault					High
High-Side OC Fault		Latch-off	3 PWM counts, then both FETs off	Yes	Yes	Yes	Low
		Restart	3 PWM counts, then both FETs off, restart after 7 × TON_RISE				Low
		Ignore	Cycle-by-cycle peak current limit				High
V_{OUT} OV Fault	PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)	Latch-off	High-side FET OFF, low-side FET response configured byOV_RESP_SEL Bit: latch ON or turn on till FB drops below 0.2 V	Yes	Yes	Yes	Low
		Restart	High-side FET OFF, low-side FET response configured byOV_RESP_SEL Bit: latch ON or turn on till FB drops below 0.2 V. Then restart after 7 × TON_RISE				
		Ignore	PWM maintains control of FETs				

(1) When the overtemperature fault is tripped, the device shuts off both FETs and restarts until the sensed temperature decreases 20°C from the tripping threshold.
(2) The bandgap-overtemperature fault cannot be ignored, the device shuts off both FETs and restarts after the internal die temperature drops below the threshold.

Table 7. Fault Protection Summary (continued)

FAULT or WARN	PROGRAMMING	FAULT RESPONSE SETTING	FET BEHAVIOR	ACTIVE DURING TON_RISE	SOURCE OF SMBALERT	SMBALERT MASKABLE	PGOOD
V_{OUT} OV Warn	PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)	Latch-off or restart on fault	PWM maintains control of FETs	Yes	Yes	Yes	Low
		Ignore Fault					
V_{OUT} UV Fault	PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)	Latch-off	Both FETs off	No	Yes	Yes	Low
		Restart	Both FETs off, then restart after 7 × TON_RISE				
		Ignore	PWM maintains control of FETs				
V_{OUT} UV Warn	PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)	Latch-off or restart on fault	PWM maintains control of FETs	No	Yes	Yes	Low
		Ignore fault					
T_{ON} Max Fault	TON_MAX_FAULT_LIMIT	Latch-off	Both FETs off	No	Yes	Yes	Low
		Restart	Both FETs off, then restart after 7 × TON_RISE				
		Ignore	PWM maintains control of FETs				
VIN UVLO	VIN_ON, VIN_OFF	Shutdown	Both FETs off	Yes	Yes	Yes	Low

7.4 Device Functional Modes

7.4.1 Continuous Conduction Mode

The TPSM846C23 device operates in continuous conduction mode (CCM) at a fixed frequency, regardless of the output current. For the first 128 switching cycles, the low-side MOSFET on-time is slowly increased to prevent excessive current sinking in the event the device is started with a prebiased output. Following the first 128 clock cycles, the low-side MOSFET and the high-side MOSFET on-times are fully complementary.

7.4.2 Operation With CNTL Signal Control

According to the value in the ON_OFF_CONFIG register, the TPSM846C23 device can be commanded to use the CNTL pin to enable or disable regulation, regardless of the state of the OPERATION command. The CNTL pin can be configured as either active high or active low (inverted) logic. The TPSM846C23 is factory-programmed to use the CNTL pin only using active high logic.

7.4.3 Operation With OPERATION Control

According to the value in the ON_OFF_CONFIG register, the TPSM846C23 device can be commanded to use the OPERATION command to enable or disable regulation, regardless of the state of the CNTL signal.

7.4.4 Operation With CNTL and OPERATION Control

According to the value in the ON_OFF_CONFIG register, the TPSM846C23 device can be commanded to require both a signal on the CNTL pin, and the OPERATION command to enable or disable regulation.

7.5 Register Maps

This family of devices supports the following commands from the PMBus 1.3 specification.

Table 8. Legend for Register Access Type

Access Type	Code	Description
Read Type		
R	r	Read
Write Type		
W	w	Write
Other		
superscript E r/w^E	E	Bit is backed up with nonvolatile EEPROM

7.5.1 OPERATION (01h)

The OPERATION command turns the device output on or off in conjunction with input from the CNTL signal. It is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CNTL pin instructs the device to change to another mode.

For PWM loop slave device, which is recognized during power-up calibration, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

COMMAND	OPERATION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	ON	OFF	MARGIN				X	X
Default Value	0	0	0	0	0	0	X	X

7.5.1.1 On Bit

This bit is an enable command to the converter.

- 0: output switching is disabled. Both drivers placed in an off or low state.
- 1: output switching is enabled if the input voltage is above undervoltage lockout, OPERATION is configured as a gating signal in ON_OFF_CONFIG, and no fault conditions exist.

7.5.1.2 Off Bit

This bit sets the turnoff behavior when commanding the unit to turn off through OPERATION[7] (the *On* bit).

- 0: Immediately turn off the output (not honoring the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL)) when commanded off through OPERATION[7] (the *On* bit).
- 1: Use the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL) when commanded off through OPERATION[7] (also called *soft off*).

NOTE

The device ignores any values written to read-only bits. Additionally, both the on and off bits being set at the same time is not allowed and considered invalid data per section 12.1 of the PMBus Specification Part II; any attempt to do so causes the device to set the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers, and triggers SMBALERT signal.

7.5.1.3 Margin Bit

If Margin Low is enabled, load the value from the STEP_VREF_MARGIN_LOW command. If Margin High is enabled, load the value from the STEP_VREF_MARGIN_HIGH command.

- 0001: Margin Off. Output voltage source is VOUT_COMMAND. OV and UV faults are ignored.
- 0000, 0010, 0011: Margin Off. Output voltage source is VOUT_COMMAND. OV/UV faults behave normally as programmed in their respective fault response registers.
- 0101: Margin Low (Ignore Fault). Output voltage defined directly below.
- 0110: Margin Low (Act On Fault). Output voltage defined directly below.
- 1001: Margin High (Ignore Fault). Output voltage defined directly below.
- 1010: Margin High (Act On Fault). Output voltage defined directly below.
- 11XX, 0100, 0111, 1000, 1011: Shall be invalid and shall declare an Invalid Data Fault (Part II Rev 1.3 Section 10.9.3, Page 52)

VOUT_MARGIN_LOW data shall be equal to:
VOUT_COMMAND + (VREF_TRIM – STEP_VREF_MARGIN_LOW) / VOUT_SCALE_LOOP

VOUT_MARGIN_HIGH data shall be equal to:
VOUT_COMMAND + (VREF_TRIM + STEP_VREF_MARGIN_HIGH) / VOUT_SCALE_LOOP

For the Margin Low, Ignore Fault configuration (essentially [5:2] = 4'b0101), any incoming UV faults shall trigger the normal UVF status, and trigger SMB_ALERT (albeit the state machine response will be to ignore and not respond). If the desired response is to have the device to not trigger SMB_ALERT for UVF events when margining, they must set the UVF SMBALERT_MASK bit. For the Margin High, Ignore Fault configuration (essentially [5:2] = 4'b1001), any incoming OV faults shall trigger the normal OVF status, and trigger SMB_ALERT (albeit the state machine response will be to ignore and not respond). If the desired response is to have the device to not trigger SMB_ALERT for UVF events when margining, they must set the UVF SMBALERT_MASK bit. OVF and UVF can also be ignored when VOUT_COMMAND is the VOUT source by programming [5:2] to a value of 4'b0001. OVF and UVF events will still set status and trigger SMB_ALERT.

7.5.2 ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CNTL pin input and serial bus commands needed to turn the unit on and off. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL (11h) command. The default value in ON_OFF_CONFIG register is to have the device power up by CNTL pin only with the active high polarity and use the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL) for powering off the converter.

For PWM loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

COMMAND	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	X	X	X	pu	cmd	cpr	pol	cpa
Default Value	X	X	X	1	0	1	1	0

7.5.2.1 pu Bit

The pu bit sets the default to either operate any time power is present or for power conversion to be controlled by CNTL pin and PMBus OPERATION command. This bit is used in conjunction with the cpr, cmd, and on bits to determine start up.

BIT VALUE	ACTION
0	Device powers up any time power is present regardless of state of the CNTL pin.
1	Device does not power up until commanded by the CNTL pin and/or OPERATION command as programmed in bits [3:0] of the ON_OFF_CONFIG register.

7.5.2.2 cmd Bit

The cmd bit controls how the device responds to the OPERATION command. This bit is used in conjunction with the cpr, pu, and on bits to determine start up.

BIT VALUE	ACTION
0	Device ignores the "on" bit in the OPERATION command.
1	Device responds to the "on" bit in the OPERATION command.

7.5.2.3 cpr Bit

The cpr bit sets the CNTL pin response. This bit is used in conjunction with the cmd, pu, and on bits to determine start up.

BIT VALUE	ACTION
0	Device ignores the CNTL pin. Power conversion is controlled only by the OPERATION command.
1	Device requires the CNTL pin to be asserted to start the unit.

7.5.2.4 pol Bit

The pol bit controls the polarity of the CNTL pin. For a change to become effective, the contents of the ON_OFF_CONFIG register must be stored to nonvolatile memory using the STORE_DEFAULT_ALL command and the device power cycled. Simply writing a new value to this bit does not change the polarity of the CNTL pin.

BIT VALUE	ACTION
0	CNTL pin is active low.
1	CNTL pin is active high.

7.5.2.5 cpa Bit

The cpa bit sets the CNTL pin action when turning the converter off.

BIT VALUE	ACTION
0	Use the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL).
1	Immediately turn off the output (not honoring the programmed turnoff delay (TOFF_DELAY) and ramp down (TOFF_FALL)).

7.5.3 CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT signal output if the device is asserting the SMBALERT signal. The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately reset and the host notified by the usual means.

NOTE

- To get a reliable clear fault result, the clear_fault command should be issued (8 × TON_RISE + TON_DELAY) after the switcher shuts down.
- In the case of OV fault with a *latch off* response, the LS FET latches on when the fault is detected. If the OV_RESP_SEL Bit in (F0h) MFR_SPECIFIC_32 is set to 1, then the LS FET releases when the FB pin voltage falls below 0.2 V. Otherwise, it remains on until the CLEAR_FAULTS command is issued. The CLEAR FAULTS command causes the LS FET to turn off.
- CNTL pin toggling can also clear fault, but the logic low duration should be higher than 100 ns for the internal circuit to recognize.

7.5.4 WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to the device configuration or operation. All supported command parameters may have their parameters read, regardless of the WRITE_PROTECT settings. Write protection also prevents protected registers from being updated in the event of a RESTORE_DEFAULT_ALL. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

COMMAND	WRITE_PROTECT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r/w^E	X	X	X	X	X
Function	bit7	bit6	bit5	X	X	X	X	X
Default Value	0	0	0	X	X	X	X	X

7.5.4.1 bit5

BIT VALUE	ACTION
0	Enable all writes as permitted in bit6 or bit7
1	Disable all writes except the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND. (bit6 and bit7 must be 0 to be valid data)

7.5.4.2 bit6

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit7
1	Disable all writes except for the WRITE_PROTECT, and OPERATION commands. (bit5 and bit7 must be 0 to be valid data)

7.5.4.3 bit7

BIT VALUE	ACTION
0	Enable all writes as permitted in bit5 or bit6
1	Disable all writes except for the WRITE_PROTECT command. (bit5 and bit6 must be 0 to be valid data)

In any case, only one of the three bits may be set at any one time. Attempting to set more than one bit results in an alert being generated and the cml bit is STATUS_WORD being set. An invalid setting of the WRITE_PROTECT command results in no write protection.

Data Byte Value	ACTION
1000 0000	Disables all WRITES except to the WRITE_PROTECT command.
0100 0000	Disables all WRITES except to the WRITE_PROTECT, and OPERATION commands.
0010 0000	Disables all WRITES except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG, and VOUT_COMMAND commands.

7.5.5 STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed. Issuing STORE_DEFAULT_ALL also causes the device to be unresponsive through PMBus for a period of approximately 100 ms.

EEPROM programming faults cause the device to NACK and set the cml bit in the STATUS_BYTE and the mem bit in the STATUS_CML registers.

7.5.6 RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected according to current setting of WRITE_PROTECT. Issuing RESTORE_DEFAULT_ALL also causes the device to be unresponsive through PMBus for a period of approximately 100 ms.

NOTE

Do not use this command while the device is actively switching, this causes the device to stop switching and the output voltage to fall during the restore event. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but this usage is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. TI strongly recommends stopping the device before issuing this command.

7.5.7 STORE_USER_ALL (15h)

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

It is permissible to use this command while the device is switching. Note however that the device continues to switch but ignores all fault conditions until the internal store process has completed. Issuing STORE_USER_ALL also causes the device to be unresponsive through PMBus for a period of approximately 100 ms.

EEPROM programming faults cause the device to NACK and set the cml bit in the STATUS_BYTE and the mem bit in the STATUS_CML registers.

This command is equivalent to STORE_DEFAULT_ALL.

7.5.8 RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command restores all of the storable register settings from EEPROM memory to those registers which are unprotected according to current setting of WRITE_PROTECT. Issuing RESTORE_USER_ALL also causes the device to be unresponsive through PMBus for a period of approximately 100 ms.

This command is equivalent to RESTORE_DEFAULT_ALL.

NOTE

Do not use this command while the device is actively switching, this causes the device to stop switching and the output voltage to fall during the restore event. Depending on loading conditions, the output voltage could reach an undervoltage level and trigger an undervoltage fault response if programmed to do so. The command can be used while the device is switching, but this usage is not recommended as it results in a restart that could disrupt power sequencing requirements in more complex systems. TI strongly recommends stopping the device before issuing this command.

7.5.9 CAPABILITY (19h)

The CAPABILITY command provides a way for a host system to determine some key capabilities of this PMBus device.

COMMAND	CAPABILITY							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	PEC	SPD		ALRT	Reserved			
Default Value	1	0	1	1	0	0	0	0

The default values indicate that the device supports packet-error checking (PEC), a maximum bus speed of 400 kHz (SPD) and the SMBus alert-response protocol using SMBALERT.

7.5.10 SMBALERT_MASK (1Bh)

The SMBALERT_MASK command can be used to prevent a warning or fault condition from asserting the SMBALERT signal.

NOTE

The command uses the SMBus Write Word command protocol to overlay a “mask byte” with an associated/designated status register. It uses the SMBus Block Write/Block Read protocol – with a block size = 1, to read the mask settings for any given status register. If the host in the Block_Count field of the Block Write portion sends a block size unequal to 1 the device returns a NACK. The device always returns a Block Count of 1 upon reads of SMBALERT_MASK.

The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command were sent with the mask byte 01000000b, then an Overtemperature Warning condition would be blocked from asserting SMBALERT. Please refer to the PMBus v1.3 specification - section 15.38 (SMBALERT_MASK Command) and the SMBus specification Block Write/Block Read protocol for further details.

There are 19 maskable SMBALERT sources in the TPSM846C23. Each of these 19 status conditions has an associated EEPROM backed mask bit. These sources are represnted and identified in the status register command descriptions by a particular status bit denoted as having EEPROM backup (for example a bit access of r/w^{E}). Writes and reads to SMBALERT_MASK command code accepts only the following as valid STATUS_x command codes:

- STATUS_WORD
- STATUS_VOUT
- STATUS_IOUT
- STATUS_INPUT
- STATUS_TEMPERATURE
- STATUS_CML
- STATUS_MFR_SPECIFIC

Attempting to write a mask byte for any STATUS_X command code other than this list causes the device to set the cml bit in the STATUS_BYTE and the ivd bit in the STATUS_CML registers, and triggers SMBALERT. Attempting to read a mask byte for any STATUS_x command code other than this list returns 00h for the mask byte. Refer to these individual command descriptions for further details on their specific SMBALERT masking capabilities.

There is one unique status bit in the that warrants special clarification: PGOOD_Z (STATUS_WORD[10]) is maskable as an SMBALERT source through SMBALERT_MASK commands to STATUS_WORD. If the user wants to write, or read, the mask bit for PGOOD_Z, the user must put 79h in the STATUS_x COMMAND_CODE field of the SMBALERT_MASK command. PGOOD_Z SMBALERT_MASK bit default to 1.

7.5.11 VOUT_MODE (20h)

The PMBus specification dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit mode and 5-bit exponent parameter, as shown below. The 3-bit mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. The mode and exponent parameters are fixed and do not permit the user to change the values.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

COMMAND	VOUT_MODE							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Mode			Exponent				
Default Value	0	0	0	1	0	1	1	1

7.5.11.1 Mode Bit

Value fixed at 000, linear mode.

7.5.11.2 Exponent Bit

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent to 1.953 mV/count).

7.5.12 VOUT_COMMAND (21h)

The VOUT_COMMAND command sets the output voltage in volts. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command. The exponent is set be VOUT_MODE at –9 (equivalent of 1.953 mV/count). The programmed internal reference voltage is computed as:

$$EA\_REF = [(VOUT\_COMMAND \times VOUT\_SCALE\_LOOP) + (VREF\_TRIM + STEP\_VREF\_MARGIN\_HIGH \times OPERATION[5] + STEP\_VREF\_MARGIN\_LOW \times OPERATION[4])] \times 2^{-9} \text{ (V)} \quad (5)$$

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The range of valid VOUT_COMMAND values is dependent upon the configured VOUT_SCALE_LOOP (29h) as follows:

VOUT_SCALE_LOOP	Vout Range (volts)	VOUT_COMMAND data valid range
1	0.35 to 1.65	179 to 845
0.5	0.7 to 2.0 (1)	358 to 1024

(1) The TPSM846C23 is designed to be operated with output voltages no higher than 2.0V.

Any VOUT_COMMAND > 2816 (5.5-V maximum V_{OUT} equivalent) is treated as *invalid data*:

- NACK the data byte
- Do not update VOUT_COMMAND
- Set CML bit in STATUS_BYTE
- Set IVD bit in STATUS_CML

If the value programmed to VOUT_COMMAND exceeds the value stored in either VOUT_MIN or VOUT_MAX. In this case, VOUT_COMMAND will be set to the appropriate VOUT_MIN or VOUT_MAX value (which ever was violated). See the command descriptions for (28h) VOUT_MIN or (24h) VOUT_MAX for the specific status bits set in either case.

COMMAND	VOUT_COMMAND															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

7.5.12.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent to 1.953 mV/count, specified in VOUT_MODE command).

7.5.12.2 Mantissa

This is the Mantissa for the linear format. The default for this bit value is: 0000 0001 0000 0000 (binary) 256 (decimal) (equivalent Vout default = 0.5 V).

7.5.13 VOUT_MAX (24h)

The VOUT_MAX command sets the maximum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a higher than acceptable output voltage. VOUT_MAX imposes an upper bound to any attempt to program the output voltage to a VOUT_EQUIV setting by changing any of the following registers:

- VOUT_COMMAND
- VOUT_MAX
- VOUT_MIN
- OPERATION[5]
- OPERATION[4]
- VREF_TRIM
- STEP_VREF_MARGIN_HIGH
- STEP_VREF_MARGIN_LOW
- VOUT_SCALE_LOOP

The exponent is set be VOUT_MODE at –9 (equivalent to 1.953 mV/count). Use Equation 6 to calculate the programmed output voltage.

$$\text{MAXIMUM } V_{OUT} \text{ allowed} = \text{VOUT\_MAX} \times \text{VOUT\_MODE (V)} = \text{VOUT\_MAX} \times 2^{-9} \text{ (V)} \quad (6)$$

The range of valid VOUT_MAX values is dependent upon the configured (29h) VOUT_SCALE_LOOP as shown in Equation 7.

$$\text{MAXIMUM VOUT Reference allowed} = \text{VOUT\_MAX} \times \text{VOUT\_SCALE\_LOOP x VOUT\_MODE (V)} = \text{VOUT\_MAX} \times \text{VOUT\_SCALE\_LOOP} \times 2^{-9} \text{ (V)} \quad (7)$$

If the output voltage is turned on and any attempt is made to program any one of the following: (1) VOUT_EQUIV to be greater than VOUT_MAX; (2) VOUT_MAX to be less than, or equal to, VOUT_MIN, or; (3) VOUT_MIN to be greater than, or equal to, VOUT_MAX, – the TPSM846C23 will:

- Clamp the internal reference voltage to VOUT_MAX × VOUT_SCALE_LOOP × VOUT_MODE value. In the event VOUT_MAX < VOUT_MIN, VOUT_MAX shall dominate.
- Sets the OTH (other) bit in the STATUS_BYTE

- Sets the VFW bit in the STATUS_WORD
- Sets the VOUT_MAX_MIN_Warning bit in the STATUS_VOUTregister
- Notifies the host through the $\overline{\text{SMBALERT}}$ pin

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

COMMAND	VOUT_MAX															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

7.5.13.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95 mV/count, specified in VOUT_MODE command).

7.5.13.2 Mantissa

The range of valid VOUT_MAX values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0011 0100 1101 (binary) 845 (decimal) (equivalent VOUT_MAX = 1.65 V)
- Minimum: 0000 0001 0001 1010 (binary) 282 (decimal) (equivalent VOUT_MAX = 0.55 V)
- Maximum: 0000 0011 0100 1101 (binary) 845 (decimal) (equivalent VOUT_MAX = 1.65 V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0110 1001 1010 (binary) 1690 (decimal) (equivalent VOUT_MAX = 3.3 V)
- Minimum: 0000 0010 0011 0100 (binary) 564 (decimal) (equivalent VOUT_MAX = 1.1 V)
- Maximum: 0000 0110 1001 1010 (binary) 1690 (decimal) (equivalent VOUT_MAX = 3.3 V)

7.5.14 VOUT_TRANSITION_RATE (27h)

The VOUT_TRANSITION_RATE command sets the rate of change in mV/µs of any output voltage change during normal operation (also includes output voltage changes in TOFF_DELAY state. In contrast, the soft-start transition rate is controlled by TON_RISE and the TOFF_FALL transition rate is controlled by TOFF_FALL command).

For PWM loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

Only 8 fixed output voltage transition rates are available in the device. As such, the range of programmed V_{OUT}-transition rates are sub-divided into 8 *buckets* that then selects one of the 8 fixed V_{OUT}-transition rates. Programmed values are rounded to the nearest *bucket/transition rate* as outlined below:

COMMAND	VOUT_TRANSITION_RATE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	1	1	0	1	0	0	0	0	0	0	1	1	1	1	0	0

7.5.14.1 Exponent

default: 11010 (binary) –6 (decimal) (0.015625)

These default settings are not programmable.

7.5.14.2 Mantissa

default: 000 0011 1100 (binary) 60 (decimal) (equivalent VOUT_TRANSITION_RATE = 1 mV/µs)

NOTE

Using VOUT_TRANSITION_RATE to slew Vref faster than the voltage loop can track is possible, but may result in a overshoot/undershoot on the output voltage.

VOUT_TRANSITION rate (mV/µs)	VOUT_TRANSITION Mantissa (d)	
	Greater than	Less than or equal to
0.067	—	5
0.1	5	7
0.143	7	12
0.222	12	17
0.333	17	25
0.5	25	47
1	47	79
1.5	79	—

7.5.15 VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command is is limited to only 2 possible options/ratios: 1 (default, no R_{SET} needed), 0.5 (R_{SET}= 10 kΩ). Attempting to write a value unequal to one of these options cause the device to set the cml bit in the STATUS_BYTE, and the ivd bit in the STATUS_CML registers. Additionally, SMBALERT is asserted and the value of VOUT_SCALE_LOOP remains unchanged. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

NOTE

Construct the feedback resistor ratio appropriately (see Table 5). If the VOUT_SCALE_LOOP does not match the external feedback resistor ratio, the converter will regulate the output with the reference voltage as outlined in Equation 2. Program the VOUT_SCALE_LOOP setting before the output is turned on.

For the range checking to work properly and to avoid invalid data scenarios:

- VOUT_SCALE_LOOP should be changed first, if needed.
- VOUT_MIN and VOUT_MAX should be changed after VOUT_SCALE_LOOP, if needed.
- Additionally, it is assumed that VOUT_SCALE_LOOP will be programmed before the output is turned on; but, the hardware will not do anything to prohibit changing VOUT_SCALE_LOOP in any state.

COMMAND	VOUT_SCALE_LOOP															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0

7.5.15.1 Exponent

default: 11110 (binary) –2 (decimal) (equivalent LSB = 0.25)

These default settings are not programmable.

7.5.15.2 Mantissa

default: 000 0000 0100 (binary) 4 (decimal) (equivalent VOUT_SCALE_LOOP voltage = 1)

For VOUT_SCALE_LOOP = 1, mantissa = 004h. ($4 \times 2^{-2} = 1$)

For VOUT_SCALE_LOOP = 0.5, mantissa = 002h. ($2 \times 2^{-2} = 0.5$)

7.5.16 VOUT_MIN (2Bh)

The VOUT_MIN command sets the minimum output voltage. The purpose is to protect the devices on the output rail supplied by this device from a lower than acceptable output voltage. VOUT_MIN imposes a lower bound to any attempt to program the output voltage to a VOUT_EQUIV setting by changing any of the following registers:

- VOUT_COMMAND
- VOUT_MAX
- VOUT_MIN
- OPERATION[5]
- OPERATION[4]
- VREF_TRIM
- STEP_VREF_MARGIN_HIGH
- STEP_VREF_MARGIN_LOW
- VOUT_SCALE_LOOP

The exponent is set be VOUT_MODE at –9 (equivalent of 1.953 mV/count). Use Equation 8 to calculate the programmed output voltage.

$$\text{MINIMUM VOUT allowed} = \text{VOUT\_MIN} \times \text{VOUT\_MODE (V)} = \text{VOUT\_MIN} \times 2^{-9}\ \text{(V)} \quad (8)$$

The range of valid VOUT_MIN values is dependent upon the configured (29h) VOUT_SCALE_LOOP as shown in Equation 9.

$$\text{MINIMUM VOUT allowed} = \text{VOUT\_MIN} \times \text{VOUT\_SCALE\_LOOP} \times \text{VOUT\_MODE (V)} = \text{VOUT\_MIN} \times \text{VOUT\_SCALE\_LOOP} \times 2^{-9}\ \text{(V)} \quad (9)$$

If, while the output voltage is turned on, any attempt is made to program: (1) VOUT_EQUIV to be less than VOUT_MIN, the device will:

- Clamp the internal reference voltage to VOUT_MIN × VOUT_SCALE_LOOP × VOUT_MODE value. In the event VOUT_MAX < VOUT_MIN, VOUT_MAX shall dominate.
- Sets the OTH (other) bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the VOUT_MAX_MIN_Warning bit in the STATUS_VOUTregister
- Notifies the host through the $\overline{\text{SMBALERT}}$ pin

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

COMMAND	VOUT_MIN															
Format	Linear, unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Mantissa															

7.5.16.1 Exponent

Value fixed at 10111, Exponent for Linear mode values is –9 (equivalent of 1.95 mV/count, specified in VOUT_MODE command).

7.5.16.2 Mantissa

The range of valid VOUT_MIN values is dependent upon the configured (29h) VOUT_SCALE_LOOP as follows.

If VOUT_SCALE_LOOP = 1:

- default: 0000 0000 1011 0011 (binary) 179 (decimal) (equivalent VOUT_MIN = 0.35 V)
- Minimum: 0000 0000 1011 0011 (binary) 179 (decimal) (equivalent VOUT_MIN = 0.35 V)
- Maximum: 0000 0011 0000 0000 (binary) 768 (decimal) (equivalent VOUT_MIN = 1.5 V)

If VOUT_SCALE_LOOP = 0.5:

- default: 0000 0001 0110 0110 (binary) 358 (decimal) (equivalent VOUT_MIN = 0.7 V)
- Minimum: 0000 0001 0110 0110 (binary) 358 (decimal) (equivalent VOUT_MIN = 0.7 V)
- Maximum: 0000 0110 0000 0000 (binary) 1536 (decimal) (equivalent VOUT_MIN = 3 V)

7.5.17 VIN_ON (35h)

The VIN_ON command sets the value of the input voltage at which the unit should start operation assuming all other required startup conditions are met. Values are mapped to the nearest supported increment. Values outside the supported range are treated as invalid data and cause the device set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_ON remains unchanged on an out-of-range write attempt. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The supported VIN_ON values are shown in Table 9:

Table 9. Supported VIN_ON Values

VIN_ON Values (V)				
4.25	4.5 (default)	4.75	5	5.25
5.5	5.75	6	6.25	6.5
6.75	7	7.25	7.5	7.75

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT signal being asserted along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5-bit exponent and an 11-bit mantissa. The four most significant bits of the mantissa are fixed, while the lower 4 bits may be altered.

COMMAND	VIN_ON															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0

7.5.17.1 Exponent

default: 11110 (binary) –2 (decimal) (equivalent LSB = 0.25 V)

These default settings are not programmable.

7.5.17.2 Mantissa

default: 000 0001 0010 (binary) 18 (decimal) (equivalent VIN_ON voltage = 4.5 V)

Minimum: 000 0001 0001 (binary) 17 (decimal) (equivalent VIN_ON voltage = 4.25 V)

Maximum: 000 0001 1111 (binary) 31 (decimal) (equivalent VIN_ON voltage = 7.75 V)

7.5.18 VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage at which the unit should stop operation. Values are mapped to the nearest supported increment. Values outside the supported range is treated as invalid data and causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers, and trigger SMBALERT signal. The value of VIN_OFF remains unchanged during an out-of-range write attempt. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The supported VIN_OFF values are shown in Table 10:

Table 10. Supported VIN_OFF Values

VIN_OFF Values (V)				
4 (default)	4.25	4.5	4.75	5
5.25	5.5	5.75	6	6.25
6.5	6.75	7	7.25	7.5

VIN_ON must be set higher than VIN_OFF. Attempting to write either VIN_ON lower than VIN_OFF or VIN_OFF higher than VIN_ON results in the new value being rejected, SMBALERT being asserted along with the cml bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The data word that accompanies this command is divided into a fixed 5 bit exponent and an 11 bit mantissa. The 4 most significant bits of the mantissa are fixed, while the lower 7 bits may be altered.

COMMAND	VIN_OFF															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0

7.5.18.1 Exponent

default: 11110 (binary) –2 (decimal) (equivalent LSB = 0.25 V)

These default settings are not programmable.

7.5.18.2 Mantissa

default: 000 0001 0000 (binary) 16 (decimal) (equivalent VIN_OFF voltage = 4 V)

Minimum: 000 0001 0000 (binary) 16 (decimal) (equivalent VIN_OFF voltage = 4 V)

Maximum: 000 0001 1110 (binary) 30 (decimal) (equivalent VIN_OFF voltage = 7.5 V)

7.5.19 IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET command is used to compensate for offset errors in the READ_IOUT results and the IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT thresholds. The units are amperes. The default setting is 0 A. The resolution of the argument for this command is 62.5 mA and the range is +3.9375 A to –4 A. Values written outside of this range alias into the supported range. This occurs because the read-only bits are fixed. The exponent is always –4 and the 5 MSB bits of the Mantissa are always equal to the sign bit. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

COMMAND	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w^{E}	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										

COMMAND	IOUT_CAL_OFFSET															
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.19.1 Exponent

default: 11100 (binary) –4 (decimal) (LSB = 62.5 mA)

These default settings are not programmable.

7.5.19.2 Mantissa

MSB is programmable with sign, next 4 bits are sign extend only.
Lower six bits are programmable with a default value of 0 (decimal).

7.5.20 VOUT_OV_FAULT_RESPONSE (41h)

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an Output Over Voltage Fault based on MFR_SPECIFIC_07 (PCT_OV_UV_WRN_FLT_LIMITS). The device also:

- Sets the OVF bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the OVF bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The default response to a output overvoltage fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	VOUT_OV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	TD[2]	TD[1]	TD[0]
Default Value	1	0	1	1	1	1	1	1

7.5.20.1 RSP[1] Bit

This bit sets the output voltage overvoltage response to either ignore or not. The default for this bit is 1.

BIT VALUE	ACTION
0	The PMBus device continues operation without interruption. Note: In this *ignore* fault response mode, the associated fault status bits is set. Additionally, $\overline{\text{SMBALERT}}$ remains triggered if it is not masked.
1	The PMBus device shuts down and restarts according to RS[2:0].

7.5.20.2 RS[2:0] Bits

These bits are output voltage overvoltage retry setting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Note: because all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

7.5.20.3 TD[2:0] Bits

These bits are output voltage overvoltage retry time delay retting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry time delay setting means that the unit does not attempt to delay a restart. This is only supported when Restart is disabled by RS[2:0] = 000. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry time delay setting means that the unit waits 7 TON_RISE times before it goes through a normal startup (Soft start). This is only supported when Restart is enabled by RS[2:0] = 111.

These bits are direct reflections of the RS[2] (bit 5) value in this register.

7.5.21 VOUT_UV_FAULT_RESPONSE (45h)

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an Output Under Voltage Fault based on MFR_SPECIFIC_07 (PCT_OV_UV_WRN_FLT_LIMITS). The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the UVF bit in the STATUS_VOUT register, and
- Notifies the host by asserting SMBALERT

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The default response to a output undervoltage fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	VOUT_UV_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^{E}	r	r/w^{E}	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	TD[2]	TD[1]	TD[0]
Default Value	1	0	1	1	1	1	1	1

7.5.21.1 RSP[1] Bit

This bit sets the output voltage undervoltage response to either ignore or not. The default for this bit is 1.

BIT VALUE	ACTION
0	The PMBus device continues operation without interruption. Note: In this *ignore* fault response mode, the associated fault status bits are set. Additionally, SMBALERT continues to be triggered if it is not masked.
1	The PMBus device shuts down and restarts according to RS[2:0].

7.5.21.2 RS[2:0] Bits

These bits are output voltage undervoltage retry setting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry setting means that the unit goes through a normal startup (soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Because all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

7.5.21.3 TD[2:0] Bits

These bits are output voltage undervoltage retry time delay retting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry time delay setting means that the unit does not attempt to delay a restart. This is only supported when Restart is disabled by RS[2:0] = 000. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry time delay setting means that the unit waits 7 TON_RISE times before it goes through a normal startup (Soft start). This is only supported when Restart is enabled by RS[2:0] = 111.

These bits are direct reflections of the RS[2] (bit 5) value in this register.

7.5.22 IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. The IOUT_OC_FAULT_LIMIT should be set equal to or greater than the IOUT_OC_WARN_LIMIT. Writing a value to IOUT_OC_FAULT_LIMIT less than IOUT_OC_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command. Since 2-LSBs are not stored in EEPROM, on STORE, always round up. If IOUT_OC_FAULT_LIMIT [1:0] > 0, add 1 to IOUT_OC_FAULT_LIMIT [6:2]

The IOUT_OC_FAULT_LIMIT takes a two-byte data word formatted as shown below:

COMMAND	IOUT_OC_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w	r/w
Function	Exponent					Mantissa										
Default Value	See Below															

7.5.22.1 Exponent

default: 11111 (binary) –1 (decimal) (0.5 A)

These default settings are not programmable.

7.5.22.2 Mantissa

The upper four bits are fixed at 0.

The lower seven bits are programmable.

Use Equation 10 to calculate the actual output current for a given mantissa and exponent.

$$I_{OUT(oc)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (10)$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_FAULT_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPSM846C23	5	42	52	A

7.5.23 IOUT_OC_FAULT_RESPONSE (47h)

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an IOUT_OC_FAULT_LIMIT. The device also:

- Sets the OCF bit in the STATUS_BYTE
- Sets the OCFW bit in the STATUS_WORD
- Sets the OCF bit in the STATUS_IOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The default response to an overcurrent fault is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	IOUT_OC_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	RSP[0]	RS[2]	RS[1]	RS[0]	TD[2]	TD[1]	TD[0]
Default Value	1	1	1	1	1	1	1	1

7.5.23.1 RSP[1:0] Bits

These bits set the overcurrent fault response to either ignore or not. The default for this bit is 11b. Any value other than 00b or 11b will not be accepted, such and attempt will cause the 'cml' bit in the STATUS_BYTE register and the *ivd* bit in the STATUS_CML register to be set, and assert $\overline{\text{SMBALERT}}$. Because both bits must be the same, only one (bit 7) is stored in EEPROM. The default for this bit is 11b.

BIT VALUE	ACTION
00	The PMBus device continues operation without interruption. Note: In this "ignore" fault response mode, the associated fault status bits are set. Additionally, $\overline{\text{SMBALERT}}$ continues to be triggered if it is not masked.
11	The PMBus device shuts down and restarts according to RS[2:0].

7.5.23.2 RS[2:0] Bits

These bits are overcurrent fault retry setting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry setting means that the unit goes through a normal startup (soft-start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Because all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

7.5.23.3 TD[2:0] Bits

These bits are over current retry time delay retting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry time delay setting means that the unit does not attempt to delay a restart. This is only supported when Restart is disabled by RS[2:0] = 000. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry time delay setting means that the unit waits 7 TON_RISE times before it goes through a normal startup (Soft start). This is only supported when Restart is enabled by RS[2:0] = 111.

These bits are direct reflections of the RS[2] (bit 5) value in this register.

7.5.24 IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent warning. When this current level is exceeded the device:

- Sets the oth bit in the STATUS_BYTE
- Sets the OCFW bit in the STATUS_WORD
- Sets the OCW bit in the STATUS_IOUT register, and
- Notifies the host by asserting SMBALERT

The IOUT_OC_WARN_LIMIT threshold should always be set to less than or equal to the IOUT_OC_FAULT_LIMIT. Writing a value to IOUT_OC_WARN_LIMIT greater than IOUT_OC_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the SMBALERT signal. In such case, the register content will remain unchanged. This behavior can be overridden by the user setting Data Limit Override (DLO) in MFR_SPECIFIC_21[4].

The default IOUT_OC_WARN_LIMIT is always set to 87.5% of the OCF value. Because the IOUT_OC_WARN_LIMIT is not stored in EEPROM, the IOUT_OC_WARN_LIMIT register is set to 12.5% less than the stored OCF threshold upon any RESTORE from EEPROM (reset_restore, or RESTORE_DEFAULT_ALL command). The digital math to achieve this is: OCW_default = (OCF – OCF/8).

The IOUT_OC_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	IOUT_OC_WARN_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	See Below															

7.5.24.1 Exponent

default: 11111 (binary) –1 (decimal) (0.5 A)

These default settings are not programmable.

7.5.24.2 Mantissa

The upper four bits are fixed at 0.

Lower seven bits are programmable.

The actual output warning current level for a given mantissa and exponent is:

$$I_{OUT\,(OCW)} = \text{Mantissa} \times 2^{\text{Exponent}} = \frac{\text{Mantissa}}{2} \quad (11)$$

The default values and allowable ranges for each device are summarized below:

DEVICE	OC_WARN_LIMIT			UNIT
	MIN	DEFAULT	MAX	
TPSM846C23	4	37	50	A

7.5.25 OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an overtemperature fault condition, when the sensed temperature from the internal sensor exceeds this limit.

The OT_FAULT_LIMIT must always be greater than the OT_WARN_LIMIT. Writing a value to OT_FAULT_LIMIT less than or equal to OT_WARN_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as asserts the SMBALERT signal. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The OT_FAULT_LIMIT takes a two byte data word formatted as shown below.

COMMAND	OT_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1

7.5.25.1 Exponent

default: 00000 (binary) 0 (decimal) (represents mantissa with steps of 1 degree Celcius)

These default settings are not programmable.

7.5.25.2 Mantissa

default: 000 1001 0001 (binary) 145 (decimal) (145°C)

Minimum: 000 0111 1000 (binary) (equivalent OTF = 120°C)

Maximum: 000 1010 0101 (binary) (equivalent OTF = 165°C)

7.5.26 OT_FAULT_RESPONSE (50h)

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an OT_FAULT_LIMIT. The device also:

- Sets the OTFW bit in the STATUS_BYTE
- Sets the OTF bit in the STATUS_TEMPERATURE
- Notifies the host by asserting SMBALERT

When the overtemperature fault is tripped, the fault flag is latched until the internal sensed temperature decreases 20°C from the OT_FAULT_LIMIT.

The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The default response to an over temperature fault is to ignore. Fixed Bandgap Detected Overtemperature faults are never ignored. The Bandgap OT faults always respond in a shutdown and attempted restart once the part cools.

COMMAND	OT_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	TD[2]	TD[1]	TD[0]
Default Value	0	0	1	1	1	1	1	1

7.5.26.1 RSP[1] Bit

This bit sets the over temperature fault response to either ignore or not. The default for this bit is 0.

BIT VALUE	ACTION
0	The PMBus device continues operation without interruption. Note: In this “ignore” fault response mode, the associated fault status bits are set. Additionally, SMBALERT continues to be triggered if it is not masked.
1	The PMBus device shuts down and restarts according to RS[2:0].

7.5.26.2 RS[2:0] Bits

These bits are over temperature fault retry setting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the Retry Setting means that the unit goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert SMBALERT along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Because all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

NOTE

The programmed response here is also applied to the bandgap-detected overtemperture (OT) faults with the one exception of the *ignore* response. The fixed Bandgap-detected overtemperature faults are never ignored. The bandgap OT faults always respond in a shutdown and attempted restart when the part cools.

7.5.26.3 TD[2:0] Bits

These bits are overtemperature fault retry time delay retting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry time delay setting means that the unit does not attempt to delay a restart. This is only supported when restart is disabled by RS[2:0] = 000. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry time delay setting means that the unit waits 7 TON_RISE times before it goes through a normal startup (soft start). This is only supported when restart is enabled by RS[2:0] = 111.

These bits are direct reflections of the RS[2] (bit 5) value in this register.

7.5.27 OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the value of the temperature, in degrees Celsius, that causes an overtemperature warning condition, when the sensed temperature from the internal sensor exceeds this limit. Upon triggering the overtemperature warning, the device takes the following actions:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the OT Warning bit in the STATUS_TEMPERATURE
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

Once the overtemperature warning is tripped, the warning flag is latched until the internal sensed temperature decreases 20°C from the OT_WARN_LIMIT.

The OT_WARN_LIMIT must always be less than the OT_FAULT_LIMIT. Writing a value to OT_WARN_LIMIT greater than or equal to OT_FAULT_LIMIT causes the device to set the CML bit in the STATUS_BYTE and the invalid data (ivd) bit in the STATUS_CML registers as well as assert the $\overline{\text{SMBALERT}}$ signal. In such case, the register content will remain unchanged. This behavior can be overridden by the user setting Data Limit Override (DLO) in MFR_SPECIFIC_21[4].

The default OT_WARN_LIMIT is mathematically derived from the EEPROM backed OTF limit by subtracting 25 from (4Fh) OT_FAULT_LIMIT to reach the default OT_WARN_LIMIT. If the calculated OTW is less than 100°C, then the default value is set to 100°C. OTW=max(OTF-25, 100)

The OT_WARN_LIMIT takes a two byte data word formatted as shown below:

COMMAND	OT_WARN_LIMIT															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

7.5.27.1 Exponent

default: 00000 (binary) 0 (decimal) (represents mantissa with steps of 1 degree Celcius)

These default settings are not programmable.

7.5.27.2 Mantissa

default: 000 0111 1000 (binary) 120 (decimal) (120°C) 25°C less than default OTF

Minimum: 000 0110 0100 (binary) (equivalent OTF = 100°C)

Maximum: 000 1000 1100 (binary) (equivalent OTF = 140°C)

7.5.28 TON_DELAY (60h)

The TON_DELAY command sets the time in milliseconds, from when a start condition is received to when the output voltage starts to rise. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The TON_DELAY command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_DELAY															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.28.1 Exponent

default: 00000 (binary) 0 (decimal) (1 millisecond)

These default settings are not programmable.

7.5.28.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0000 (binary) (0 ms).

Only 16 fixed TON_DELAY times are available in the device. As such, the range of programmed TON_DELAY settings are sub-divided into 16 *buckets* that then selects one of the 16 supported times. Programmed values are rounded to the nearest *bucket/transition rate* as outlined in the table Supported TON_DELAY Values:

Table 11. Supported TON_DELAY Values

EFFECTIVE TON_DELAY (ms)	PROGRAMMED TON_DELAY MANTISSA (decimal)	
	Greater than	Less than or equal to
0 (50 us)	—	0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	—

7.5.29 TON_RISE (61h)

The TON_RISE command sets the time in milliseconds, from when the reference starts to rise until the voltage has entered the regulation band. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

Programming a value of 0 instructs the unit to bring its output voltage to the programmed regulation value as quickly as possible. For the device, this results in an effective TON_RISE time of 1ms (fastest time supported).

The TON_RISE command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_RISE															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

7.5.29.1 Exponent

default: 00000 (binary) 0 (decimal) (1 millisecond)

These default settings are not programmable.

7.5.29.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0011 (binary) (3 ms). For PWM loop slave device, the effective TON_RISE time is locked at 100 ms.

The supported TON_RISE times over PMBus are shown in Table 12:

Table 12. Supported TON_RISE Values

Effective TON_RISE (ms)	Programmed TON_RISE Mantissa (d)	
	Greater than	Less than or equal to
1	—	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62
72	62	86
100	86	—

7.5.30 TON_MAX_FAULT_LIMIT (62h)

The TON_MAX_FAULT_LIMIT command sets an UPPER limt in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit. The time begins counting as soon as the device enters the soft-start state begins to ramp the output. In other words, the TON_MAX_FAULT_LIMIT timer starts at the beginning of the TON_RISE state.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

When TON_MAX_FAULT_LIMIT is set to 0, the TON_MAX_FAULT timer is disabled, which means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely.

The device does not prohibit setting TON_MAX_FAULT_LIMIT < TON_RISE, however, in this configuration, the device will trigger a TON_MAX_FAULT if the VOUT has not risen above the UVF threshold by 4 seconds after the TON_DELAY and TON_RISE times expire.

The TON_MAX_FAULT_LIMIT command is formatted as a linear mode two's complement binary integer.

COMMAND	TON_MAX_FAULT_LIMIT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.30.1 Exponent

default: 00000 (binary) 0 (decimal) (Disable)

These default settings are not programmable.

7.5.30.2 Mantissa

The upper four bits are fixed at 0.

This register is not EEPROM backed, a RESTORE_DEFAULT_ALL command causes the TON_MAX_FAULT_LIMIT to restore to the default 0 ms value.

The supported TON_MAX_FAULT_LIMIT times over PMBus are shown below:

Table 13. Supported TON_MAX_FAULT_LIMIT Values

Effective TON_MAX_FAULT_LIMIT (ms)	Programmed TON_MAX_FAULT_LIMIT Mantissa (d)	
	Greater than	Less than or equal to
No Limit (timer disabled)	—	0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22
27	22	32
37	32	44
52	44	62

Table 13. Supported TON_MAX_FAULT_LIMIT Values (continued)

Effective TON_MAX_FAULT_LIMIT (ms)	Programmed TON_MAX_FAULT_LIMIT Mantissa (d)	
	Greater than	Less than or equal to
72	62	86
100	86	—

7.5.31 TON_MAX_FAULT_RESPONSE (63h)

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to an TON_MAX_FAULT_LIMIT.

The device also:

- Sets the oth bit in the STATUS_BYTE
- Sets the VFW bit in the STATUS_WORD
- Sets the TONMAXF bit in the STATUS_VOUT register, and
- Notifies the host by asserting $\overline{\text{SMBALERT}}$

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

The default response to a TON_MAX_FAULT is to shut down and restart with 7 × TON_RISE time delay.

COMMAND	TON_MAX_FAULT_RESPONSE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r/w	r/w	r	r	r
Function	RSP[1]	0	RS[2]	RS[1]	RS[0]	TD[2]	TD[1]	TD[0]
Default Value	1	0	1	1	1	1	1	1

7.5.31.1 RSP[1] Bit

This bit sets the TON_MAX_FAULT response to either ignore or not. The default for this bit is 1.

BIT VALUE	ACTION
0	The PMBus device continues operation without interruption. Note: In this *ignore* fault response mode, the associated fault status bits are set. Additionally, $\overline{\text{SMBALERT}}$ continues to be triggered if it is not masked.
1	The PMBus device shuts down and restarts according to RS[2:0].

7.5.31.2 RS[2:0] Bits

These bits are TON_MAX_FAULT retry setting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry setting means that the unit goes through a normal startup (soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown.

Any value other than 000 or 111 is not accepted. Attempting to write any other value is rejected, causing the device to assert $\overline{\text{SMBALERT}}$ along with the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML. Because all 3 bits must be the same, only one (bit 5) is stored in EEPROM.

7.5.31.3 TD[2:0] Bits

These bits are TON_MAX_FAULT retry time delay retting. The default for this bit is 111b.

BIT VALUE	ACTION
000	A zero value for the retry time delay setting means that the unit does not attempt to delay a restart. This is only supported when restart is disabled by RS[2:0] = 000. The output remains disabled until the fault is cleared (Refer to section 10.7 of the PMBus specification)
111	A one value for the retry time delay setting means that the unit waits 7 TON_RISE times before it goes through a normal startup (soft start). This is only supported when restart is enabled by RS[2:0] = 111.

These bits are direct reflections of the RS[2] (bit 5) value in this register.

7.5.32 TOFF_DELAY (64h)

The TOFF_DELAY command sets the time in milliseconds, from when a stop condition is received and when the output voltage starts to fall. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The TOFF_DELAY command is formatted as a linear mode two's complement binary integer.

COMMAND	TOFF_DELAY															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.32.1 Exponent

default: 00000 (binary) 0 (decimal) (1 millisecond)

These default settings are not programmable.

7.5.32.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0000 (binary) (0 ms).

Only 16 fixed TOFF_DELAY times are available in the device. As such, the range of programmed TOFF_DELAY settings are sub-divided into 16 *buckets* that then selects one of the 16 supported times. Programmed values are rounded to the nearest *bucket/transition rate* as outlined in the table Supported TOFF_DELAY Values:

Table 14. Supported TOFF_DELAY Values

EFFECTIVE TOFF_DELAY (ms)	PROGRAMMED TOFF_DELAY MANTISSA (decimal)	
	Greater than	Less than or equal to
0	—	0
1	0	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22

Table 14. Supported TOFF_DELAY Values (continued)

EFFECTIVE TOFF_DELAY (ms)	PROGRAMMED TOFF_DELAY MANTISSA (decimal)	
	Greater than	Less than or equal to
27	22	32
37	32	44
52	44	62
72	62	86
100	86	—

7.5.33 TOFF_FALL (65h)

The TOFF_FALL command sets the time in milliseconds, from the end of the TOFF_DELAY time until the voltage reaches 0 V. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

Programming a value of 0 instructs the unit to bring its output voltage down to 0 as quickly as possible. For the device, this results in actively ramping down the output voltage in 1 ms (the fastest supported ramp down).

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The TOFF_FALL command is formatted as a linear mode two's complement binary integer.

COMMAND	TOFF_FALL															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E
Function	Exponent					Mantissa										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.33.1 Exponent

default: 00000 (binary) 0 (decimal) (1 millisecond)

These default settings are not programmable.

7.5.33.2 Mantissa

The upper four bits are fixed at 0. The lower seven bits are programmable with a default value of 000 0000 0011 (binary) (3 ms).

The supported TOFF_FALL times over PMBus are shown in Supported TOFF_FALL Values:

Table 15. Supported TOFF_FALL Values

Effective TOFF_FALL (ms)	Programmed TOFF_FALL Mantissa (d)	
	Greater than	Less than or equal to
1	—	1
2	1	2
3	2	3
4	3	4
5	4	5
6	5	6
7	6	9
10	9	12
14	12	17
19	17	22

Table 15. Supported TOFF_FALL Values (continued)

Effective TOFF_FALL (ms)	Programmed TOFF_FALL Mantissa (d)	
	Greater than	Less than or equal to
27	22	32
37	32	44
52	44	62
72	62	86
100	86	—

7.5.34 STATUS_BYTE (78h)

The STATUS_BYTE command returns one byte of information with a summary of the most critical device faults.

COMMAND	STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	OVF	OCF	X	OTFW	CML	oth
Default Value	0	X	0	0	0	0	0	1

A 1 in any of these bit positions indicates that:

OFF The device is not providing power to the output, regardless of the reason. In this family of devices, this flag means that the converter is not enabled.

OVF An output overvoltage fault has occurred. This bit directly reflects the state of STATUS_VOUT[7] – OVF. If the user wants this fault source to be masked and not trigger SMBALERT, they must do it by masking STATUS_VOUT[7]. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_VOUT that cause this bit to be set. For loop slave device, this bit is 0.

OCF An output overcurrent fault has occurred. This bit directly reflect the state of STATUS_IOUT[7] – OCF. If the user wants this fault sourced to be masked and not trigger SMBALERT, they must do it by masking STATUS_IOUT[7]. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_IOUT that cause this bit to be set.

OTFW A temperature fault or warning has occurred. Check STATUS_TEMPERATURE. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_TEMPERATURE that cause this bit to be set.

CML A communications, memory or logic fault has occurred. Check STATUS_CML. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_CML that cause this bit to be set.

oth A fault or warning not listed through bits 1-7 has occurred, which include an undervoltage fault, over current warning, overvotlge warning, undervoltage warning, TON_MAX_FAULT, LOW_VIN, VOUT_MAX_MIN_Warning, OTF_BG, or IV_PPV1. Check other status registers. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_VOUT, STATUS_IOUT, STATUS_IOUT (7Bh), or STATUS_MFR_SPECIFIC (80h)that cause this bit to be set. The default for this bit is 1 because the default of STATUS_INPUT[3] LOW_Vin defaulting to 1.

7.5.35 STATUS_WORD (79h)

The STATUS_WORD command returns two bytes of information with a summary of the device fault and warning conditions. The low byte is identical to the STATUS_BYTE above. The additional byte reports the warning conditions for output overvoltage and overcurrent, as well as the power good status of the converter.

COMMAND	STATUS_WORD (low byte) = STATUS_BYTE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	X	OFF	OVF	OCF	x	OTFW	CML	oth
Default Value	0	X	0	0	0	0	0	1

COMMAND	STATUS_WORD (high byte)							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r^E	r	r	r
Function	VFW	OCFW	INPUT	MFR	PGOOD_Z	X	X	X
Default Value	0	0	X	0	X	0	0	0

A 1 in any of the high byte bit positions indicates that:

VFW An output voltage fault or warning has occurred (OVF or OVW or UVW or UVF or VOUT_MAX_Warning or TONMAXF). Check STATUS_VOUT. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_VOUT that cause this bit to be set.

OCFW An output current warning or fault has occurred (OCF or OCW). Check STATUS_IOUT. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_IOUT that cause this bit to be set.

INPUT INPUT fault or warning in STATUS_INPUT is present. Check STATUS_INPUT. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_INPUT that cause this bit to be set.

MFR An manufacturer specific fault or warning condition has occurred (over temperature fault from Bandgap or IV_PPV1). Check STATUS_MFR_SPECIFIC. Per the PMBus v1.3 spec sections 10.2.4 and 10.2.5, this bit is not clearable through a PMBus write. In contrast, the bit is to be cleared by clearing the bits in STATUS_MFR_SPECIFIC that cause this bit to be set.

PGOOD_Z Power is not good, and the following condition is present: output over or under voltage warning or fault, TON_MAX_FAULT, over temperature warning or fault, over current warning or fault, insufficient input voltage. Please refer to the FAULT RESPONSE table for the possible sources to trigger PGOOD_Z. The signal is unlatched and always represents the current state of the device. The factory default setting for PGOOD_Z mask bit is 1, indicating that PGOOD_Z itself cannot trigger SMBALERT by default. If unmask PGOOD_Z bit, the SMBALERT is set not to trigger before Power Good going high the first time, which is to avoid the device holding up SMBALERT bus when it is not commanded to start up and PGOOD stays low.

7.5.36 STATUS_VOUT (7Ah)

The STATUS_VOUT command returns one byte of information relating to the status of the output voltage related faults.

COMMAND	STATUS_VOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r/w^E	r	r
Function	OVF	OVW	UVW	UVF	VOUT_MAX_MIN_Warning	TONMAXF	X	X
Default Value	0	0	0	0	0	0	0	0

A 1 in any of these bit positions indicates that:

OVF The device has seen the output voltage rise above the output overvoltage fault threshold VOUT_OV_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

OVW The device has seen the output voltage rise above the output overvoltage warn threshold VOUT_OV_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

UVW The device has seen the output voltage fall below the output undervoltage warn threshold VOUT_UV_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

UVF The device has seen the output voltage fall below the output undervoltage fault threshold VOUT_UV_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

VOUT_MAX_MIN_Warning An attempt is made to program the VOUT_COMMAND in excess of the value in VOUT_MAX or under the value in VOUT_MIN. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

TONMAXF A TON_MAX_FAULT has occurred. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. For loop slave device, this bit is forced to 0.

7.5.37 STATUS_IOUT (7Bh)

The STATUS_IOUT command returns one byte of information relating to the status of the output current related faults.

COMMAND	STATUS_IOUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r/w^E	r	r	r	r	r
Function	OCF	X	OCW	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A 1 in any of these bit positions indicates that:

OCF The device has seen the output current rise above the level set by IOUT_OC_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

OCW The device has seen the output current rise above the level set by IOUT_OC_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

7.5.38 STATUS_INPUT (7Ch)

The STATUS_INPUT command returns one byte of information relating to the status of the input-related faults of the converter.

COMMAND	STATUS_INPUT							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w^E	r	r	r
Function	X	X	X	X	LOW_Vin	X	X	X
Default Value	0	0	0	0	1	0	0	0

A 1 in any of these bit positions indicates that:

LOW_Vin The unit is off because of insufficient input voltage. The bit sets when the unit powers up and stays set until the first time VIN exceeds VIN_ON. During the initial power up, LOW_Vin is not latched and does not trigger SMBALERT. Once VIN does exceed VIN_ON for the first time, any subsequent VIN < VIN_OFF events are latched, trigger SMBALERT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

7.5.39 STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns one byte of information relating to the status of the internal temperature related faults.

COMMAND	STATUS_TEMPERATURE							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r	r	r	r	r	r
Function	OTF	OTW	X	X	X	X	X	X
Default Value	0	0	0	0	0	0	0	0

A 1 in any of these bit positions indicates that:

OTF The measured internal temperature value of READ_TEMPERATURE_1 is equal to or greater than the level set by OT_FAULT_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. However, once cleared, the bit is set again unless the value in READ_TEMPERATURE_1 has fallen 20°C from the OT_FAULT_LIMIT.

OTW The measured internal temperature value of READ_TEMPERATURE_1 is equal to or greater than the level set by OT_WARN_LIMIT. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK. However, once cleared, the bit is set again unless the value in READ_TEMPERATURE_1 has fallen 20°C from the OT_WARN_LIMIT.

7.5.40 STATUS_CML (7Eh)

The STATUS_CML command returns one byte of information relating to the status of the communication-related faults of the converter.

COMMAND	STATUS_CML							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r/w^E	r/w^E	r/w^E	r	r	r/w^E	r
Function	ivc	ivd	pec	mem	X	X	oth	X
Default Value	0	0	0	0	0	0	0	0

A 1 in any of these bit positions indicates that:

ivc An invalid or unsupported command has been received. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

ivd An invalid or unsupported data has been received. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

pec A packet error check failed. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

mem A fault has been detected with the internal memory. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

oth Some other communication fault or error has occurred. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

7.5.41 STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC command returns one byte of information relating to the status of manufacturer-specific faults or warnings.

COMMAND	STATUS_MFR_SPECIFIC							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w^E	r	r	r/w^E	r	r	r	r
Function	otf_bg	illzero	illmany1s	iv_ppv1	iv_ppv0	0	is_Slave	sync_flt

COMMAND	STATUS_MFR_SPECIFIC							
Default Value	0	0	0	0	0	0	0	0

A 1 in any of these bit positions indicates that:

otf_bg The internal temperature from bandgap is above the thermal shutdown (TSD) fault threshold. This bit is writeable to clear and the EEPROM bit is for SMBALERT_MASK.

illzero The operation FSM has hit an illegal *ZERO* state. The FSM is a one-step implementation, so all zeros in the state is illegal and should never occur. This event is informational only and would not trigger SMBALERT.

illmany1s The operation FSM for has hit an illegal *more than one hot* state. The FSM is a one-hot implementation, so a state where multiple state bits are HI is illegal and should never occur. This event is informational only and would not trigger SMBALERT.

iv_ppv1 The ADDR1 detection fails to resolve 4 consecutive values. To avoid initial turnon events from clearing this condition and the user not being aware why the default ADDR1 value was used, this bit is only clearable through the CLEAR_FAULTS command or writing a logic 1 to this bit, essentially off and on events do not clear it as with the other standard status bits. This condition will trigger SMBALERT.

iv_ppv0 The ADDR0 detection fails.

sync_flt A synchronization fault. This could be because (a) Clock slave: an expected external SYNC was never present; or present, then lost, or (b) Clock master: an internal SYNC signal is not sensed on the SYNC pin. This bit is a live (essentially, unlatched) indicator. This event is informational only and would not trigger SMBALERT. This bit will always read 0 if the DIS_SYNC_FLT bit is set.

7.5.42 READ_VOUT (8Bh)

The READ_VOUT commands returns two bytes of data in the linear data format that represent the output voltage of the converter. The output voltage is sensed at the remote sense amplifier output pin so voltage drop to the load is not accounted for. The data format is as shown below:

COMMAND	READ_VOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Mantissa															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.42.1 Exponent

Value fixed at 10111, Exponent for linear mode values is –9 (equivalent of 1.95 mV/count, specified in the VOUT_MODE command).

7.5.42.2 Mantissa

Use Equation 12 to calculate the output voltage.

$$V_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \tag{12}$$

7.5.43 READ_IOUT (8Ch)

The READ_IOUT commands returns two bytes of data in the linear data format that represent the output current of the converter. The average output current is sensed according to the method described in *Low-Side MOSFET Current Sensing and Overcurrent Protection*. The data format is as shown below:

COMMAND	READ_IOUT															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

COMMAND	READ_IOUT															
Function	Exponent					Mantissa										
Default Value	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

The device scales the output current before it reaches the internal analog to digital converter so that resolution of the output current read is 62.5 mA. The maximum value that can be reported is 40 A. The user must set the IOUT_CAL_OFFSET parameter correctly to obtain accurate results. Use Equation 13 to calculate the output current.

$$I_{OUT} = \text{Mantissa} \times 2^{\text{Exponent}} \quad (13)$$

7.5.43.1 Exponent

default: 11100 (binary) -4 (decimal) (62.5 mA LSB)

These default settings are not programmable.

7.5.43.2 Mantissa

The lower 10 bits are the result of the ADC conversion of the average output current, as indicated by the output of the internal current sense amplifier. The 11th bit is fixed at 0 because only positive numbers are considered valid. Any computed negative current is reported as 0 A.

7.5.44 READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the internal die temperature in degrees Celsius.

COMMAND	READ_TEMPERATURE_1															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Exponent					Mantissa										

7.5.44.1 Exponent

default: 00000 (binary) 0 (decimal)

These default settings are not programmable.

7.5.44.2 Mantissa

The lower 11 bits are the result of the ADC conversion of the external temperature.

7.5.45 PMBUS_REVISION (98h)

The PMBUS_REVISION command returns a single, unsigned binary byte that indicates that these devices are compatible with the 1.3 revision of the PMBus specification (Part I and Part II).

COMMAND	PMBUS_REVISION							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Default Value	0	0	1	1	0	0	1	1

7.5.46 IC_DEVICE_ID (ADh)

Th IC_DEVICE_ID command is a read-only block-read command that returns a single word (16 bits) with the unique device-code identifier for each device for which this device can be configured. The BYTE_COUNT field in the block read command is 2 (indicating 2 bytes follow): low byte first, high byte second.

COMMAND	IC_DEVICE_ID
Format	Linear, binary

COMMAND	IC_DEVICE_ID															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Default Value	See below															

The default for the device identifier code is 4623h – Code Identifier for TPSM846C23.

7.5.47 IC_DEVICE_REV (AEh)

The IC_DEVICE_REV command is a read-only block-read command that returns a single word (16 bits) with the unique Device revision identifier. The DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision. The BYTE_COUNT field in the Block Read command is 2 (indicating 2 bytes follow): low byte first, high byte second.

COMMAND	IC_DEVICE_REV															
Format	Linear, tbinary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Default Value	See below															

The default of the device identifier code is 0001b.

7.5.48 MFR_SPECIFIC_00 (D0h)

The MFR_SPECIFIC_00 command is dedicated as a user scratch pad. Only the lower 8 bits are writeable for users. This is a read word command, with only the lower 8 bits accessible. This command is not a read byte command. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

COMMAND	MFR_SPECIFIC_00															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	User scratch pad															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.5.49 VREF_TRIM (MFR_SPECIFIC_04) (D4h)

The VREF_TRIM command applies a fixed offset voltage to the Error Amplifier reference (EA_REF) voltage. It is most typically used to trim the output voltage at the time the PMBus device is assembled into the end user's system. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The settings of the VOUT_MODE command determine the effect of VREF_TRIM command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal).

$$\text{EA\_REF} = [(\text{VOUT\_COMMAND} \times \text{VOUT\_SCALE\_LOOP}) + (\text{VREF\_TRIM} + \text{STEP\_VREF\_MARGIN\_HIGH} \times \text{OPERATION}[5] + \text{STEP\_VREF\_MARGIN\_LOW} \times \text{OPERATION}[4])] \times 1.953\ \text{mV} \quad (14)$$

The maximum trim ranges between –64*1.953 mV to +63*1.953 mV in 1.953-mV steps.

If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The value of EA_REF including VREF_TRIM is also limited by the values of VOUT_MAX, VOUT_MIN, VOUT_COMMAND, VOUT_SCALE_LOOP and STEP_VREF_MARGIN_HIGH/LOW. See VOUT_MAX and VOUT_MIN for additional details.

The EA_REF voltage transition occurs at the rate determined by the current state:

- Soft-Start: TON_RISE command
- Steady-State: VOUT_TRANSITION_RATE command
- TOFF_DELAY: VOUT_TRANSITION_RATE command
- Soft-Stop: TOFF_FALL command

The VREF_TRIM has two data bytes formatted as two's complement binary integer and can have positive and negative values.

COMMAND	VREF_TRIM															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w^{E}	r	r	r	r	r	r	r	r	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}
Function	High Byte								Low Byte							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

High Byte:

default: 0000 0000 (binary) 0 (decimal)
Minimum: 1111 1111 (binary) (sign extended)
Maximum: 0000 0000 (binary) (sign extended)

Low Byte:

default: 0000 0000 (binary) 0 (decimal)
Minimum: 1100 0000 (binary) –64 (decimal) (–125 mV) (sign extended, two's compliment)
Maximum: 0011 1111 (binary) 63 (decimal) (123 mV)

7.5.50 STEP_VREF_MARGIN_HIGH (MFR_SPECIFIC_05) (D5h)

The STEP_VREF_MARGIN_HIGH command, specifing a positive offset voltage on EA_VREF, is used to increase the reference voltage by shifting the reference higher. When the OPERATION command is set to *Margin High*, the output will increase by the voltage indicated by this command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). The actual reference voltage commanded by a margin high command can be found in Equation 14.

The margin high range is between 0 and 31 × 1.953 mV in 1.953-mV steps.

If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The value of EA_REF including STEP_VREF_MARGIN_HIGH is also limited by the values of VOUT_MAX, VOUT_MIN, VOUT_COMMAND, VOUT_SCALE_LOOP and VREF_TRIM. See VOUT_MAX and VOUT_MIN for additional details.

The EA_REF voltage transition occurs at the rate determined by the current state:

- Soft-Start: TON_RISE command
- Steady-State: VOUT_TRANSITION_RATE command
- TOFF_DELAY: VOUT_TRANSITION_RATE command
- Soft-Stop: TOFF_FALL command

COMMAND	STEP_VREF_MARGIN_HIGH															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							

High Byte:

default: 0000 0000 (binary) 0 (decimal)

Low Byte:

Minimum: 0000 0000 (binary) 0 (decimal) (0 mV)

Maximum: 0001 1111 (binary) 31 (decimal) (60.5 mV)

The read-writeable bits in this register do NOT have direct EEPROM backup; however, the register does restore to one of two configurable values as determined by RSMHI_VAL in (E5h) MFR_SPECIFIC_21 (OPTIONS).

- RSMHI_VAL = 0: STEP_VREF_MARGIN_HIGH will restore to 0009h (9 decimal or 17.6 mV).
- RSMHI_VAL = 1: STEP_VREF_MARGIN_HIGH will restore to 000fh (15 decimal or 29.3 mV).

7.5.51 STEP_VREF_MARGIN_LOW (MFR_SPECIFIC_06) (D6h)

The STEP_VREF_MARGIN_LOW command, specifying a negative offset voltage on EA_VREF, is used to decrease the reference voltage by shifting the reference lower. When the OPERATION command is set to *Margin Low*, the output will decrease by the voltage indicated by this command.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The effect of this command is determined by the settings of the VOUT_MODE command. In this device, the VOUT_MODE is fixed to Linear with an exponent of –9 (decimal). The actual reference voltage commanded by a margin low command can be found in Equation 14.

The margin low range is between -64*1.953 mV and -1*1.953 mV in 1.953-mV steps.

If a value outside this range is given with this command, the device sets the reference voltage to the upper or lower limit depending on the direction of the setting, asserts SMBALERT and sets the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

The value of EA_REF including STEP_VREF_MARGIN_LOW is also limited by the values of VOUT_MAX, VOUT_MIN, VOUT_COMMAND, VOUT_SCALE_LOOP and VREF_TRIM. See VOUT_MAX and VOUT_MIN for additional details.

The EA_REF voltage transition occurs at the rate determined by the current state:

- Soft-Start: TON_RISE command
- Steady-State: VOUT_TRANSITION_RATE command
- TOFF_DELAY: VOUT_TRANSITION_RATE command
- Soft-Stop: TOFF_FALL command

COMMAND	STEP_VREF_MARGIN_LOW															
Format	Linear, two's complement binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r/w	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	High Byte								Low Byte							

High Byte:

default: 1111 1111 (binary) (MSB is sign bit, sign extended)

Low Byte:

Minimum: 1100 0000 (binary) –64 (decimal) (–125 mV)

Maximum: 1111 1111 (binary) –1 (decimal) (–2 mV)

The read-writeable bits in this register do NOT have direct EEPROM backup; however, the register does restore to one of two configurable values as determined by RSMLO_VAL in (E5h) MFR_SPECIFIC_21 (OPTIONS).

- RSMLO_VAL = 0: STEP_VREF_MARGIN_LOW will restore to fff7h (–9 decimal or –17.6 mV)
- RSMLO_VAL = 1: STEP_VREF_MARGIN_LOW will restore to fff1h (–15 decimal or –29.3 mV)

7.5.52 PCT_OV_UV_WRN_FLT_LIMITS (MFR_SPECIFIC_07) (D7h)

The PCT_OV_UV_WRN_FLT_LIMITS command is used to set the PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) limits as a percentage of nominal.

For loop slave device, this command cannot be accessed. Any writes to this command will be ignored. An attempt to read or write this command will result in a NACK'd command, the reporting of an IVC fault, and triggering of SMB_ALERT.

The PCT_OV_UV_WRN_FLT_LIMITS takes a one byte data formatted as shown below:

COMMAND	PCT_OV_UV_WRN_FLT_LIMITS							
Format	Unsigned binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w^{E}	r/w^{E}
Function	X	X	X	X	X	X	PCT_MSB	PCT_LSB
Default Value	0	0	0	0	0	0	0	0

The PGOOD, VOUT_UNDER_VOLTAGE (UV) and VOUT_OVER_VOLTAGE (OV) settings are shown in Table 16, as a percentage of nominal reference voltage on the FB pin.

Table 16. OV/UV Protection Settings (Typical Values)

PCT_MSB	PCT_LSB	UV FAULT	UV WARN	OV WARN	OV FAULT	UNIT
0	0	–83%	–88%	112%	117%	EA_REF
0	1	–88%	–90%	110%	112%	EA_REF
1	0	–72%	–78%	112%	117%	EA_REF
1	1	–58%	–64%	112%	117%	EA_REF

The PGOOD pin may trip if the output voltage is too high (using OV WARN) or too low (using UV WARN). Additionally, the PGOOD pin has hysteresis. When the OV WARN output voltage OV WARN is tripped, the FB voltage must lower below the 105% of EA_REF, before PGOOD is reset. Likewise, when output voltage UV WARN is tripped, the FB voltage must rise above 95% of EA_REF, before PGOOD is reset.

7.5.53 OPTIONS (MFR_SPECIFIC_21) (E5h)

The OPTIONS register can be used for setting user selectable options, as shown below. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

COMMAND	OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w	r/w^{E}	r/w^{E}	r/w^{E}	r/w^{E}	r/w	r/w	r/w^{E}	r/w^{E}	r/w^{E}
Function	X	RSMHI_VAL	RSMLO_VAL	x	RST_VOUT_oSD	x	READ_VOUT_RANGE[1:0]		EN_AUTO_ARA	AVG_PROG[1:0]		DLO	VSM	EN_ADC_CNTL	EN_RESET_B	DIS_NEGILIM
Default Value	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0

7.5.53.1 DIS_NEGILIM Bit

When set, this bit disables the negative current limit protection on the LFET.

7.5.53.2 EN_RESET_B Bit

When set, this bit enables the RESET_B functionality of the $\overline{\text{RESET}}$/PGD pin.

BIT VALUE	ACTION
0	$\overline{\text{RESET}}$/PGD pin = PGOOD
1	$\overline{\text{RESET}}$/PGD pin = RESET_B

7.5.53.3 EN_ADC_CNTL Bit

This bit enables ADC operation used for voltage, current and temperature monitoring.

BIT VALUE	ACTION
0	Disable ADC operation
1	Enable ADC operation

NOTE

The EN_ADC_CNTL bit must be set to enable output voltage, current and temperature telemetry. When the EN_ADC_CNTL bit is zero, the READ_VOUT, READ_IOUT and READ_TEMPERATURE_2 registers do not update continuously, and retain the previous values from the last time EN_ADC_CNTL was set.

7.5.53.4 VSM Bit

This bit configures the measurement system for fast, V_{OUT}-only measurement mode. Setting this bit disables READ_IOUT, and READ_TEMPERATURE_1, and instead allows the device to update READ_VOUT more frequently. This bit does not have EEPROM backup.

BIT VALUE	ACTION
0	Measure V_{OUT}, temperature, and I_{OUT}
1	Measure only V_{OUT}

NOTE

For READ_VOUT, multiple samples (defined by AVG_PROG[1:0] Bits) are obtained and averaged. When entering and exiting VSM mode, the first calculated result could lose one sample, for example, 7 sampled value but averaged by 8, resulting the first updated READ_VOUT data point have worst case error about 1/8 of the nominal value.

7.5.53.5 DLO Bit

This bit allows bypassing the normal valid data checks on register writes. This feature is included for flexibility during debug to quickly generate fault conditions and/or possibly work around any data limit protection mechanisms prohibiting output voltage programming. This bit does not have EEPROM backup.

BIT VALUE	ACTION
0	Normal PMBus data write restrictions
1	Data write restrictions are overridden for the following registers: SMBALERT_MASK, VOUT_COMMAND, VOUT_SCALE_LOOP, VREF_TRIM, STEP_VREF_MARGIN_HIGH, STEP_VREF_MARGIN_LOW, IOUT_OC_FAULT_LIMIT, IOUT_OC_WARN_LIMIT, OT_FAULT_LIMIT, OT_WARN_LIMIT, VOUT_MIN, VOUT_MAX, VIN_ON, VIN_OFF, and OPERATION.

NOTE

CAUTION: Users should use this bit with extreme caution. Setting this bit allows invalid data conditions to be programmed into the device which can lead to damage. Invalid data written into any register when DLO is enabled does NOT set the IVD bit; nor trigger SMBALERT. The invalid data is simply allowed to be programmed. Furthermore, invalid data programmed into a command/status register while DLO is enabled, does not trigger SMBALERT upon deassertion of DLO. So, it is possible to exit DLO mode with invalid data in command/status registers. Use with extreme caution.

7.5.53.6 AVG_PROG[1:0] Bits

These bits configure programmable digital measurement averaging. Bits provide programmable averaging for current (READ_IOUT), temperature (READ_TEMPERATURE_1), and voltage (READ_VOUT). The default (00b) yields 16x averaging for all three parameters; however, this default can be changed and stored in EEPROM, if necessary. The programming options are as follows:

BIT VALUE	ACTION
00	Accumulating Averaging = 16x
01	Accumulating Averaging = 0x. Use this setting to bypass the averagers. Every sample from measurement system updates corresponding READ_XXX CSR.
10	Accumulating Averaging = 8x
11	Accumulating Averaging = 32x

7.5.53.7 EN_AUTO_ARA Bit

This bit enables auto-alert response address response. When this feature is enabled, and after the device has successfully responded to an ARA transaction, the hardware automatically masks any fault source currently set from reasserting SMBALERT. This prevents PMBus *bus hogging* in the case of a persistent fault in a device that consistently wins ARA arbitration because of the device address. In contrast, when this bit is cleared, immediate reassertion of SMBALERT is allowed in the event of a persistent fault and the responsibility is upon the host to mask each source individually.

7.5.53.8 READ_VOUT_RANGE[1:0] Bits

The ADC input voltage range is limited to 0.9 V. For READ_VOUT, the output voltage is divided down before input to ADC. Large signal amplitude gives better signal-to-noise ratio. The READ_VOUT_RANGE[1:0] bits are used to force the input voltage divider of the internal ADC for output voltage measurement to one of the 3 possible values.

VOUT_SCALE_LOOP	READ_VOUT_RANGE[1:0]	OUT
1	00b	1/2 IN
x	11b	
0.5	00b	1/4 IN
x	10b	
0.25	00b	1/8 IN
x	01b	

7.5.53.9 RST_VOUT_oSD Bit

When set high, this bit is used to force VOUT_COMMAND to the default value upon any shutdown or fault condition:

- FAULT with programmed shutdown response
- FAULT with programmed restart response
- Normal, controlled shutdown (e.g. CNTL pin)
- LOW_VIN

7.5.53.10 RSMLO_VAL Bit

The restore step-margin low-value (RSMLO_VAL) bit is used to configure the default restore value for (D6h) MFR_SPECIFIC_06 (STEP_VREF_MARGIN_LOW).

BIT VALUE	ACTION
0	STEP_VREF_MARGIN_LOW will restore to fff7h (–9 decimal or –17.6 mV)
1	STEP_VREF_MARGIN_LOW will restore to fff1h (–15 decimal or –29.3 mV)

7.5.53.11 RSMHI_VAL Bit

This restore step margin high value (RSMHI_VAL) bit is used to configure the default restore value for (D5h) MFR_SPECIFIC_05 (STEP_VREF_MARGIN_HIGH).

BIT VALUE	ACTION
0	STEP_VREF_MARGIN_HIGH will restore to 0009h (9 decimal or 17.6 mV)
1	STEP_VREF_MARGIN_HIGH will restore to 000fh (15 decimal or 29.3 mV)

7.5.54 MISC_CONFIG_OPTIONS (MFR_SPECIFIC_32) (F0h)

This user-accessible register is used for miscellaneous options, as shown below. The contents of this register can be stored to nonvolatile memory using the STORE_DEFAULT_ALL command.

COMMAND	MISC_CONFIG_OPTIONS															
Format	Unsigned binary															
Bit Position	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w^E	r/w^E	r/w^E	r	r/w^E	r	r/w^E	r/w^E	r/w^E
Function	X	X	X	X	X	X	X	SYNC_FAULT_DIS	FORCE_SYNC_IN	FORCE_SYNC_OUT	X	EN_AVS_USER	X	HSOC_USER_TRIM[1:0]		OV_RESP_SEL
Default Value	0	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1

7.5.54.1 OV_RESP_SEL Bit

This bit selects between two options for low-side FET behavior after an output overvoltage fault condition. Regardless of the setting of this bit, the low-side FET latches on when an output OV fault is detected (if the OV_FAULT_RESPONSE is not programmed to *ignore*).

BIT VALUE	ACTION
0	The low-side FET remains on until either the part initiates a new startup of the output voltage or the CLEAR_FAULTS command is given while the part is in the *DISABLE* operational state
1	The low-side FET turns off as soon as the sensed output (at FB pin) drops below 0.2 V.

7.5.54.2 HSOC_USER_TRIM[1:0] Bits

These trim bits are provided so the user can adjust the HSOC threshold to account for the application-specific requirements for input-voltage sensing parasitics and component-current handling. The bit settings are defined as follows:

BIT VALUE	ACTION
00	HSOC change from default = 0
01	HSOC change from default = 12.5%
10	HSOC change from default = –25%
11	HSOC change from default = –12.5%

7.5.54.3 EN_AVS_USER Bit

Setting this bit high is required enabling the COMP-level shifter that eliminates overshoot and undershoot of V_{OUT} when the reference is ramped. The value of this bit is latched when the driver is enabled to switch which prevents the user from enabling or disabling the level shifter while the output is switching.

7.5.54.4 FORCE_SYNC_OUT Bit

This bit forces the device to output the free-running clock on the SYNC pin.

7.5.54.5 FORCE_SYNC_IN Bit

This bit forces the device to be synchronized to an external PWM clock applied on the SYNC pin.

7.5.54.6 SYNC_FAULT_DIS Bit

When set, this bit disables any reporting (digital status) and response (analog and digital) to SYNC_FAULT.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

The TPSM846C23 is a highly integrated, synchronous step-down DC-DC power module that supports PMBus commands. The TPSM846C23 converts a higher DC-input voltage to a lower DC-output voltage, with a maximum output current of 35 A. Use the following design procedure to select key component values and set the appropriate behavioral options through the PMBus.

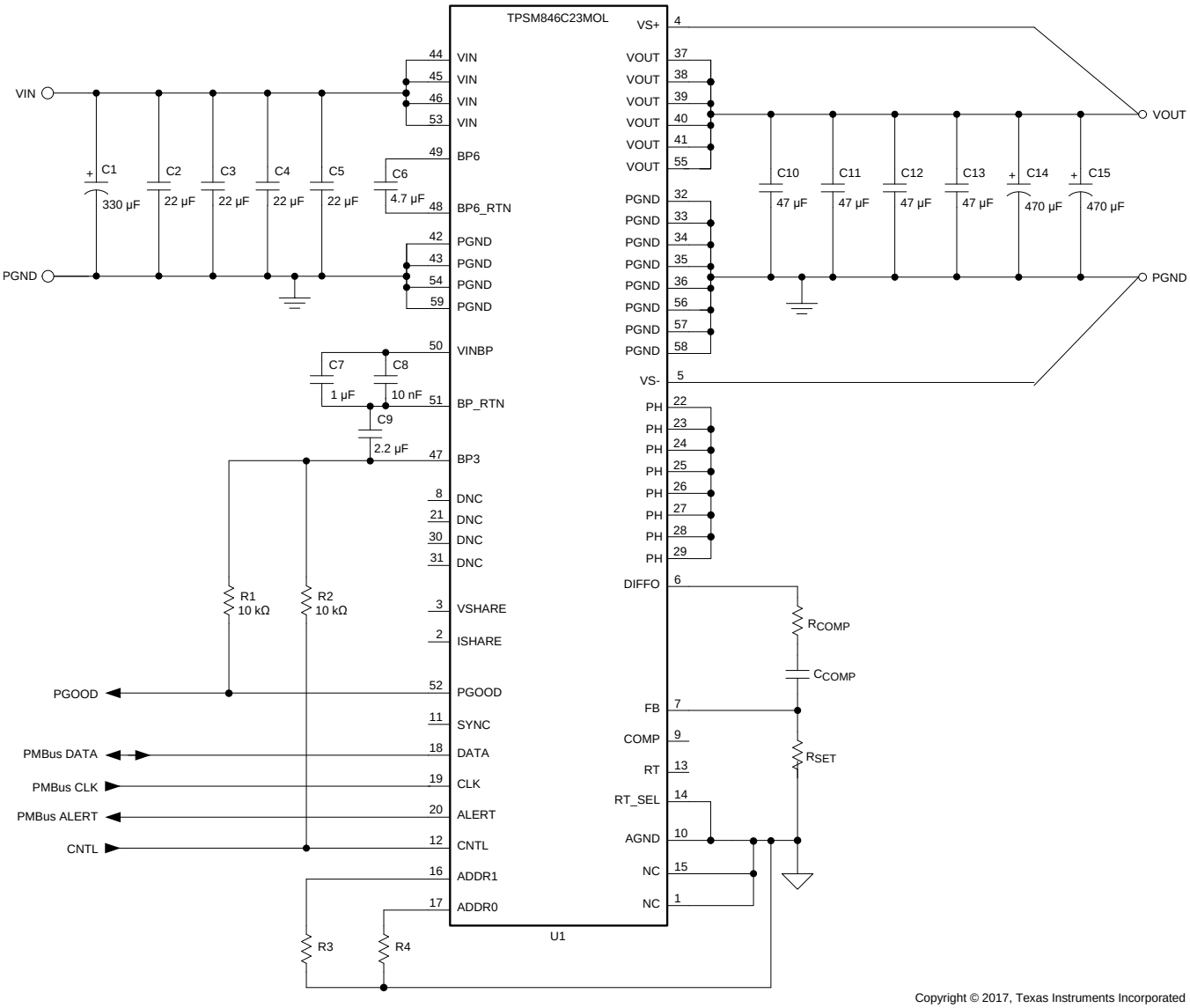


Figure 19. Typical Application Schematic

Typical Application (continued)

8.1.1 Design Requirements

For this design example, use the parameters listed in Table 17 and follow the *Detailed Design Procedure*.

Table 17. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	12 V typical
Output voltage V_{OUT}	1.2 V
Output current rating	35 A
Key care-abouts	PMBus control, small footprint, high efficiency, PGOOD signal

8.1.2 Detailed Design Procedure

8.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM846C23 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.1.2.2 Setting the Output Voltage

The output voltage of the TPSM846C23 is designed to be set via the PMBus using the VOUT_COMMAND (21h).

$$\text{VOUT\_COMMAND value} = (\text{desired } V_{OUT} \times 512) \quad (15)$$

To set the output voltage to 1.2 V, using Equation 15, the calculated VOUT_COMMAND value is 614, which converted to hex is 266h. This value can be written to RAM using the VOUT_COMMAND and saved as the new default value to non-volatile memory using the STORE_DEFAULT_ALL command.

The actual output voltage is also dependant on the value of VOUT_SCALE_LOOP (29h) and the presence of a resistor, R_{SET}. Because the desired output voltage is between 0.35 V and 1.65 V (VOUT_SCALE_LOOP = 1), the R_{SET} resistor must be left open.

8.1.2.3 Input and Output Capacitance

The minimum required input capacitance network consists of four 22-µF (or two 47-µF) ceramic capacitors plus a 330-µF bulk capacitor. The minimum required output capacitance network consists of four 47-µF (or two 100-µF) ceramic capacitors plus two 470-µF, low ESR polymer capacitors. The combined ESR of the polymer capacitors must not be greater than 5 mΩ. Additional input and output capacitors can be added to improve ripple or transient response.

In this design example, the minimum required input and output capacitance is used.

8.1.2.4 Selecting the Compensation Components

The TPSM846C23 requires an external series resistor and capacitor compensation network to be connected between the DIFFO pin (pin 6) and the FB pin (pin 7). The value of these components is determined by the total amount of output capacitance.

In this design example, the value of R_{COMP} and C_{COMP} is selected from Table 3 based on the total amount of output capacitance of 1120 µF. R_{COMP} = 1.0 kΩ and C_{COMP} = 1000 pF.

8.1.2.5 Setting the Switching Frequency

The TPSM846C23 is set to a default switching frequency of 500 kHz. To operate the TPSM846C23 at the default switching frequency, connect the RT_SEL pin (pin 14) to AGND and the RT pin (pin 13) must be left open.

In this design example, the switching frequency is selected to operate at the default switching frequency of 500 kHz by connecting RT_SEL pin to AGND, and the R_{RT} resistor is left open.

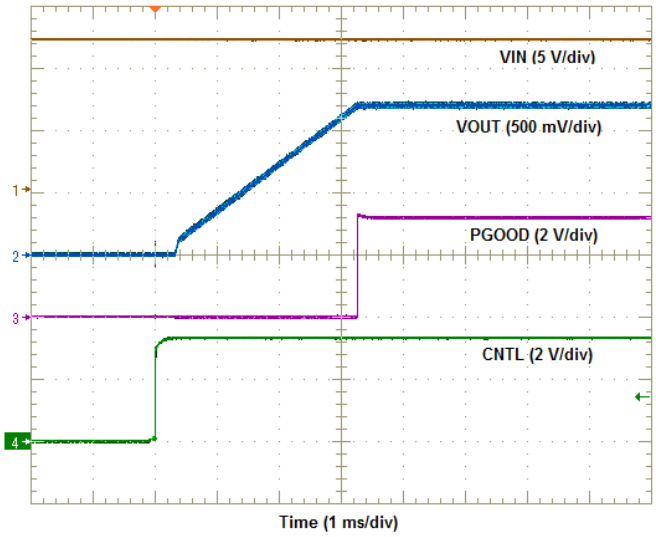
8.1.2.6 Power Good (PGOOD)

Applications requiring voltage rail sequencing can benefit from the PGOOD signal present with the TPSM846C23. The PGOOD pin is an open-drain output. When the output voltage is typically between 95% and 105% of the setpoint, the PGOOD pin pulldown is released, and the pin floats, requiring an external pullup resistor for a high signal. A 10-kΩ pullup resistor is placed between the PGOOD pin and the BP3 rail.

8.1.2.7 ON/OFF Control (CNTL)

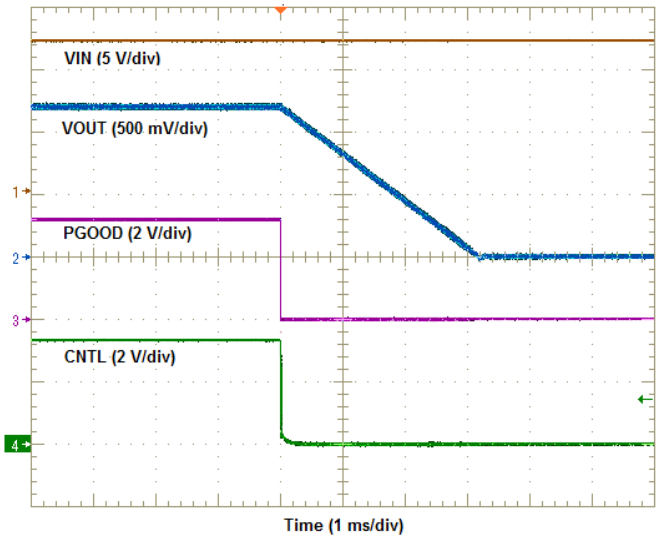
The CNTL signal is an input signal on the PMBus. It is used to turn the power conversion function of the module on and off in conjunction with commands received over the bus. It can be configured as an active high or active low signal through the ON_OFF_CONFIG command. The CNTL signal is programmed at the factory to be an active high signal; that is, the CNTL pin must be pulled high for power conversion to occur. The CNTL pin requires an external pullup resistor for a high signal. A 10-kΩ pullup resistor is placed between the CNTL pin and the BP3 rail.

8.1.3 Application Curves



V_{IN} = 12 V V_{OUT} = 1.2 V I_{OUT} = 10 A

Figure 20. Start-up Waveforms



V_{IN} = 12 V V_{OUT} = 1.2 V I_{OUT} = 10 A

Figure 21. Shutdown Waveform

9 Power Supply Recommendations

The TPSM846C23 device is designed to operate from an input voltage supply between 4.5 V and 15 V. This supply must be well regulated. These devices are not designed for split-rail operation. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in *Layout*.

10 Layout

10.1 Layout Guidelines

Layout is critical for good power-supply design. Figure 22 and Figure 23 show top-side and bottom-side PCB-layout configuration for recommended component placement. Additional power, ground and signal layers are present in any PCB design. A list of PCB layout considerations using these devices is listed as follows:

- Place the input bypass capacitors as close as physically possible to the VIN and PGND pins. Additionally, a high-frequency bypass capacitor on the VIN pins can help reduce switching spikes. Place this capacitor on the bottom side of the PCB directly underneath the device to keep a minimum loop.
- The BP6 bypass capacitor carries a large switching current for the gate driver. Bypassing the BP6 pin to BP6_RTN with a low-impedance path is very critical to the stable operation of the TPSM846C23 device. Place the BP6 high-frequency bypass capacitor as close as possible to the device pins 48 and 49.
- The VINBP and BP3 pins also require good local bypassing. Place bypass capacitors as close as possible to the device pins and BP_RTN. Poor bypassing on the VINBP and BP3 pins can degrade the performance of the device.
- Place signal components as close as possible to the pins to which they are connected. These components include the feedback resistors and the RT resistor. Keep these components from fast switching voltage and current paths. Terminate these components to AGND with a minimum return loop.
- Route the VS+ and VS– lines from the output capacitor bank at the load back to the device pins as a tightly coupled differential pair. These traces must be kept away from switching or noisy areas which can add differential-mode noise.
- Use caution when routing of the SYNC, VSHARE and ISHARE traces for parallel configurations. The SYNC trace carries a rail-to-rail signal and must be routed away from sensitive analog signals, including the VSHARE, ISHARE, RT, and FB signals. The VSHARE and ISHARE traces must also be kept away from fast switching voltages or currents formed by the VIN, PH, and BP6 pins.

10.2 Layout Example

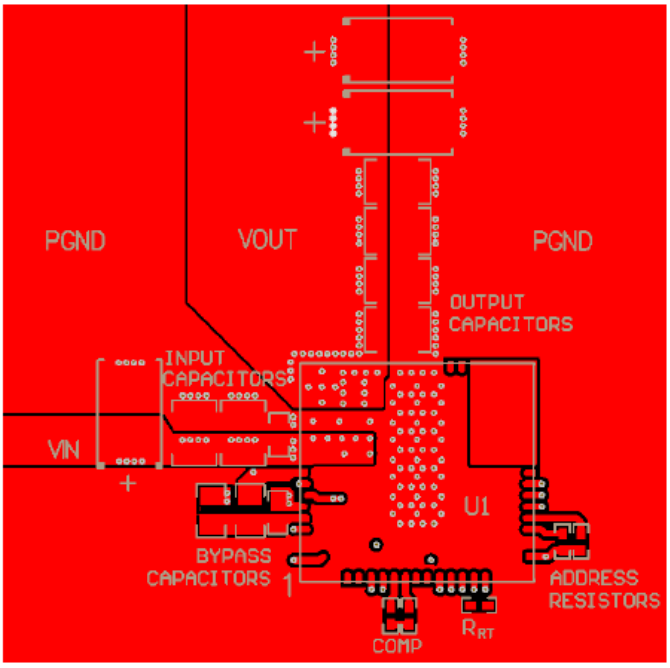


Figure 22. PCB Top-side Layout Recommendation

Layout Example (continued)

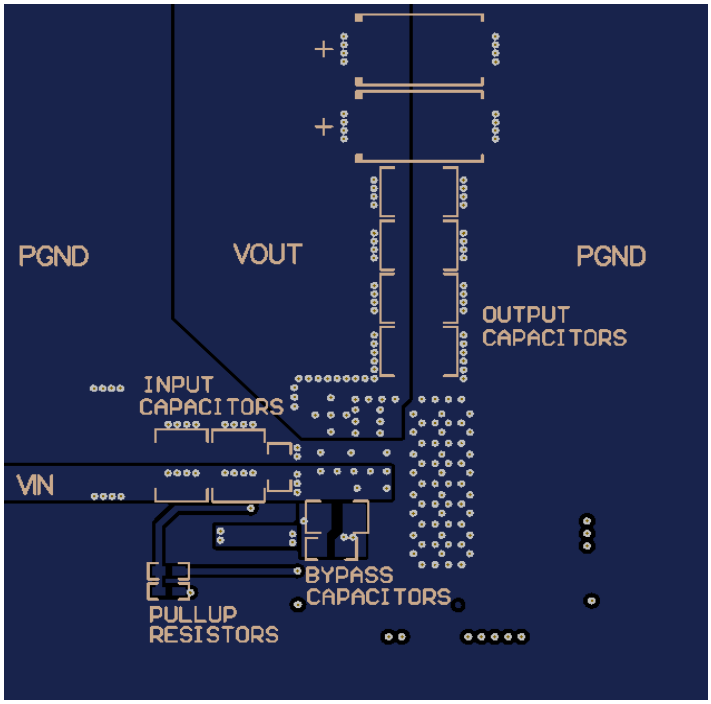


Figure 23. PCB Bottom-side Layout Recommendation

10.3 Package Specifications

TPSM846C23		VALUE	UNIT
Weight		3.92	grams
Flammability	Meets UL 94 V-O		
MTBF Calculated Reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	26.6	MHrs

10.4 EMI

The TPSM846C23 is compliant with EN55022 Class A radiated emissions. Figure 24 to Figure 27 show typical examples of radiated emissions plots for the TPSM846C23. The EMI plots were taken using the TPSM846C23 EVM with a resistive load and input power was provided using a lead acid battery. All graphs show plots of the antenna in the horizontal and vertical positions.

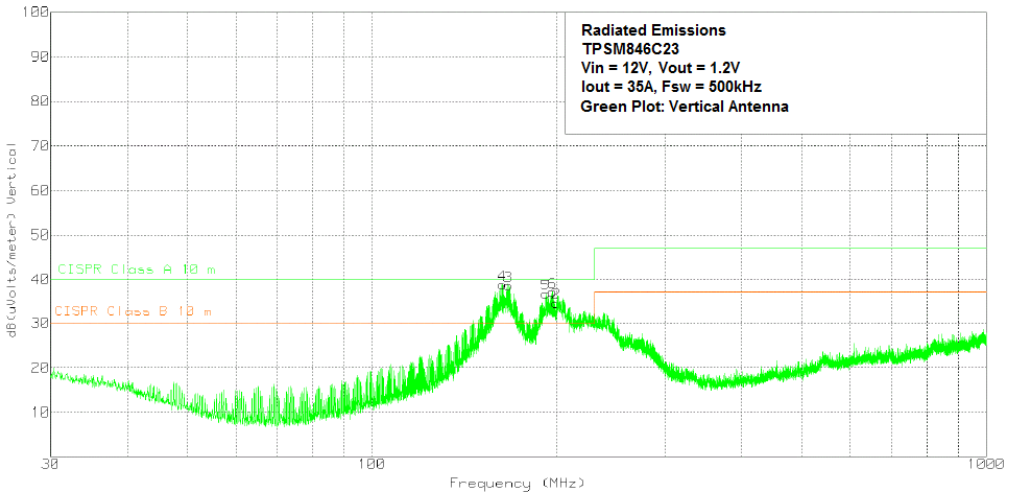


Figure 24. Radiated Emissions 12-V Input, 1.2-V Output, 35-A Load Vertical Antenna

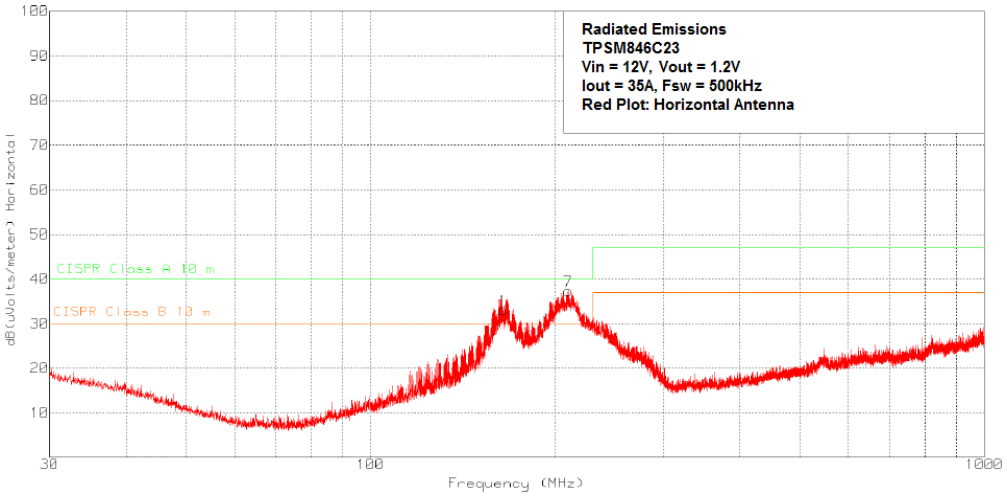


Figure 25. Radiated Emissions 12-V Input, 1.2-V Output, 35-A Load Horizontal Antenna

EMI (continued)

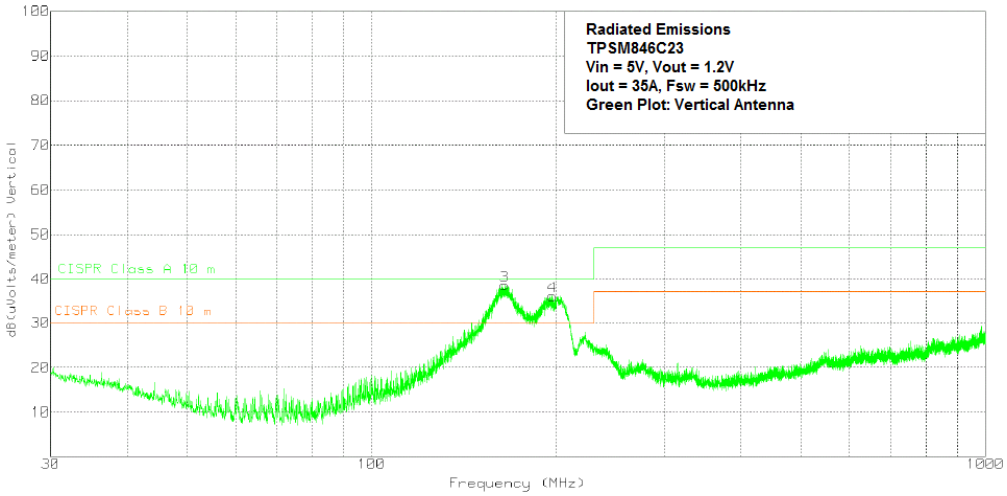


Figure 26. Radiated Emissions 5-V Input, 1.2-V Output, 35-A Load Vertical Antenna

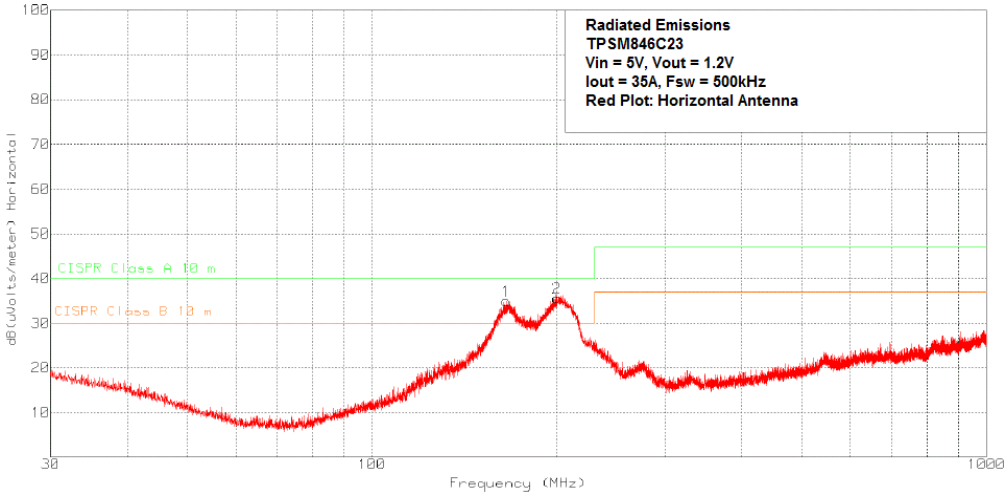


Figure 27. Radiated Emissions 5-V Input, 1.2-V Output, 35-A Load Horizontal Antenna

10.5 Mounting and Thermal Profile Recommendation

Proper mounting technique adequately covers the exposed thermal pad with solder. Excessive heat during the reflow process can affect electrical performance. Figure 28 shows the recommended reflow-oven thermal profile. Proper post-assembly cleaning is also critical to device performance. Refer to *Power Module MSL Ratings and Reflow Ratings* for more information.

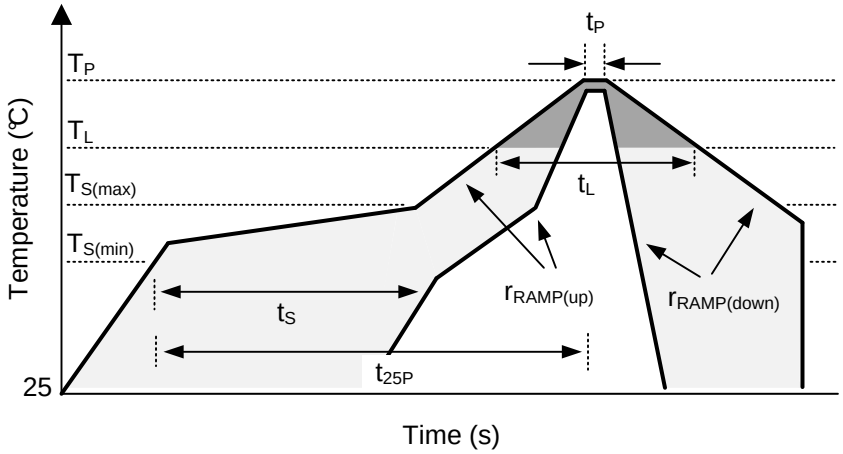


Figure 28. Recommended Reflow-Oven Thermal Profile

Table 18. Recommended Thermal Profile Parameters

PARAMETER		MIN	TYP	MAX	UNIT
RAMP UP AND RAMP DOWN					
$r_{RAMP(up)}$	Average ramp-up rate, $T_{S(max)}$ to T_P			3	°C/s
$r_{RAMP(down)}$	Average ramp-down rate, T_P to $T_{S(max)}$			6	°C/s
PRE-HEAT					
T_S	Preheat temperature	150		200	°C
t_S	Preheat time, $T_{S(min)}$ to $T_{S(max)}$	60		120	s
REFLOW					
T_L	Liquidous temperature		217		°C
T_P	Peak temperature			260	°C
t_L	Time maintained above liquidous temperature, T_L	60		150	s
t_P	Time maintained within 5°C of peak temperature, T_P	20		30	s
t_{25P}	Total time from 25°C to peak temperature, T_P			480	s

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM846C23 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *PMB Power Management Protocol Specification, Part 1, revision 1.3* available at http://pmbus.org
- TI User Guide *Operating TPSM846C23 in Parallel*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
PMBus is a trademark of SMIF, Inc..
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

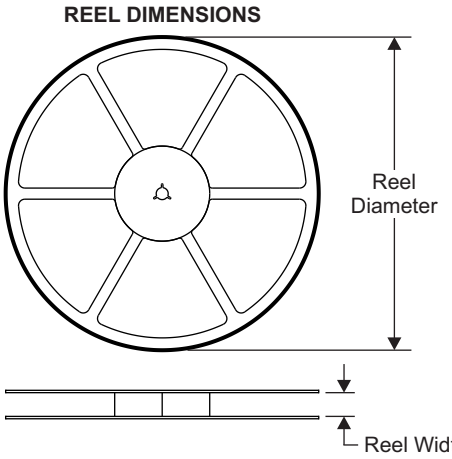
SLYZ022 — *TI Glossary*.

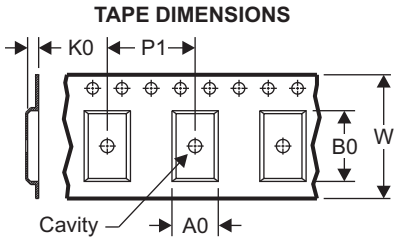
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

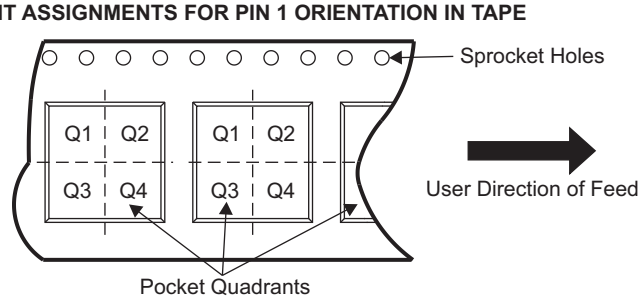
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information



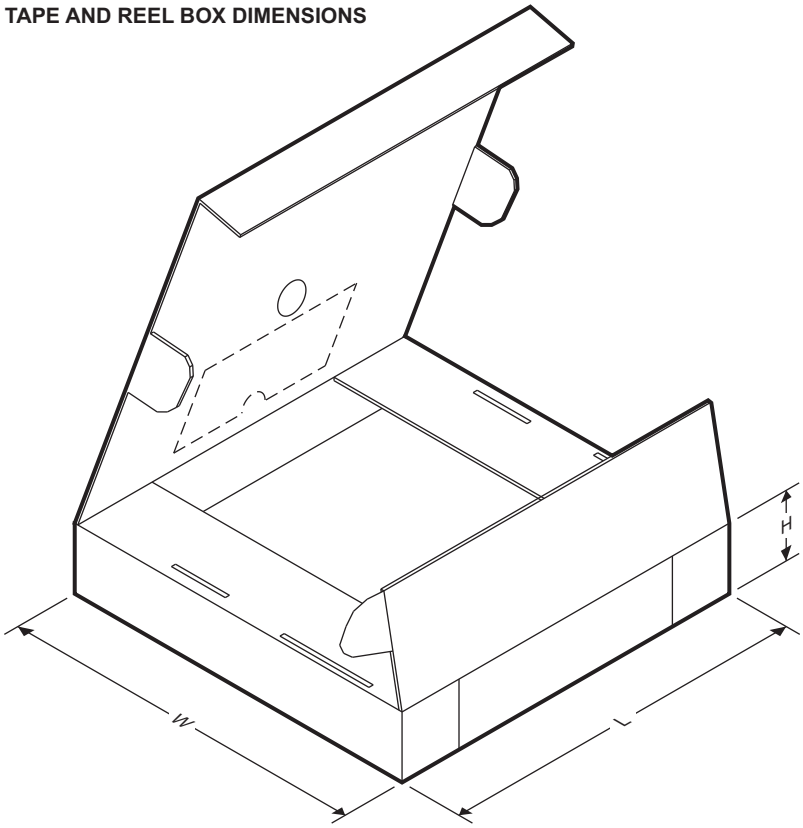


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM846C23MOLR	QFM	MOL	59	350	330.0	32.4	15.35	16.35	6.1	24.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM846C23MOLR	QFM	MOL	59	350	383.0	353.0	58.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM846C23MOLR	ACTIVE	QFM	MOL	59	350	RoHS Exempt & Green	NIAU	Level-3-260C-168 HR	-40 to 105	TPSM846C23	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

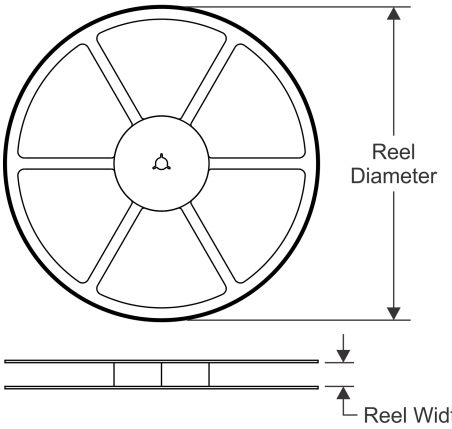
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

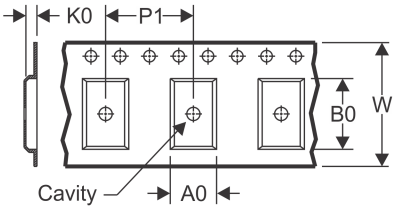
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

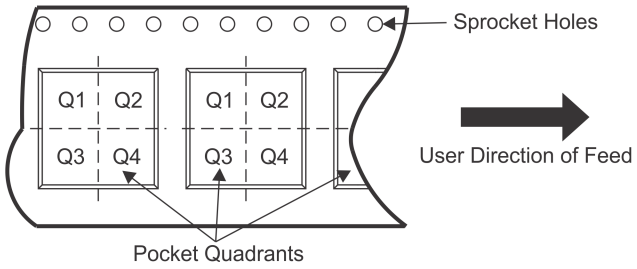


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

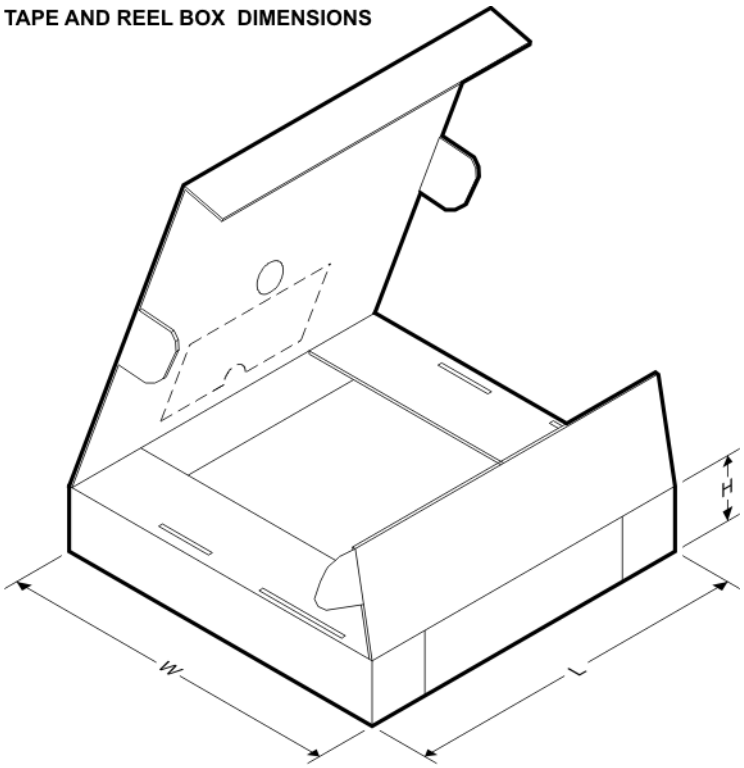
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM846C23MOLR	QFM	MOL	59	350	330.0	32.4	15.35	16.35	6.1	24.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

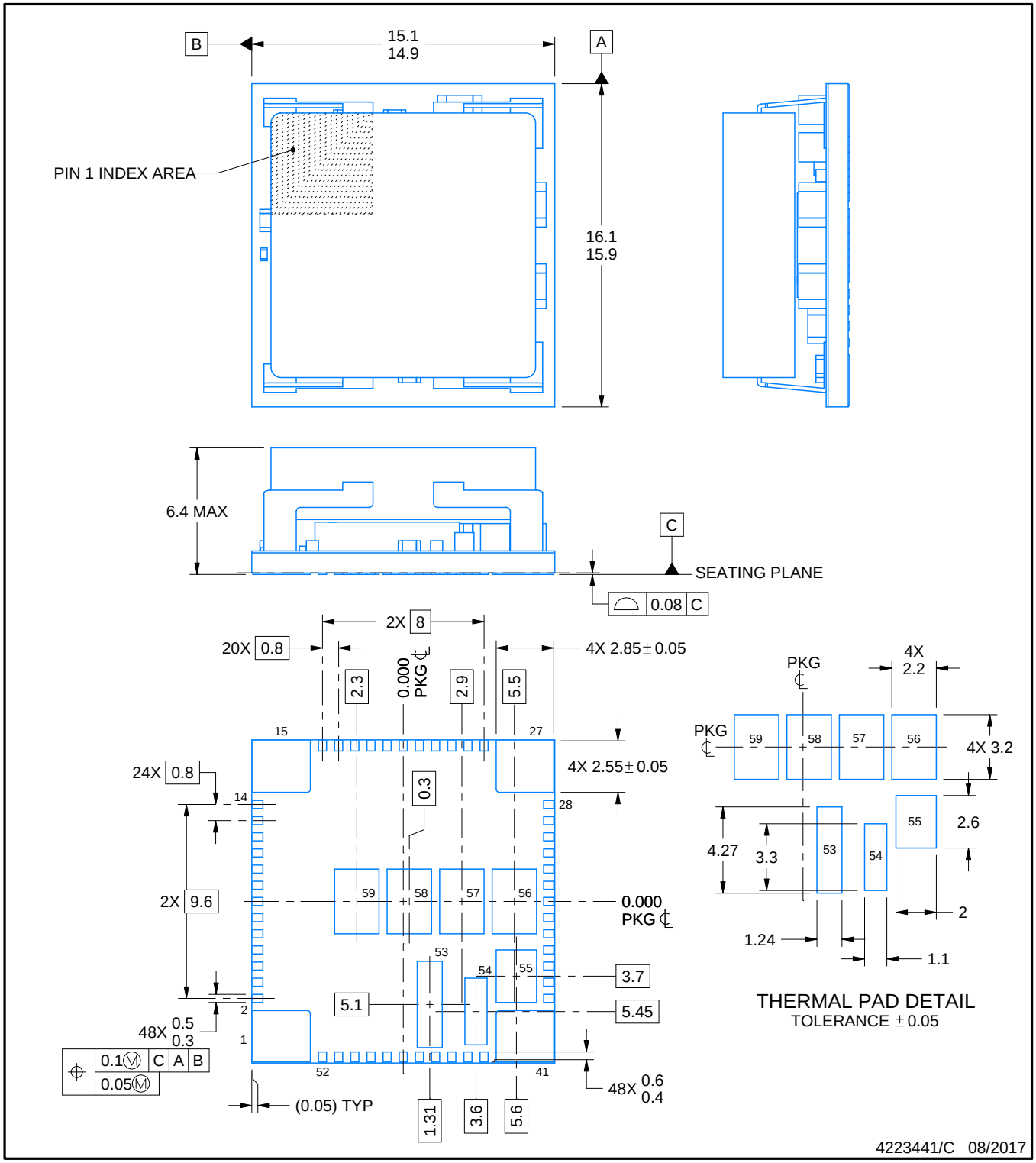
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM846C23MOLR	QFM	MOL	59	350	383.0	353.0	58.0

MOL0059A

PACKAGE OUTLINE

QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE



NOTES:

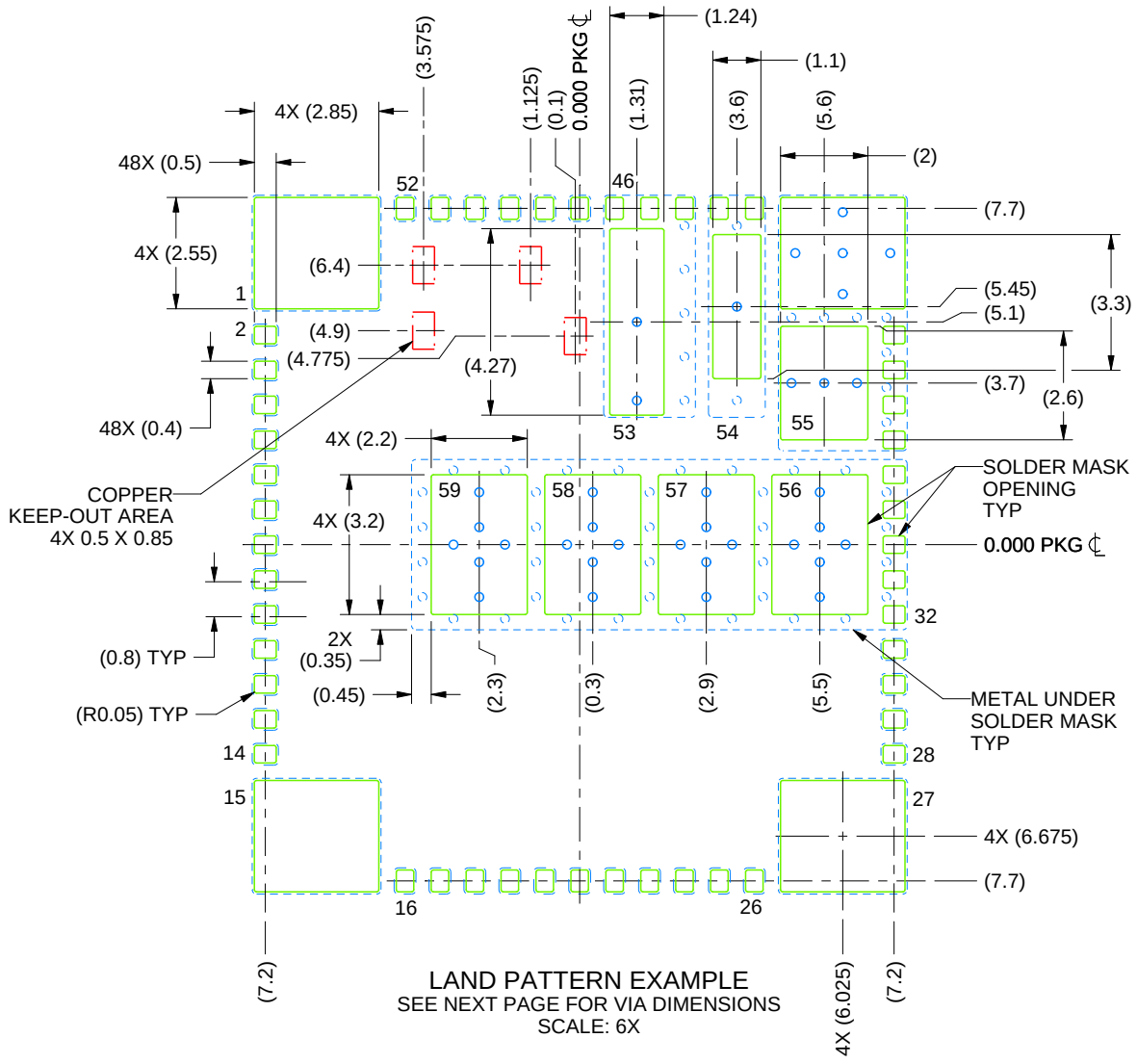
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

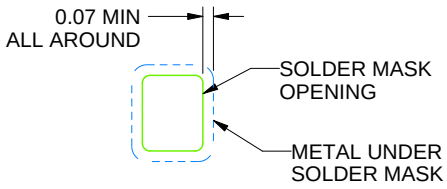
MOL0059A

QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE



LAND PATTERN EXAMPLE
SEE NEXT PAGE FOR VIA DIMENSIONS
SCALE: 6X



SOLDER MASK DETAILS
SOLDER MASK DEFINED PADS

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NOTES: (continued)

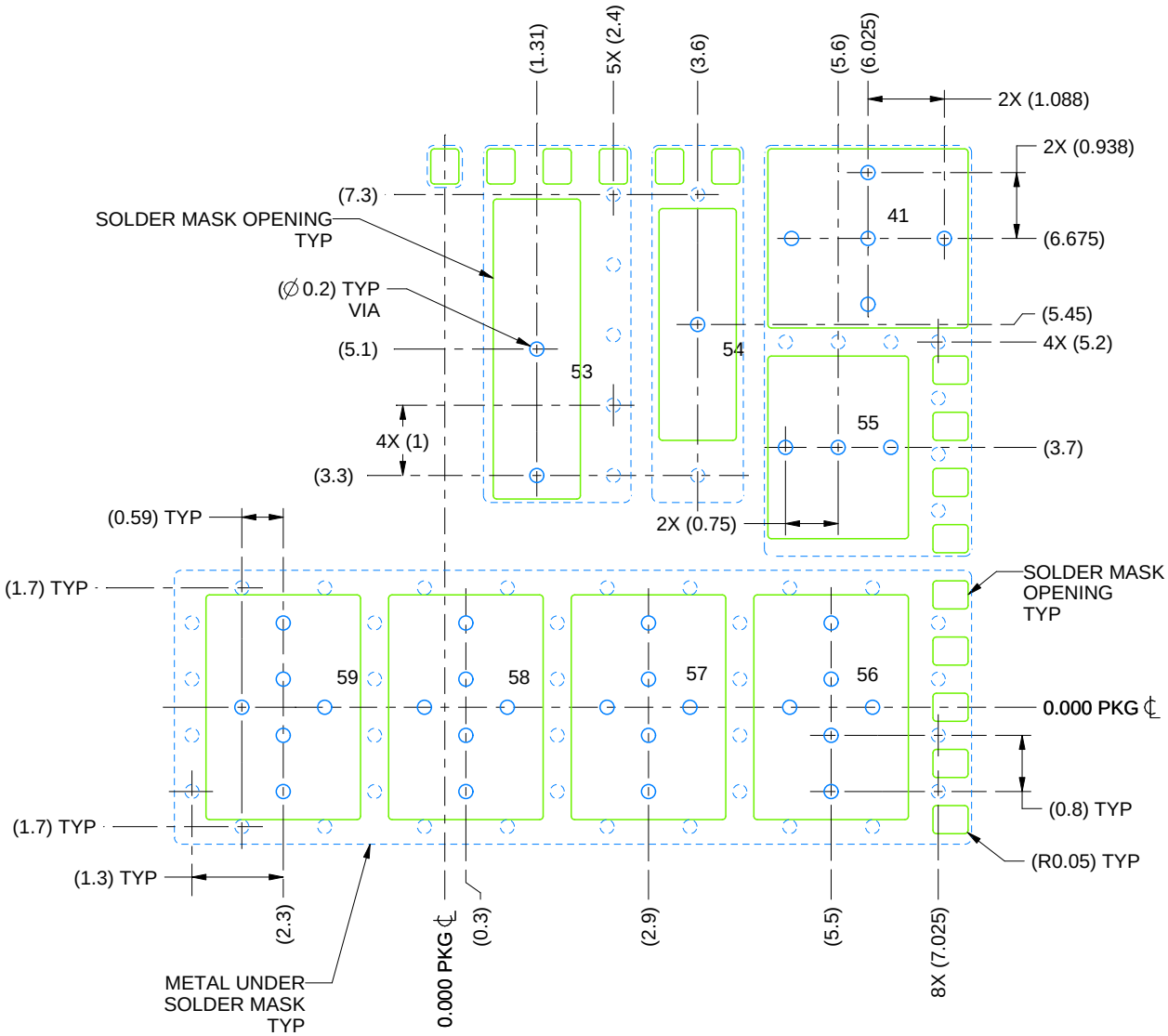
4. This package is designed to be soldered to the thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE BOARD LAYOUT

MOL0059A

QFM - 6.4 mm max height

PLASTIC QUAD FLAT MODULE



LAND PATTERN EXAMPLE
VIA DETAIL
SCALE: 10X

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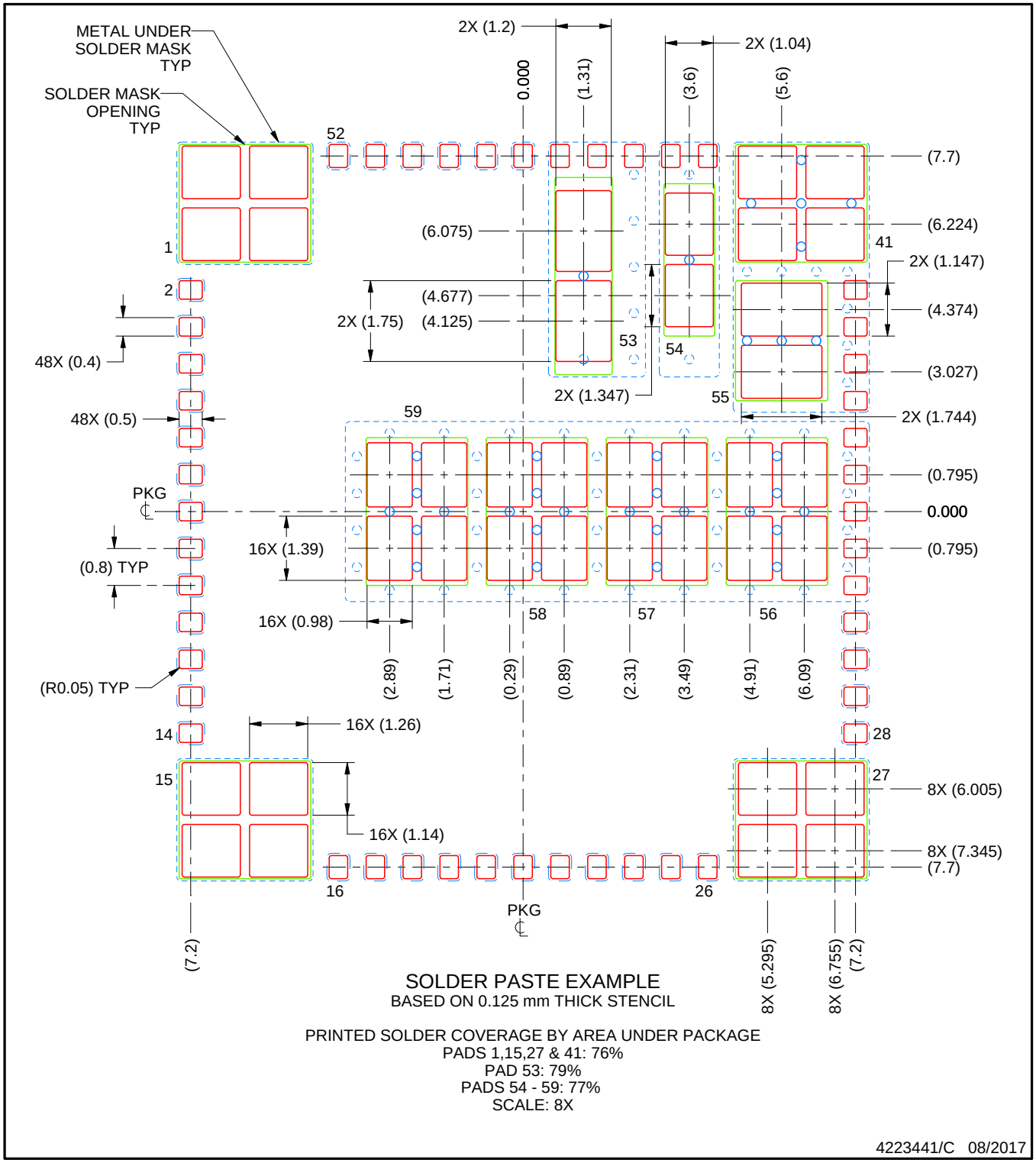

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,15,27 & 41: 76%
PAD 53: 79%
PADS 54 - 59: 77%
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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