Keywords: T1, E1, LIU, line interface unit, octal, short haul

APPLICATION NOTE 3916

# DS26303 Short-Haul Line Interface Unit vs. IDT82V2048

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*Abstract: This document provides an explanation of the differences between the DS26303 and the IDT82V2048 with emphasis on the information required to use the DS26303 in an existing IDT82V2048 application. Descriptions of the feature differences, register considerations, and hardware considerations are provided.*

## Introduction

This document provides an explanation of the differences between the DS26303 and the IDT82V2048 with emphasis on the information required to use the DS26303 in an existing IDT82V2048 application. The DS26303 is an 8-channel short-haul line interface unit (LIU) that supports E1/T1/J1 from a single 3.3V power supply. This device supports the functions of the IDT82V2048 without software modification, while providing additional features. The DS26303 can be used in an existing IDT82V2048 application without changing PCB layout, but by simply replacing external component values for the desired application.

Descriptions of the feature differences are provided in three separate sections. **Table 1** provides a list of DS26303 features not present in the IDT82V2048. **Table 2** gives a list of IDT82V2048 features not present in the DS26303. **Table 3** provides a list of features present in both the DS26303 and IDT82V2048 that are not implemented the same on both devices.

The differences between registers of the DS26303 and IDT82V2048 are described in **Tables 6** through **10**, along with the additional functionality provided by additional register banks of the DS26303. **Figure 1** and **Table 11** provide the minor changes in component values required when using the DS26303 in an existing IDT82V2048 application.

**Table 1. DS26303 Features Not Present in IDT82V2048**

| DS26303 | IDT82V2048 |
|---|---|
| Programmable option to clear interrupt status on write or read. Clear on read is default. | Not supported. |
| Individual channel control for jitter attenuator:<br>• Enable/disable<br>• FIFO depth<br>• FIFO limit trip | All channels have global control. |
| Internal software-selectable transmit and receive-side termination for 100Ω T1 twisted-pair, 110Ω J1 twisted-pair, 120Ω E1 twisted-pair, and 75Ω E1 coaxial applications. | Not supported. |
| In HPS mode, the transmitter output and the internal impedance of the receiver can be turned off with only the OE pin. | Requires that both receivers use the same front-end termination. |
| Built in BERT tester for diagnostics. | Not supported. |
| Individual channel control for:<br>• Short-circuit protection<br>• AIS enable on LOS<br>• RCLK inversion<br>• TCLK inversion | All channels have global control. |
| Individual channel-line violation detection. | Not supported. |
| Flexible MCLK See **Table 4** for available input frequencies. | Not supported. |
| Programmable TECLK output pin (1.544MHz or 2.048MHz) | Not supported. |
| Programmable CLKA output pin See **Table 5** for available output frequencies. | Not supported. |
| Flexible interrupt pin | Not supported. |

**Table 2. IDT82V2048 Features Not Present in DS26303**

| DS26303 | IDT82V2048 |
|---|---|
| Uses single optimal value. | Capability to select the jitter attenuator bandwidth. |
| Not provided. | Inband loopack (loopup and loopdown codes). |

**MLCK Pin Functionality**

The DS26303 and IDT82V2048 both require MCLK to for data with clock recovery as well as AIS detection.

The MCLK pin of the IDT82V2048 provides additional functionality not present in the DS26303.

IDT82V2048 MCLK held high.

- The IDT82V2048 slices the incoming bipolar line signal into RZ pulse (data-recovery mode).

IDT82V2048 MCLK held low.

- All the receivers are powered down, and the output pins RCLKn, RDPn, and RDNn are switched to high impedance.

Note that wait state generation through RDY/ACK is not available if MCLK is not provided.

**Table 3. Feature Differences Between DS26303 and IDT82V2048**

| DS26303 | IDT82V2048 |
|---|---|
| 3.3V LIU power only, 5V not provided. | 5V LIU power. |
| Non-mux Intel® write address to WRB rising-edge setup time is 17ns. | Non-mux Intel write address to WRB rising-edge setup time is 6ns. |
| Expects non-mux Intel read address to be valid when RDB is active. | Non-mux Intel read address to RDB rising-edge setup time is 6ns. This might be an error in data sheet because data is out before this setup time. |
| Inactive RDY to tri-state delay time 12ns (max). | Inactive RDY to tri-state delay time 3ns (max). |
| Clears the interrupt pin when reading or writing the interrupt status. | Clear interrupt pin by reading the corresponding status register. |
| Jitter attenuator FIFO depths of 32 bits or 128 bits. | Jitter attenuator FIFO depths of 32 bits or 64 bits. |
| Individual channel control for jitter attenuator:<br>• Enable/disable<br>• FIFO depth<br>• FIFO limit trip | All channels have global control. |

**Table 4. MCLK Selections for the DS26303**

| PLLE | MPS1, MPS0 | MCLK MHz (±50ppm) | FREQS | T1 or E1 Mode |
|---|---|---|---|---|
| 0 | xx | 1.544 | x | T1 |
| 0 | xx | 2.048 | x | E1 |
| 1 | 00 | 1.544 | 1 | T1/J1 or E1 |
| 1 | 01 | 3.088 | 1 | T1/J1 or E1 |
| 1 | 10 | 6.176 | 1 | T1/J1 or E1 |
| 1 | 11 | 12.352 | 1 | T1/J1 or E1 |
| 1 | 00 | 2.048 | 0 | T1/J1 or E1 |
| 1 | 01 | 4.096 | 0 | T1/J1 or E1 |
| 1 | 10 | 8.192 | 0 | T1/J1 or E1 |
| 1 | 11 | 16.384 | 0 | T1/J1 or E1 |

**Table 5. DS26303 Clock A Selections**

| CLKA3 to CLKA0 | MCLK (Hz) |
|---|---|
| 0000 | 2.048M |
| 0001 | 4.096M |
| 0010 | 8.192M |
| 0011 | 16.384M |
| 0100 | 1.544M |
| 0101 | 3.088M |
| 0110 | 6.176M |
| 0111 | 12.352M |
| 1000 | 1.536M |
| 1001 | 3.072M |
| 1010 | 6.144M |
| 1011 | 12.288M |
| 1100 | 32k |
| 1101 | 64k |
| 1110 | 128k |
| 1111 | 256k |

# Register Considerations

The DS26303 contains four major register banks.

- Primary Registers (DS26303 and IDT82V2048)
- Secondary Registers (DS26303 and IDT82V2048)
- Individual LIU Registers (DS26303 only)
- BERT Registers (DS26303 only)

To take advantage of the DS26303's additional features and flexibility, additional code must be added to any original source code written for an IDT82V2048 application. The address pointer control register (ADDP), address 1Fh, is used as a pointer to access the desired register bank. Table 6 provides a list of the DS26303 register banks and the required ADDP value required for access to the desired register bank.

**Table 6. Address Pointer Bank Selection**

| ADDP7 to ADDP0 (Hex) | Bank Name | DS26303 | IDT82V2048 |
|---|---|---|---|
| 00 | Primary Bank | Yes | Yes |
| AA | Secondary Bank | Yes | Yes |
| 01 | Individual LIU Bank | Yes | No |
| 02 | BERT Bank | Yes | No |

The Primary Register Bank of the DS26303 is the same as the IDT82V2048. If the DS26303 is used in the place of an existing IDT82V2048 and only the Primary Register Bank is used, the application software does not require modification. Table 7 provides an overview of the Primary Registers.

**Table 7. Primary Registers DS26303 and IDT82V2048**

| Address (Hex) | DS26303 and IDT82V2048 |
|---|---|
| 00–15 | Primary Registers |
| 16–1E | Reserved |
| 1F | ADDP |

While both the DS26303 and IDT82V2048 provide a Secondary Register Bank, the registers and functionality is not the same for all the registers. Table 8 provides a list of the registers contained in the Secondary Register Bank and their function for the DS26303 and the IDT82V2048.

Two additional register banks are contained in the DS26303: the Individual LIU Register Bank and the BERT Register Bank. Table 9 presents a list of the registers contained in the Individual LIU Register Bank and Table 10 has a list of the registers contained in the BERT Register Bank To take advantage of the DS26303's additional features and flexibility, additional code must be added to any original source code written for an IDT82V2048 application.

**Table 8. Secondary Register Bank of the DS26303**

| Address (Hex) | Register Name | DS26303 | IDT82V2048 |
|---|---|---|---|
| 00 | Single-Rail Mode Select | Yes | Yes |
| 01 | Line-Code Selection | Yes | Yes |
| 02 | Clock-Recovery Enable | No | Yes |
| 03 | Receiver Power-Down Enable | Yes | Yes |
| 04 | Transmitter Power-Down Enable | Yes | Yes |
| 05 | Excessive Zero-Detect Enable | Yes | Yes |
| 06 | Code-Violation-Detect Enable Bar | Yes | Yes |
| 07 | Receive Equalizer Enable | No | Yes |
| 08 | Inband Loopback (LB) Configuration | No | Yes |
| 09 | Inband LB Activation Code | No | Yes |
| 0A | Inband LB Deactivation Code | No | Yes |
| 0B | Inband LB Receive Status | No | Yes |
| 0C | Inband LB Interrupt Mask | No | Yes |
| 0D | Inband LB Interrupt Status | No | Yes |
| 0E | Inband LB Activation/Deactivation Code Generator | No | Yes |
| 1F | Set to AAh for access to Secondary Register Bank | Yes | Yes |

**Table 9. Individual LIU Register Bank of the DS26303**

| Address (Hex) | Register Name |
|---|---|
| 00 | Individual JA Enable |
| 01 | Individual JA Position Select |
| 02 | Individual JA FIFO Depth Select |
| 03 | Individual JA FIFO Limit Trip |
| 04 | Individual Short-Circuit Protection Disable |
| 05 | Individual AIS Select |
| 06 | Master-Clock Select |
| 07 | Global-Management Register |
| 08–0F | Reserved |
| 10 | Bit-Error-Rate Tester Control Register |
| 12 | Line-Violation Detect Status |
| 13 | Receive-Clock Invert |
| 14 | Transmit-Clock Invert |
| 15 | Clock-Control Register |
| 16 | RCLK Disable Upon LOS Register |
| 1E | Global-Interrupt Status Control |
| 1F | Set to 01h for access to Individual LIU Register Bank |

**Table 10. BERT Register Bank of the DS26303**

| Address (Hex) | Register Name |
|---|---|
| 00 | BERT Control Register |
| 01 | Reserved |
| 02 | BERT Pattern Configuration 1 |
| 03 | BERT Pattern Configuration 2 |
| 04 | BERT Seed/Pattern 1 |
| 05 | BERT Seed/Pattern 2 |
| 06 | BERT Seed/Pattern 3 |
| 07 | BERT Seed/Pattern 4 |
| 08 | Transmit-Error Insertion Control |
| 09–0A | Reserved |
| 0C | BERT Status Register |
| 0D | Reserved |
| 0E | BERT Status Register Latched |
| 10 | BERT Status Register Interrupt Enable |
| 11–13 | Reserved |
| 14 | Receive Bit-Error Count Register 1 |
| 15 | Receive Bit-Error Count Register 2 |

| | |
|---|---|
| 16 | Receive Bit-Error Count Register 3 |
| 17 | Receive Bit-Error Count Register 4 |
| 18 | Receive Bit-Count Register 1 |
| 19 | Receive Bit-Count Register 2 |
| 1A | Receive Bit-Count Register 3 |
| 1B | Receive Bit-Count Register 4 |
| 1C–1E | Reserved |
| 1F | Set to 02h for access to BERT Register Bank |

# Hardware Considerations

The DS26303 can replace the IDT82V2048 in an existing application without PCB layout changes. All that is needed is to replace external component values for the desired application. Figure 1 provides the recommended DS26303 network termination circuit, and Table 11 provides the component values required for proper termination of the DS26303.

## Transmitter

The IDT82V2048 requires transmit-side resistors in series with TTIP and TRING outputs. IDT82V2048 recommends that these resistors should be 0Ω (T1 3.3V mode), 9.5Ω (E1 75Ω coaxial), or 9.1Ω (E1 120Ω twisted pair). The DS26303 does not require the resistors, so any present should be 0Ω in all modes.

## Receiver

On the receive side, the IDT82V2048 requires termination resistance of 12.4Ω (T1 3.3V mode), 9.31Ω (E1 75Ω coaxial), or 15Ω (E1 120Ω twisted pair). The DS26303 requires 15Ω termination resistors for all modes when using external impedance mode. If the DS26303's software-selectable impedance-matching mode is used, these resistors are not required. The IDT82V2048 requires 1kΩ resistors in series with the RTIP and RRING pins. If software termination/impedance matching is desired, these 1kΩ resistors should be replaced with 0Ω resistors.

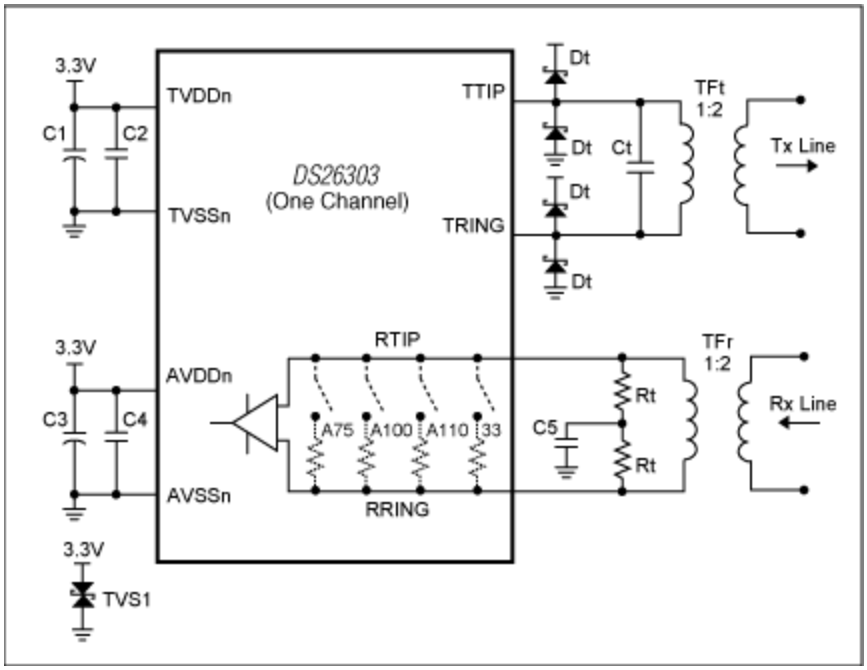


*Figure 1. LIU front-end*

**Table 11. LIU Front-End Values**

| Mode | Component | 75Ω Coaxial | 120Ω Twisted Pair | 100Ω/110Ω Twisted Pair |
|---|---|---|---|---|
| Tx Capacitance | Ct | 560pF (typ). Adjust for board parasitics for optimal return loss. | | |
| Tx Protection | Dt | International Rectifier: 11DQ04 or 10BQ060 Motorola: MBR0540T1 | | |
| Rx Transformer 1:2 | TFr | Pulse: T1124 (0°C to +70°C) | | |
| Tx Transformer 1:2 | TFt | Pulse: T1114 (-40°C to +85°C) | | |
| Tx Decoupling (ATVDD) | C1 | Common decoupling for all eight channels is 68µF. | | |
| Tx Decoupling (ATVDD) | C2 | Recommended decoupling per channel is 0.1µF. | | |
| Rx Decoupling (AVDDn) | C3 | Common decoupling for all eight channels is 68µF. | | |
| Rx Decoupling (AVDDn) | C4 | Common decoupling for all eight channels is 0.1µF. | | |
| Rx Termination | C5 | When in external impedance mode, Rx capacitance for all eight channels is 0.1µF. Do not populate if using internal impedance mode. | | |
| Rx | | When in external impedance mode, the two resistors for all modes shall | | |

| | | |
|---|---|---|
| Termination | Rt | be 15.0Ω ±1%. Do not populate if using internal impedance mode. |
| Voltage Protection | TVS1 | SGS-Thomson: SMLVT 3V3 (3.3V transient suppressor) |

# DS26303 Further Information

For more information about Maxim communication products, please consult the data sheets available on our website at T/E Carrier and Packetized Products. If you have further questions concerning the operation of these communication devices, please contact the Telecommunication Applications support team.



| Related Parts | | |
|---|---|---|
| DS26303 | 3.3V, E1/T1/J1, Short-Haul, Octal Line Interface Unit | Free Samples |

**More Information**
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 3916: http://www.maximintegrated.com/an3916
APPLICATION NOTE 3916, AN3916, AN 3916, APP3916, Appnote3916, Appnote 3916