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Connecting the VFLT Pin of the 71M6515H

This document describes the proper connection of the VFLT pin controlling the built-in watchdog timer of the 71M6515H Energy Meter ICs.

Background

The VFLT pin is used to monitor an external DC voltage representative of the on-board DC supply voltage. When the voltage at VFLT falls below 1.5V (VBIAS), the digital parts of the chip enter their safe reset state, and battery back-up protection for the RTC, the crystal oscillator and the RAM is enabled.

The VFLT pin is also used to control the on-chip watchdog timer of the 71M6515H. When the voltage at VFLT is close to V3P3 (V3P3 – 10mV to V3P3 - 400mV), the watchdog timer is disabled. When the voltage at VFLT is between 1.5V and V3P3 – 400mV, the watchdog timer is enabled. Once the watchdog timer is enabled, a chip hardware reset is automatically executed, unless the watchdog timer is triggered (reset) at least every 1.5 seconds. There is no way to disable the watchdog timer other than by tying the VFLT pin to a voltage close to V3P3.

Proper Connection of the VFLT Pin

The 71M6515H was designed to work without a watchdog timer, because the host performs close monitoring of the 71M6515H when working in the operation modes recommended by TERIDIAN. This close monitoring, which involves the 71M6515H interrupting the host at the end of each accumulation interval, makes a separate watchdog logic unnecessary. When the voltage at the VFLT pin is below V3P3 – 400mV, the on-chip hardware watchdog timer is enabled and will cause frequent hardware resets of the 71M6515H that will disrupt proper operation

The voltage at the VFLT pin has to be pulled up to V3P3 (nominally 3.3VDC) in all designs. In this setting, no hardware resets caused by the watchdog timer will occur.

When monitoring the 71M6515H, the host handles fault conditions as follows:

- Unexpected conditions are signaled by bits in the *STATUS* word of the 71M6515H. The host should monitor the *STATUS* word and respond to the reported conditions. The *BOOTUP* bit signals an un-initialized condition and should cause the host to re-establish the energy-relevant registers of the 71M6515H.
- A missing interrupt from the 71M6515H should be detected by a time-out logic set at a time slightly longer than the expected accumulation interval. When encountering a missing interrupt, the host should reset and re-initialize the 71M6515H.

More details on communication between 71M6515H and the host can be found in the 71M6515H Data Sheet.

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