

PCN Number:	20160222000A		PCN Date:	Oct. 12, 2016	
Title:	Qualification of TI Taiwan as Additional Assembly Site for Select SOIC Package Devices				
Customer Contact:	PCN Manager	Dept:	Quality Services		
Change Type:					
<input checked="" type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site	<input type="checkbox"/>	Wafer Fab Site
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Materials
		<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

PCN Details

Description of Change:

Revision A is to update the description of change to provide additional information on the lead finish type and marking format for the affected devices. We apologize for any inconvenience this may have caused.

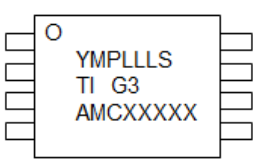
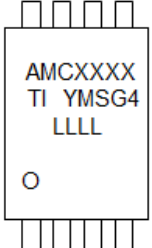
Texas Instruments Incorporated is announcing the qualification TI Taiwan as Additional Assembly Site for select devices listed in the "Product Affected" Section. Current assembly sites and Material differences are as follows.

Assembly Site	Assembly Site Origin	Assembly Country Code	Assembly Site City
ASE Shanghai	ASH	CN	Shanghai
TI Taiwan	TAI	TW	Chung Ho, New Taipei City

Material Differences:

	ASE Shanghai	TI Taiwan
Lead finish	Matte Sn	NiPdAu
Mold compound	EN2000510	4221499
Mount Compound	EY1000063	4211470

Marking Format:

ASE Shanghai	TI Taiwan
 <p> TI = TI Letters YM = Year Month Code P = Secondary Site Code LLL = Lot Trace Code S = Assembly Site Code O = Pin 1 </p>	 <p> TI = TI Letters YM = Year Month Code LLL = Lot Trace Code S = Assembly Site Code O = Pin 1 </p>

Reason for Change:

Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Anticipated impact on Material Declaration

<input type="checkbox"/>	No Impact to the Material Declaration	<input checked="" type="checkbox"/>	Material Declarations or Product Content reports are driven from production data and will be available following the production release. Upon production release the revised reports can be obtained from the TI ECO website .
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Changes to product identification resulting from this PCN:

Assembly Site		
ASE Shanghai	Assembly Site Origin (22L)	ASO: ASH
TI-Taiwan	Assembly Site Origin (22L)	ASO: TAI

Sample product shipping label (not actual product label)

ASSEMBLY SITE CODES: ASE Shanghai = A, TI-Taiwan = T

Product Affected:

AMC1100DWV	AMC1100DWVR	AMC1200BDWV	AMC1200BDWVR
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Qualification Report

AMC1200TDWVRQ1 (2 die MCM) using die rev CAMC1200GANZ in a new package
Approved 19-Feb-2016

Product Attributes

Attributes	Qual Device: AMC1200TDWVRQ1
Wafer Fab Supplier	DMOS 5, TSMC
Die Revision	F, G
Assembly Site	TITL
Package Type	SOP
Package Designator	DWV
Ball/Lead Count	8

- QBS: Qual By Similarity
- Qual Device AMC1200TDWVRQ1 is qualified at LEVEL2-260C
- Device AMC1200TDWVRQ1 contains multiple dies.

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: AMC1200TDWVRQ1
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	3/231/0
AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0
TC-WBP	A4	MIL-STD883 Method 2011	1	30	Post Temp. Cycle Bond Pull	Wires	1/30/0
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp. Storage Bake, 150C	1000 Hours	3/135/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 150C	408 Hours	3/231/0
WBS	C1	AEC Q100-001	1	30	Bond Shear	Wires	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull	Wires	3/90/0
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability	Pb Free	1/15/0

SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability	Pb	1/15/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	--	3/30/0
HBM	E2	AEC Q100-002	1	3	ESD – HBM	2500 V	1/3/0
CDM	E3	AEC Q100-011	1	3	ESD - CDM	1000 V	1/3/0
LU	E4	AEC Q100-004	1	6	Latch-up	JES78	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Per datasheet parameters	3/90/0

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

- The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com