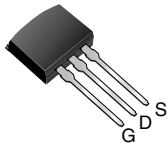
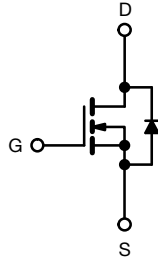
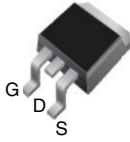


Power MOSFET

I²PAK (TO-262)

D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

| PRODUCT SUMMARY | | |
|--------------------------------|-----------------|-----|
| V_{DS} (V) | 400 | |
| $R_{DS(on)}$ max. (Ω) | $V_{GS} = 10$ V | 1.0 |
| Q_g max. (nC) | 22 | |
| Q_{gs} (nC) | 5.8 | |
| Q_{gd} (nC) | 9.3 | |
| Configuration | Single | |

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Single transistor flyback Xfmr. reset
- Single transistor forward Xfmr. reset (both US line input only)

| ORDERING INFORMATION | | | | |
|---------------------------------|-----------------------------|-------------------------------|-------------------------------|-----------------------------|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) | I ² PAK (TO-262) |
| Lead (Pb)-free and halogen-free | SiHF730AS-GE3 | SiHF730ASTRL-GE3 ^a | SiHF730ASTRR-GE3 ^a | SiHF730AL-GE3 |
| Lead (Pb)-free | IRF730ASPbF | IRF730ASTRLPbF ^a | - | - |

Note

a. See device orientation.

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted) | | | | | |
|---|------------------|----------------|-------------|------|---|
| PARAMETER | SYMBOL | | LIMIT | UNIT | |
| Drain-source voltage | V_{DS} | | 400 | V | |
| Gate-source voltage | V_{GS} | | ± 30 | | |
| Continuous drain current | V_{GS} at 10 V | $T_C = 25$ °C | 5.5 | A | |
| | | $T_C = 100$ °C | 3.5 | | |
| Pulsed drain current ^{a, e} | I_{DM} | | 22 | | |
| Linear derating factor | | | 0.6 | W/°C | |
| Single pulse avalanche energy ^{b, e} | E_{AS} | | 290 | mJ | |
| Avalanche current ^a | I_{AR} | | 5.5 | A | |
| Repetitive avalanche energy ^a | E_{AR} | | 7.4 | mJ | |
| Maximum power dissipation | $T_C = 25$ °C | | P_D | 74 | W |
| Peak diode recovery dV/dt ^{c, e} | dV/dt | | 4.6 | V/ns | |
| Operating junction and storage temperature range | T_J, T_{stg} | | -55 to +150 | °C | |
| Soldering recommendations (peak temperature) ^d | for 10 s | | 300 | | |

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25$ °C, $L = 19$ mH, $R_g = 25$ Ω , $I_{AS} = 5.5$ A (see fig. 12)
- $I_{SD} \leq 5.5$ A, $dI/dt \leq 90$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C
- 1.6 mm from case
- Uses IRF730A, SiHF730A data and test conditions



| THERMAL RESISTANCE RATINGS | | | | |
|--|-------------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient (PCB mounted, steady-state) ^a | R _{thJA} | - | 40 | °C/W |
| Maximum junction-to-case (drain) | R _{thJC} | - | 1.7 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

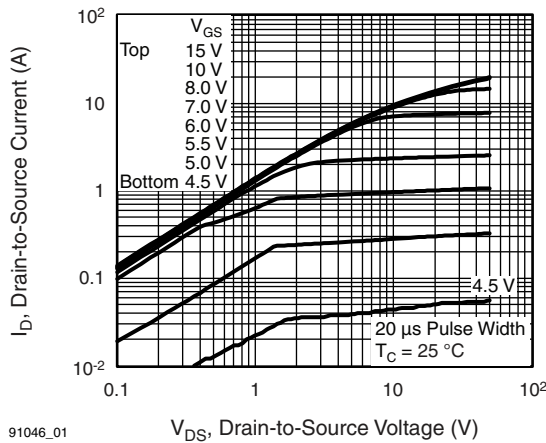
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|---|----------------------------------|---|--------------------------------------|------|-------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | |
| Drain-source breakdown voltage | V _{DS} | V _{GS} = 0, I _D = 250 μA | 400 | - | - | V |
| V _{DS} temperature coefficient | ΔV _{DS} /T _J | Reference to 25 °C, I _D = 1 mA ^d | - | 0.5 | - | V/°C |
| Gate-source threshold voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 2.0 | - | 4.5 | V |
| Gate-Source Leakage | I _{GSS} | V _{GS} = ± 30 V | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 400 V, V _{GS} = 0 V | - | - | 25 | μA |
| | | V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C | - | - | 250 | |
| Drain-Source On-State Resistance | R _{DSON} | V _{GS} = 10 V, I _D = 3.3 A ^b | - | - | 1.0 | Ω |
| Forward Transconductance | g _{fs} | V _{DS} = 50 V, I _D = 3.3 A ^d | 3.1 | - | - | S |
| Dynamic | | | | | | |
| Input Capacitance | C _{iss} | V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^d | - | 600 | - | pF |
| Output Capacitance | C _{oss} | | - | 103 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 4.0 | - | |
| Output Capacitance | C _{oss} | V _{GS} = 0 V | V _{DS} = 1.0 V, f = 1.0 MHz | - | 890 | - |
| | | | V _{DS} = 320 V, f = 1.0 MHz | - | 30 | - |
| Effective Output Capacitance | C _{oss eff.} | V _{DS} = 0 V to 320 V ^{c, d} | - | 45 | - | |
| Total Gate Charge | Q _g | V _{GS} = 10 V, I _D = 3.5 A, V _{DS} = 320 V, see fig. 6 and 13 ^{b, d} | - | - | 22 | nC |
| Gate-Source Charge | Q _{gs} | | - | - | 5.8 | |
| Gate-Drain Charge | Q _{gd} | | - | - | 9.3 | |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 200 V, I _D = 3.5 A, R _g = 12 Ω, R _D = 57 Ω, see fig. 10 ^{b, d} | - | 10 | - | ns |
| Rise Time | t _r | | - | 22 | - | |
| Turn-Off Delay Time | t _{d(off)} | | - | 20 | - | |
| Fall Time | t _f | | - | 16 | - | |
| Gate Input Resistance | R _g | f = 1 MHz, open drain | 2.7 | - | 10.9 | Ω |
| Drain-Source Body Diode Characteristics | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 5.5 | A |
| Pulsed Diode Forward Current ^a | I _{SM} | | - | - | 22 | |
| Body Diode Voltage | V _{SD} | T _J = 25 °C, I _S = 5.5 A, V _{GS} = 0 V ^b | - | - | 1.6 | V |
| Body Diode Reverse Recovery Time | t _{rr} | T _J = 25 °C, I _F = 3.5 A, di/dt = 100 A/μs ^{b, d} | - | 370 | 550 | ns |
| Body Diode Reverse Recovery Charge | Q _{rr} | | - | 1.6 | 2.4 | μC |
| Forward Turn-On Time | t _{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D) | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
- d. Uses IRF730A, SiHF730A data and test conditions.

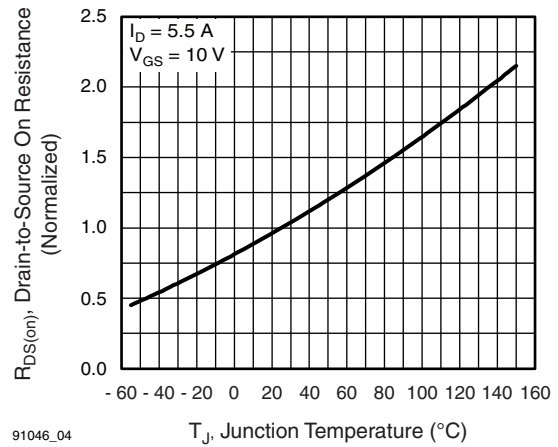


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



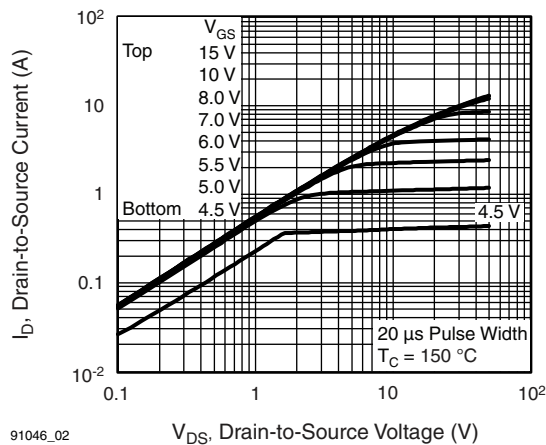
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Fig. 1 - Typical Output Characteristics



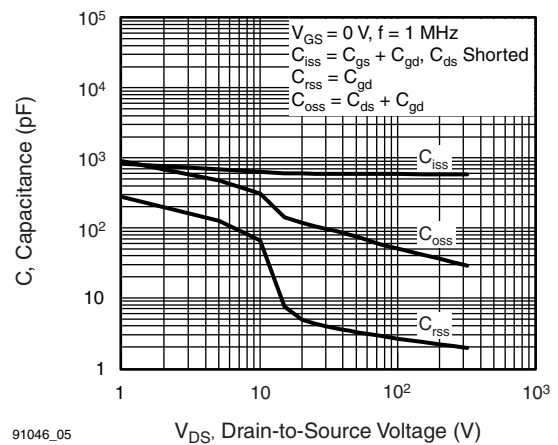
91046_04

Fig. 4 - Normalized On-Resistance vs. Temperature



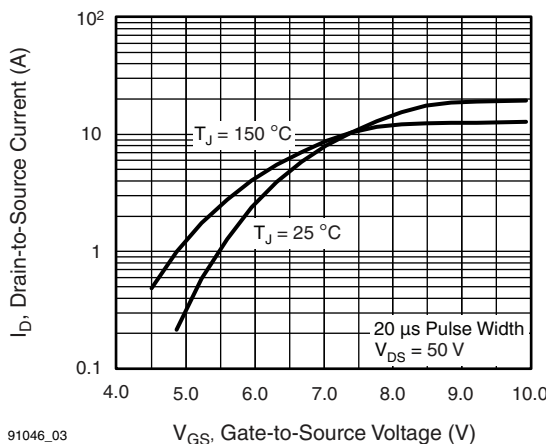
91046_02

Fig. 2 - Typical Output Characteristics



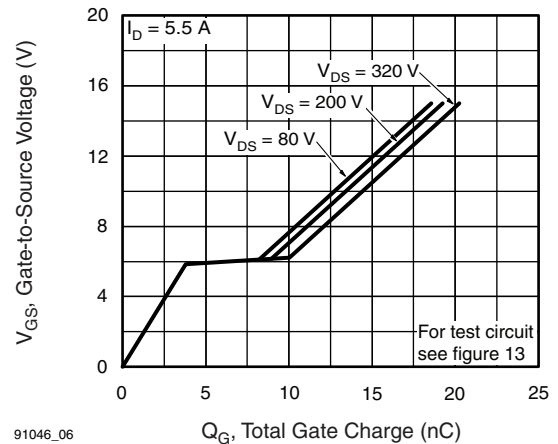
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Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



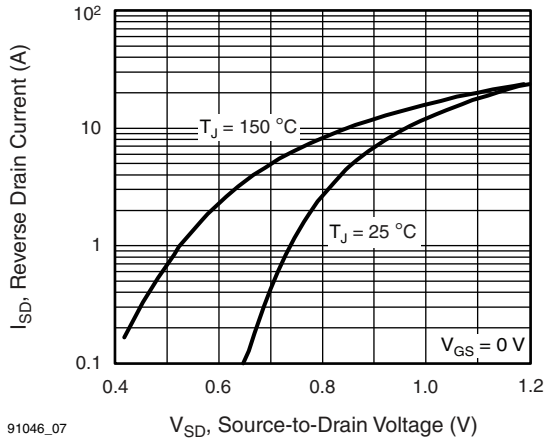
91046_03

Fig. 3 - Typical Transfer Characteristics



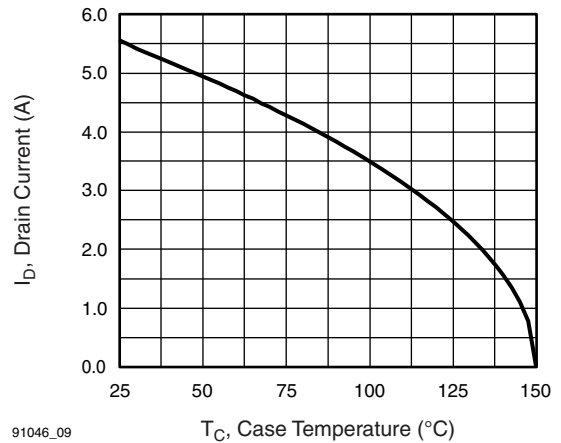
91046_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



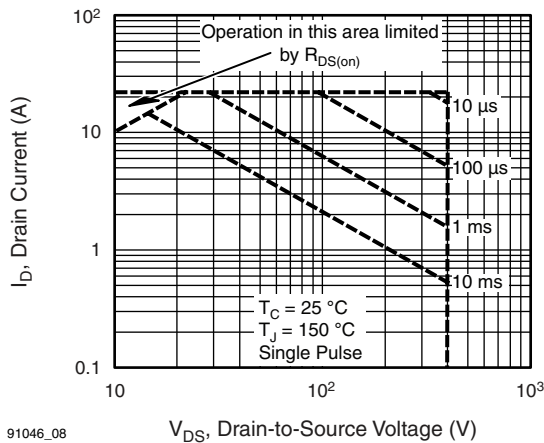
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Fig. 7 - Typical Source-Drain Diode Forward Voltage



91046_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91046_08

Fig. 8 - Maximum Safe Operating Area

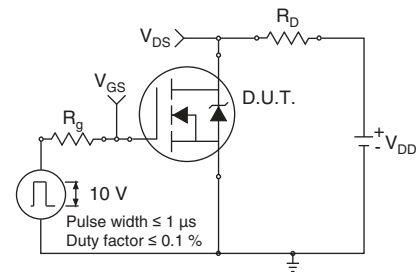


Fig. 10a - Switching Time Test Circuit

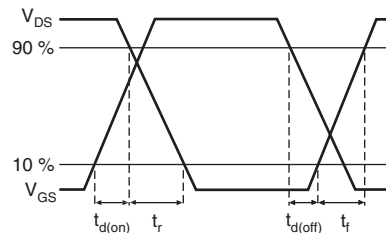
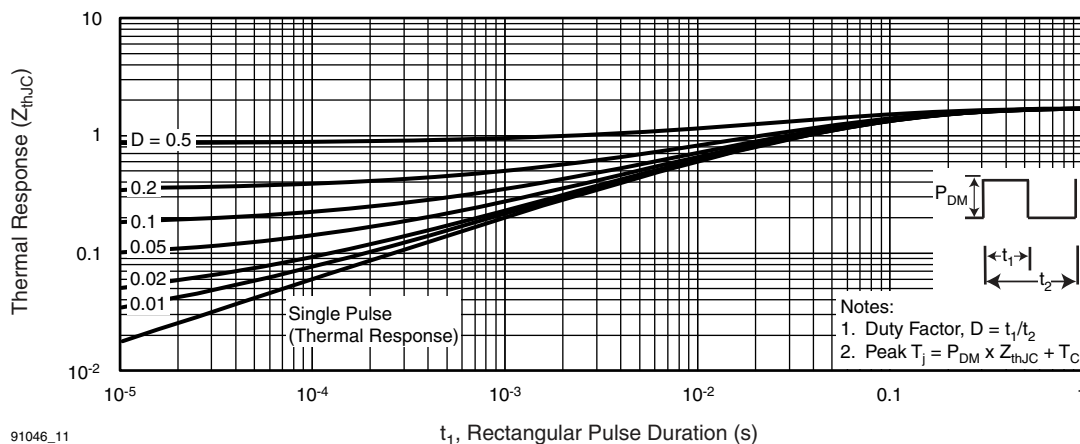


Fig. 10b - Switching Time Waveforms



91046_11

t_1 , Rectangular Pulse Duration (s)

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

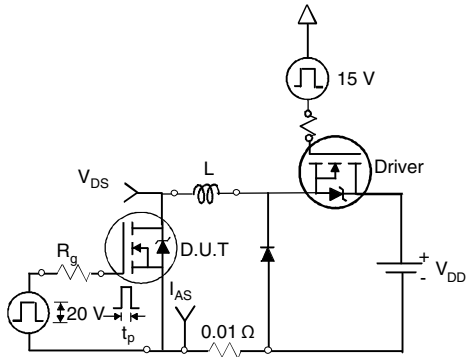


Fig. 12a - Unclamped Inductive Test Circuit

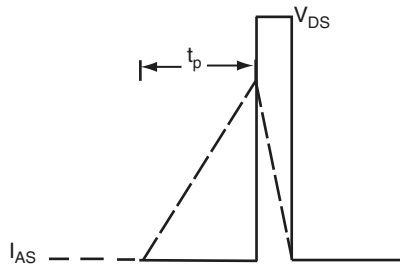


Fig. 12b - Unclamped Inductive Waveforms

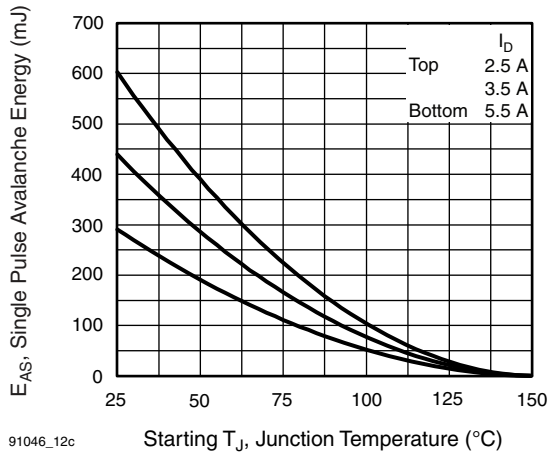


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

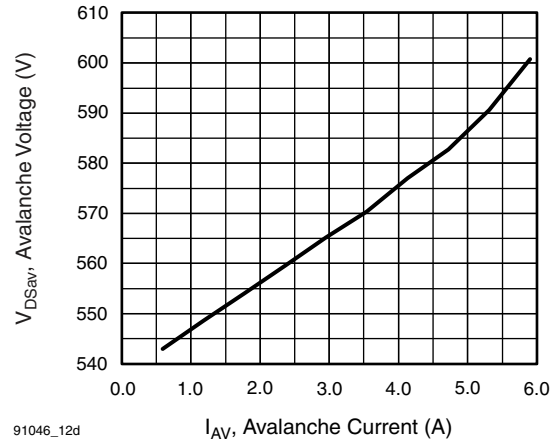


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

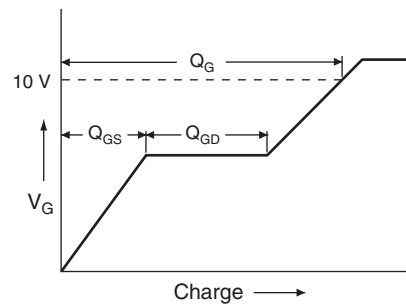


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

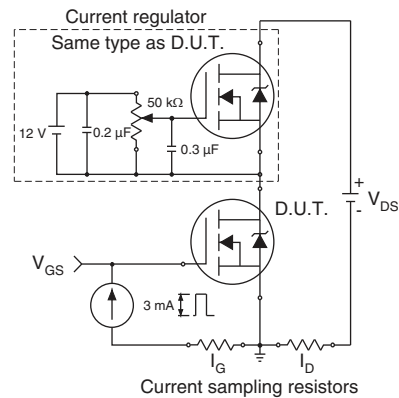
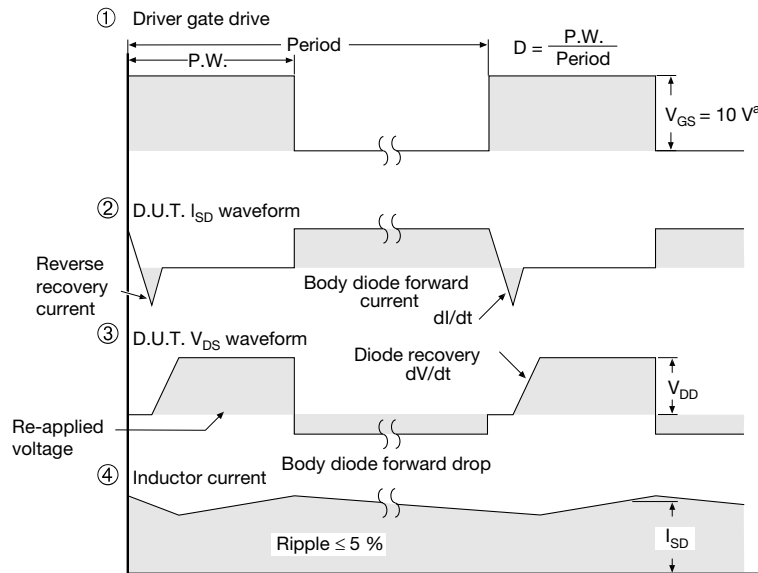
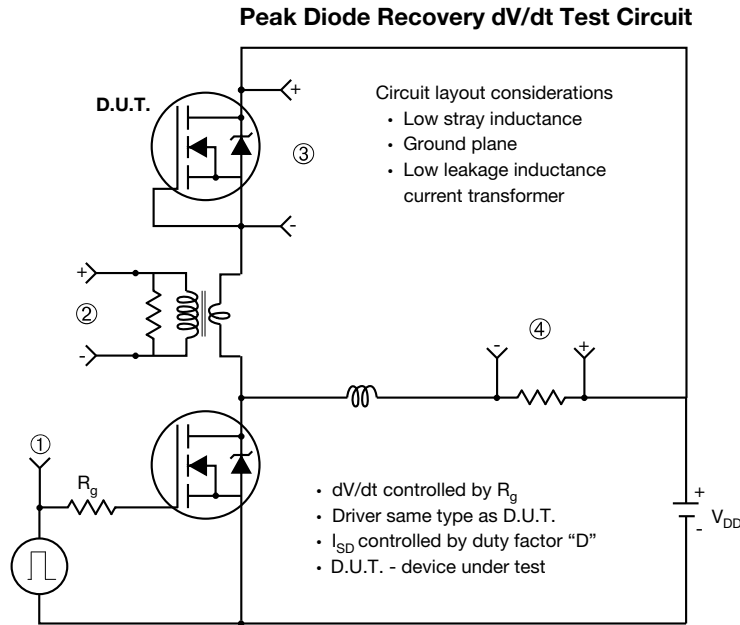


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

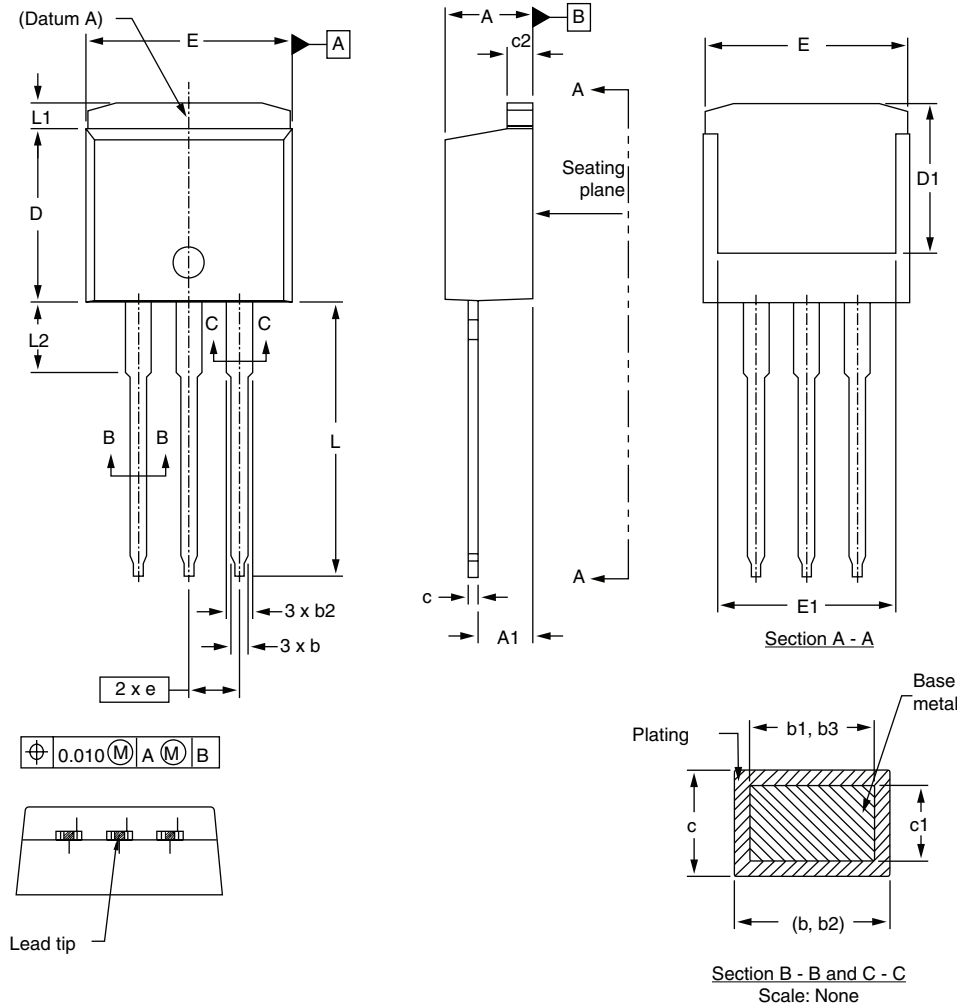
| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 2.03 | 3.02 | 0.080 | 0.119 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D | 8.38 | 9.65 | 0.330 | 0.380 |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.46 | 14.10 | 0.530 | 0.555 |
| L1 | - | 1.65 | - | 0.065 |
| L2 | 3.56 | 3.71 | 0.140 | 0.146 |

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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