



Process Change Notification

PCN Number: PCN-2016-57

PCN Notification Date: 09/30/2016

Initial PCN

STATS ChipPAC* Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA

Dear Customer,

This is notification of the STATS ChipPAC* Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA. STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.

The described change(s) within this PCN will not take effect (i.e. Shipped) any earlier than **90** days from Initial PCN notification or the successful completion of the Cirrus Logic qualification, unless a customer agreement has been reached on an earlier implementation of the identified process change.

Cirrus Logic requests acknowledgement of receipt for this Initial PCN notification within 30 calendar days and acceptance of the identified change(s) within 90 days from receipt. Shipment of said material will commence after the 90 day period or upon successful completion of the Cirrus Logic defined qualification; lack of acknowledgement / communication is considered as acceptance.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and assistance in this respective matter. Any specific or immediate inquiries should be directed to your local Field Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

* - STATS ChipPAC was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015.



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Products Affected:

The devices listed on subsequent pages are the complete list of affected devices. According to our records, one or more of these devices have been purchased by your organization within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	STATS ChipPAC* Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA		
Customer Contact:	Local Field Sales Representative	Phone: (512) 851-4000	Dept: Corporate Quality
Proposed 1st Ship Date:	Q1_2017	Estimated Sample Availability Date:	Q1_2017
Change Type:	Site Transfer: Change Type = Major, but considered Minor; as the subcontractor (STATS ChipPAC*) is an existing qualified supplier for Cirrus Logic and there are no changes to the equipment or material.		
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Assembly Process
<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Wafer Fab Process
<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Test Site	<input type="checkbox"/>	Test Process
<input type="checkbox"/>	Electrical Specification	<input type="checkbox"/>	Mechanical Specification
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Other
Comments:			

PCN Details
<p>Description of Change:</p> <p>Cirrus Logic is qualifying the STATS ChipPAC* Test and Final Pack Site Transfer from Shanghai to Jiangyin CHINA.</p> <p>Below you will find an outline of the described changes for these components:</p> <p>Special Note: Change Type = Major, but considered Minor. The subcontractor (STATS ChipPAC*) is an existing qualified supplier and all material as well as equipment associated with the Test and Final Pack Site processes will not change.</p> <ul style="list-style-type: none"> Test and Final Pack Site Change: <p>From: STATS ChipPAC* site location in Shanghai CHINA To: STATS ChipPAC* site location in Jiangyin CHINA</p>
<p>Reason for Change:</p> <p>STATS ChipPAC* was acquired by Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET) in 2015. All assets will be consolidating to the JCET site location in Jiangyin CHINA targeted for the end of Q1_2017.</p>

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Special Note:

Earlier production level material may be available from the qualified Jiangyin CHINA site location, but shipment(s) from Cirrus Logic are contingent on successful qualification completion of the designated site transfer.

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No anticipated adverse impact to the Quality and/or Reliability of said product; as the transfer site is part of an already existing Cirrus Logic qualified subcontractor STATS ChipPAC* and there are no changes to the equipment or material.

Product Affected:

Cirrus Logic Part Number(s):

CS4365-DQZ[R]/B
CS4385-DQZ[R]/B
CS4385A-DQZ[R]/B1

Changes To Product Identification Resulting From This PCN:

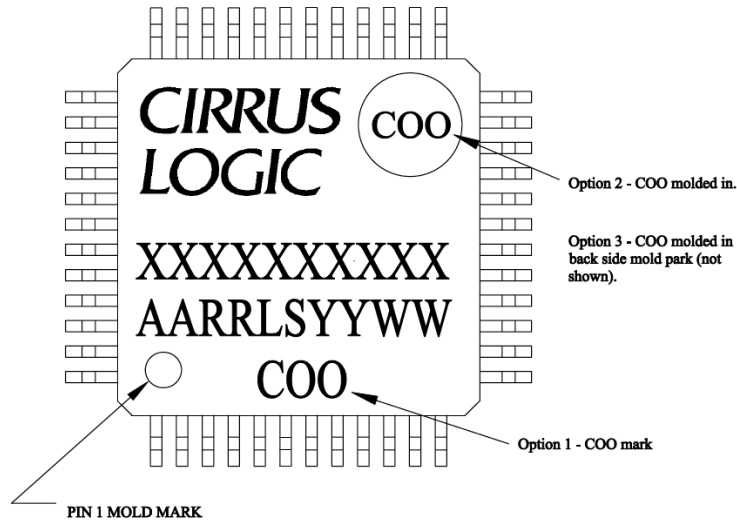
The Cirrus Logic component symbolization on the external face will remain the same.

Top Side Mark:

Mark Lay-out	Top Side Brand	STATS ChipPAC (Shanghai CHINA)	STATS ChipPAC (Jiangyin CHINA)	Comparison Results
See Below Illustration	Logo Line	CIRRUS	CIRRUS	Same
	1st Line: Cirrus Part Number	CS43x5[A]-xQZ[R]/Bx	CS43x5[A]-xQZ[R]/Bx	Same
	2nd Line: Package Mark	(BARRLSYYWW) Site Code = AA Die Rev = RR LS = Lot Sequence Code YY = Year of Manufacture WW = Work Week of Manufacture	(BARRLSYYWW) Site Code = AA Die Rev = RR LS = Lot Sequence Code YY = Year of Manufacture WW = Work Week of Manufacture	Same
	3rd Line: Country of Origin (COO)	CN	CN	Same

Note: *Lot code and Date code characters vary according to the lot and timeframe of build

Below is a 2D representative image of the Package: MF (Mark Format) = 233 Rev A



TOP SIDE BRAND

CIRRUS
 Logo Line: LOGIC stacked logo
 Line 1: Part Number (10 spaces max.)
 Line 2: Package Mark (10 spaces max.)
 Line 3: Country of Origin (COO). Not required if molded into package. See Options 1, 2, and 3 below.

PACKAGE MARK FIELDS

AA = Assembly Site Code
 RR = Die Rev Code
 LS = Lot Sequence Number Code
 YY = Year of Manufacture
 WW = Work Week of Manufacture

Test Site Qualification Plan

Purpose
STATS ChipPAC* Test Site Transfer from Shanghai to Jiangyin CHINA

The Equipment Platform Technology, Hardware and Software remain the same.
The Visual / Mechanical inspection and Tape and Reel operations are compliant to JEDEC industry standards.

The Test Equipment Correlation involves the following:

- Running the new site program with an OPEN Socket (No Unit) to ensure "All" tests fail.
- Serializing Control (Known Good) Units and testing the material on both test platforms (Existing and New Location) at all applicable test temperatures utilizing the same load-board and test site(s). A correlation comparison will be made on "All" individual components. If there is a concern or a discrepancy exists, a bench level correlation will be performed to ensure new site meets data sheet requirements.
- Performing Bin yield and Bin movement correlation by running samples at the existing Shanghai (SCC) site and at new Jiangyin site (JSCC). The results from each site will be compared.
- Running (the same) sample non-continuity failures (different failing tests) and testing them at the existing site and at the new site. All units are expected to fail at the new site location.
- Performing GR&R (Gauge Repeatability & Reproducibility)

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Final Pack Review and Results

Purpose
STATS ChipPAC* Final Pack Site transfer from Shanghai to Jiangyin CHINA

Lead Inspection: Sample lot run

ESD Management System: Compliant to ANSI / ESD S20.20 and ISO/TS16949: 2009 Standard Requirements

Final Pack Criteria Representative Flow: (Example Only)

Final Pack Label Formatting: (Example Only)

Final Pack Representative Label: (Example Only)

Final Pack Drop Test Methodology and Results: Compliant to EIA-481 and ISTA 2A

Methodology:

Success Criterion:

Results Summary: